FEB2 Configuration Overview and Development

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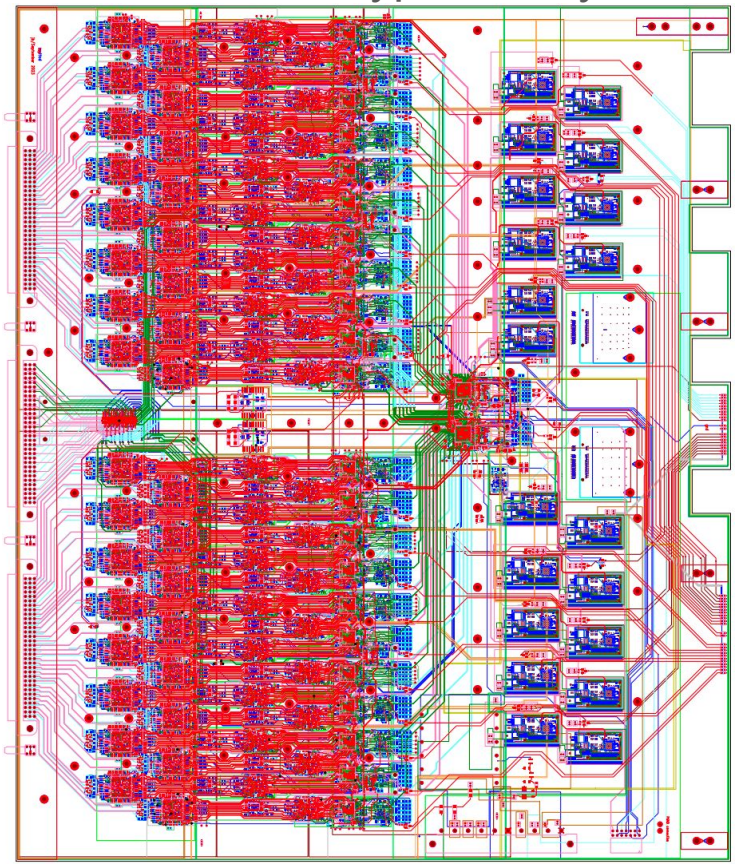
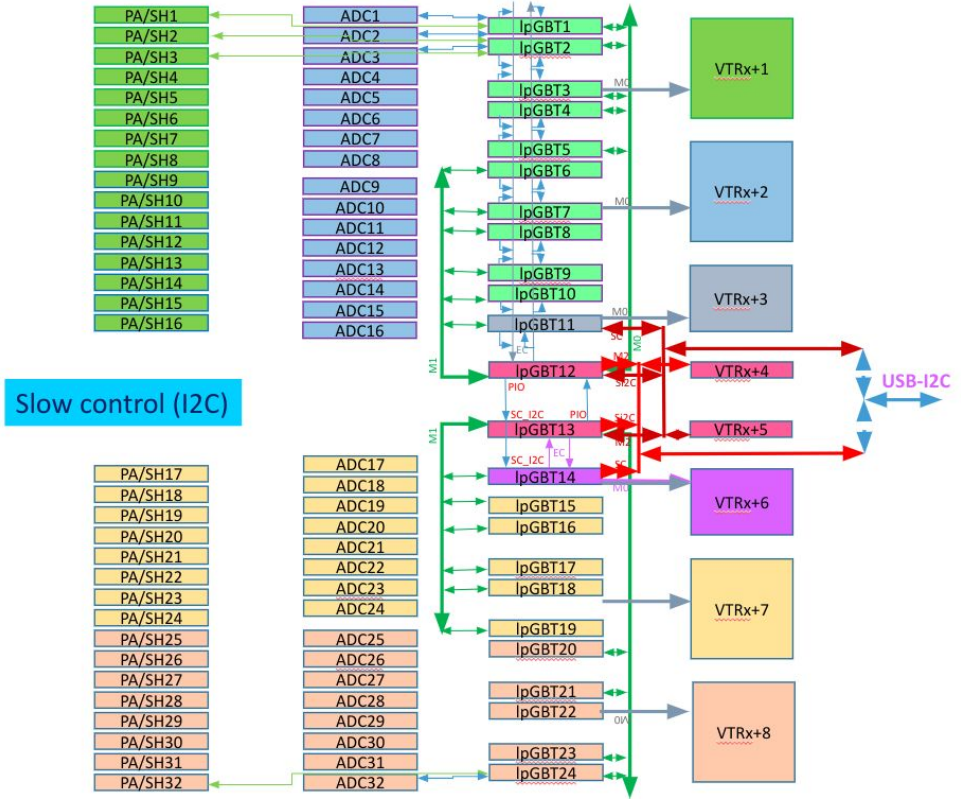
FEB2 Overview and Configurable Chips

FEB2 Prototype v2 Layout



Block Diagram Showing I2C Connections between Configurable Chips



FEB2 Configuration Requirements

- On power-on only the “control” lpGBTs 12 and 13 are on
- Starting from this state the entire board must be sequentially powered on and configured
- Board elements requiring configuration
  - Control lpGBTs : lpGBTs operating in transceiver mode that can use the IC slow control interface via the optical link
  - Data lpGBTs: lpGBTs operating in simplex mode that can be configured via I2C or EC slow control connections
  - COLUTAs : ADCs configured via the I2C interface provided by configured data lpGBTs
    - the slowest element in the system to configure
  - ALFE2s: PA/S configured via the I2C interface provided by configured data lpGBTs
  - VTRx+s: Optical driver chips configured via data lpGBT I2C interface
- In summary the key slow control interfaces are IC, EC and I2C
  - Board power-on, initialization and configuration are built on these interfaces

IC/EC Interfaces to lpGBTs

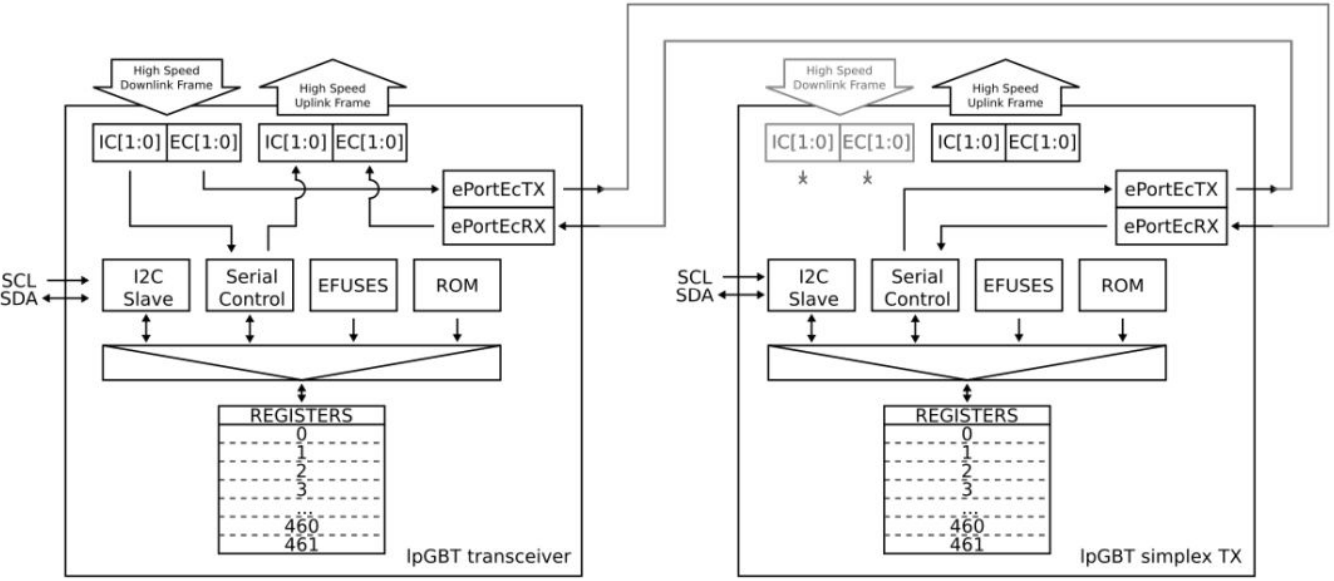


Fig. 3.1: lpGBT configuration

Table 3.3: IC/EC channel frame structure sent to lpGBT for a write-

ID	Description	Parity check
A	Frame delimiter 8'b 01111110	No
B	lpGBT address (7 bits) + R/W bit = 0	Yes
C	Command [7:0]	Yes
D	Number of data words n[7:0]	Yes
D	Number of data words n[8:8]	Yes
E	Memory address [7:0]	Yes
E	Memory address [15:8]	Yes
F	1st data (8 bits)	Yes
F	. . .	Yes
F	nth data (8 bits)	Yes
G	Parity word (8 bits)	Yes
A	Frame delimiter 8'b 01111110	No

Table 3.4: IC/EC channel frame structure sent to lpGBT for a read-

ID	Description	Parity check
A	Frame delimiter 8'b 01111110	No
B	lpGBT address (7 bits) + R/W bit = 1	Yes
C	Command [7:0]	Yes
D	Number of data words n[7:0]	Yes
D	Number of data words n[8:8]	Yes
E	Memory address [7:0]	Yes
E	Memory address [15:8]	Yes
G	Parity word (8 bits)	Yes
A	Frame delimiter 8'b 01111110	No

- lpGBT manual describes the IC/EC interfaces in depth
- Key point is that the "control" lpGBTs are configured via IC
- Data lpGBTs are configured via EC
- However in case where control lpGBT optical link fails, backup "I2C" configuration via the other control lpGBT might be required, "redundant mode"

I2C Interfaces to On-Board Chips

- Chips on lpGBT I2C buses use different I2C protocols
  - lpGBTs,VTRx+,ALFE2 : use 7-bit addressing
  - COLUTA ADCs use 10-bit addressing, different addressing mode for “channel” vs “global” configuration registers
- All of these I2C transactions are based on the I2C multi-byte write/read processes implemented in the lpGBTs

12.3.13 I2C_WRITE_MULTI (0xC)

Writing this command will immediately start a write transaction on the I2C bus. The user must write the correct Address word BEFORE writing this command. On the I2C bus, the master first transmits the 7-bit slave address with R/W=0, and then the Data bytes. The Data bytes are those previously written to the master using the commands I2C_W_MULTI_4BYTE3,2,1,0. The number of transmitted Data bytes is according to the value of bits [6:2] of the Control Register.

Table 12.18: I2C_WRITE_MULTI command

AddressExt	unused
Address	7-bit I2C address of target slave
Data0	unused
Data1	unused
Data2	unused
Data3	unused
Read	unused
ReadByte	unused

12.3.15 I2C_WRITE_MULTI_EXT (0xE)

Writing this command will immediately start a write transaction on the I2C bus. The user must write the correct Address word BEFORE writing this command. On the I2C bus, the master first transmits the 10-bit slave address with R/W=0, and then the Data bytes. The Data bytes are those previously written to the master using the commands I2C_W_MULTI_4BYTE3,2,1,0. The number of transmitted Data bytes is according to the value of bits [6:2] of the Control Register and it is limited to 15.

Table 12.20: I2C_WRITE_MULTI_EXT command

AddressExt	Bits[9:7] of 10-bit I2C address of target slave
Address	Bits[6:0] of 10-bit I2C address of target slave
Data0	unused
Data1	unused
Data2	unused
Data3	unused
Read	unused
ReadByte	unused

COLUTA ADC Configuration

COLUTAv4 Channel Configuration Bits

544 channel configuration bits sent as 68 bytes divided between 12 individual I2C write commands. Each I2C write includes 6 config bytes and 2 subaddressing fields defined below. Note there is some duplication in the data written between write #10 and #11.

#	BYTE0	BYTE1	BYTE2	BYTE3	BYTE4	BYTE5	BYTE6	BYTE7
0	ADCSEL	W+R+0x0	DATA0	DATA1	DATA2	DATA3	DATA4	DATA5
1	ADCSEL	W+R+0x3	DATA6	DATA7	DATA8	DATA9	DATA10	DATA11
2	ADCSEL	W+R+0x6	DATA12	DATA13	DATA14	DATA15	DATA16	DATA17
3	ADCSEL	W+R+0x9	DATA18	DATA19	DATA20	DATA21	DATA22	DATA23
4	ADCSEL	W+R+0xC	DATA24	DATA25	DATA26	DATA27	DATA28	DATA29
5	ADCSEL	W+R+0xF	DATA30	DATA31	DATA32	DATA33	DATA34	DATA35
6	ADCSEL	W+R+0x12	DATA36	DATA37	DATA38	DATA39	DATA40	DATA41
7	ADCSEL	W+R+0x15	DATA42	DATA43	DATA44	DATA45	DATA46	DATA47
8	ADCSEL	W+R+0x18	DATA48	DATA49	DATA50	DATA51	DATA52	DATA53
9	ADCSEL	W+R+0x1B	DATA54	DATA55	DATA56	DATA57	DATA58	DATA59
10	ADCSEL	W+R+0x1E	DATA60	DATA61	DATA62	DATA63	DATA64	DATA65
11	ADCSEL	W+R+0x1F	DATA62	DATA63	DATA64	DATA65	DATA66	DATA67

DATAX = channel configuration data byte, number X goes between 0 to 67
ADCSEL = Channel # select, 1-hot encoding (0x1,0x2,0x4,0x8,0x10,0x20,0x40,0x80)
W = WRITE FLAG
R = READBACK FLAG
The format of BYTE1 specifically is:
BYTE1[7] : WRITE FLAG
BYTE1[6] : READBACK FLAG
BYTE1[4:0] = SUBADDRESS

COLUTAv4 Global Configuration Bits

Global COLUTA configuration bits are sent in two I2C writes each containing eight bytes of configuration data. The 10-bit COLUTA I2C address is modified between these two write, adding 0x8 when sending the lower eight-bytes and 0x10 when sending the upper eight bytes. Example global configuration bits are below:

Write #	10-bit Address Modifier	I2C Write Data in Two 4-Byte Groups
0	0x8	['0x14', '0x41', '0x40', '0x4'] ['0xa0', '0xc2', '0x1f', '0x0']
1	0x10	['0x4', '0x84', '0xb9', '0x76'] ['0xd7', '0x8a', '0xd9', '0x7a']

- COLUTA ADCs configured using the slow control interfaces provided by various data lpGBTs
- Every COLUTA I2C transaction is an 8-byte write/read
- The I2C transaction require a number of writes to the data lpGBTs to set up, so this is the slowest part of the configuration

More on lpGBT Multi-Byte I2C Transactions to COLUTAs

12.3.9 I2C_W_MULTI_4BYTE0 (0x8)

Writing this command will NOT start a transaction on the I2C bus. The 4 bytes of data are stored locally within the I2C master. These data can then be written to a slave by the I2C_WRITE_MULTI or I2C_WRITE_MULTI_EXT commands.

Table 12.14: I2C_W_MULTI_4BYTE0 command

AddressExt	unused
Address	unused
Data0	1st byte for I2C write
Data1	2nd byte for I2C write
Data2	3rd byte for I2C write
Data3	4th byte for I2C write
Read	unused
ReadByte	unused

12.3.10 I2C_W_MULTI_4BYTE1 (0x9)

Writing this command will NOT start a transaction on the I2C bus. The 4 bytes of data are stored locally within the I2C master. These data can then be written to a slave by the I2C_WRITE_MULTI or I2C_WRITE_MULTI_EXT commands.

Table 12.15: I2C_W_MULTI_4BYTE1 command

AddressExt	unused
Address	unused
Data0	5th byte for I2C write
Data1	6th byte for I2C write
Data2	7th byte for I2C write
Data3	8th byte for I2C write
Read	unused
ReadByte	unused

12.3.15 I2C_WRITE_MULTI_EXT (0xE)

Writing this command will immediately start a write transaction on the I2C bus. The user must write the correct Address word BEFORE writing this command. On the I2C bus, the master first transmits the 10-bit slave address with R/W=0, and then the Data bytes. The Data bytes are those previously written to the master using the commands I2C_W_MULTI_4BYTE3,2,1,0. The number of transmitted Data bytes is according to the value of bits [6:2] of the Control Register and it is limited to 15.

Table 12.20: I2C_WRITE_MULTI_EXT command

AddressExt	Bits[9:7] of 10-bit I2C address of target slave
Address	Bits[6:0] of 10-bit I2C address of target slave
Data0	unused
Data1	unused
Data2	unused
Data3	unused
Read	unused
ReadByte	unused

- Setting up and initiating I2C transactions to COLUTA ADCs involves writing the corresponding I2C control registers in the corresponding data lpGBTs
- **This is a multi-step process**
  - Must first “latch” data via lpGBT I2C_W_MULTI_4BYTE0/1 commands

Configuration Requirements

- At minimum the IC/EC interface to control/data lpGBTs should be optimized
  - Multi-byte write/read should be supported
  - Minimal overhead would be ideal
- Ideally the I2C transactions to COLUTA ADCs would be optimized in firmware
  - In principle these transactions are built out of slow-control transaction to the corresponding controller data lpGBT
  - However this is a multi-step process involving “latching” data to the lpGBT logic
  - **Minimizing overhead and dead-time associated with setting up, initiating and verifying these multi-byte I2C transactions will be the most important factor for reducing FEB2 configuration and in-situ calibration time**
    - **“Redundant mode” configuration may require “double hopping” I2C transactions, so optimizing the I2C transaction is important to support this mode**