

FELIX packet structure for FEB2 based on felix doc. Coluta v4 package structure based on coluta datasheet. ADC packets are 160 bits long.

ADC FRAME8 and FRAME1 data are not readout for every chip on the FEB2. For ADCs readout by two lpGBTs (eg ADC2 [1-based counting]), both FRAME1 and FRAME8 are readout, and should match. For ADCs readout by one lpGBT (eg ADC1 and 3), only one or the other is readout; FRAME8 is readout for ADC1; FRAME1 is readout for ADC3. This pattern then repeats for every 3 ADCs upto and including ADC16. The pattern shifts at ADC17, which is readout by one lpGBT, and starts again at ADC18 which is readout by one lpGBT. See the board mapping diagram for a visual.

The trigger mode header event counter increments for each trigger by the FELIX. The sample counter (Smpl Cnt) increments for each sample in a trigger window, resetting for each trigger. The FELIX BCID increments by one for each sample, and resets on the BCR. the ADC BCID increments by one for each sample, rolling over a 32, and resets on the BCR.

Figure 1: Trigger mode header [256 bits]. ‘a’ bit checks alignment of 6 counters (not sure about this).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D				E				A				D				B				E				E				F			
A				A				A				A				5				5				5				5			
6				6				6				6				9				9				9				9			
F				E				D				C				B				A				9				8			
7				6				5				4				3				2				1				0			
0						a	counter				counter				counter				counter				counter				counter				
Event Counter [31:0]																															
0								Smpl Cnt [22:16]								0				FELIX BCID [11:0]											

Figure 2: Trigger Mode data payload. 160 bits per ADC. First frame word is 0x0FA8 and the last frame word is 0x0FA1 for ‘fake data’. Be careful, the payload packing changes based on ADC number, repeating a pattern every 3 ADCs. See the note above regarding a change in the pattern at ADC17.

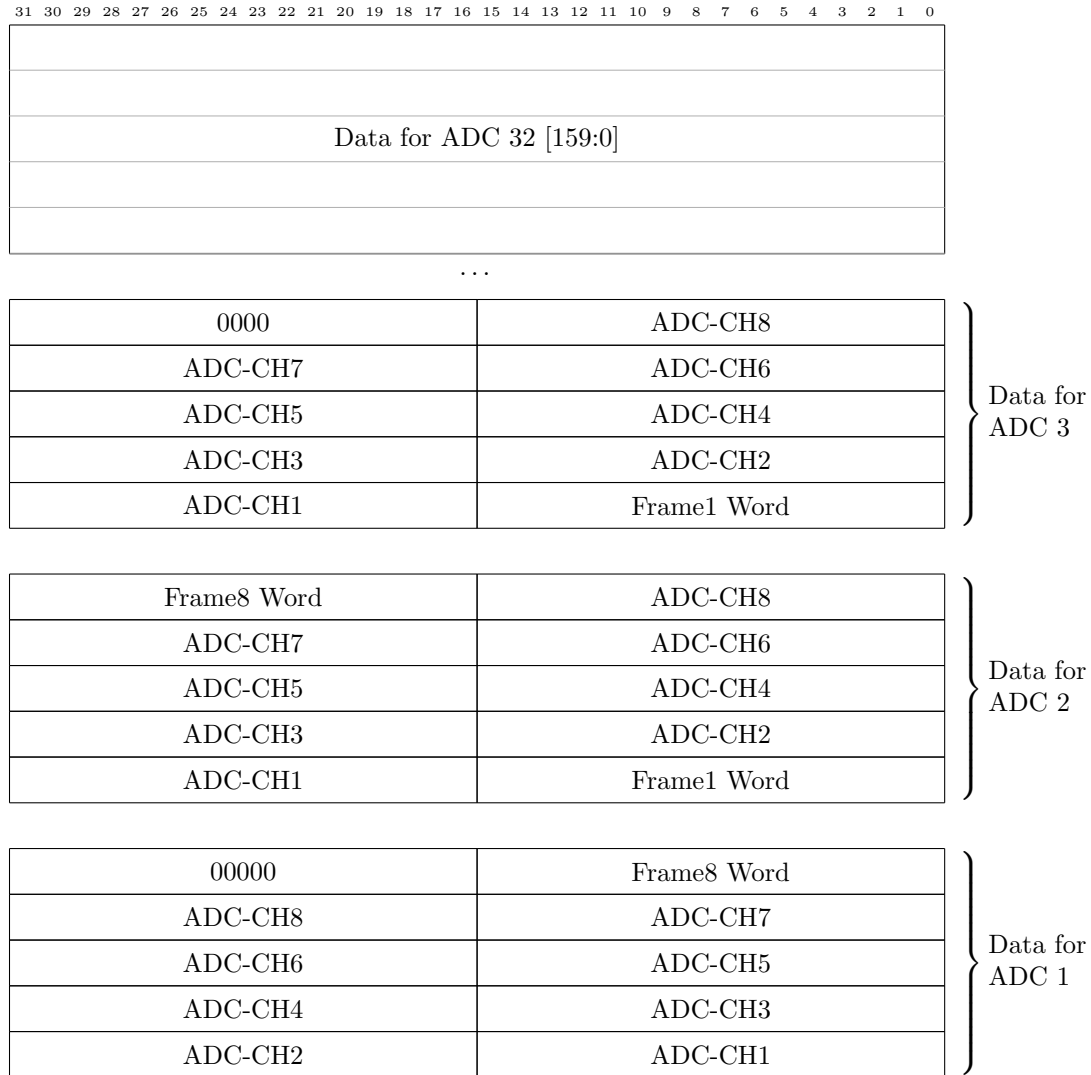


Figure 3: Frame word: the FIRST bit is 0 for non-first samples, and 1 for BCR asserted (and BCID is 0). Data word: the OVER bit is set to 1 for ADC overflow.



Figure 4: Single ADC Mode data payload. ADC data (160 bits) is the same format as above in the trigger readout. ADC data is readout in groups of 3 BCs, and the ‘Trig Counter’ increments every 3 BCs.

