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Versatile Link Plus Technical Specification, part 2.1.3

Quad Laser Driver

Abstract

This document describes the mechanical, electro-optic, and environmental specifications of the Quad Laser Driver for the transmitting path of the front-end Transceiver (VTRx+) module for use in the Versatile Link Plus common project for optical data transmission in HL-LHC detectors.

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Document History

Rev. No	***Date***	***Pages***	***Description of Changes***
1.0	10 Aug 2017	*All*	First Version
1.1	06 Oct 2017	*All*	Updated jitter specifications
1.2	14 May 2018	*8,9*	Updated padframe drawing and description
		14-23	Added Sections on Configurations and SEU tolerance
1.3	9 March 2021	*17-21*	Updated I2C register map for production version (v.5)
1.4	26 May 2023	*18*	Updated GCR default values in section 6.4

Specification Tree

The hierarchy of Versatile Link Plus specifications is shown below. The position of the present specification document is highlighted in bold. Line items in italic will not result in specification documents but are shown to ease understanding of the structure.

	EDMS Document Number
Part 1. System	1719328
Part 2. Components	
Part 2.1 Front-End Transceiver Module	1719329
Part 2.1.1 Laser diode (VCSEL) die	1762631
Part 2.1.2 Photodiode die	1762632
Part 2.1.3 **Laser Driver**	**1719330**
Part 2.1.4 Transimpedance Amplifier	1719333
Part 2.2 Back-End Transceiver	1762899
Part 2.3 Passive Optical Components	1762900
Part 2.3.1 Optical Fibre	*TBD*
Part 2.3.2 Optical Connectors	*TBD*

Contents

Introduction

The Versatile Link Plus (VL+) project [1] aims to provide a multi-gigabit per second optical physical data transmission layer for the readout and control of High Luminosity LHC (HL-LHC) experiments. The implementation of these links is flexible and can be configured at build time or by masking unused channels designated by the user. A basic point-to-point bidirectional system architecture is proposed for which components are currently being assessed and developed. One example is shown in figure 1.

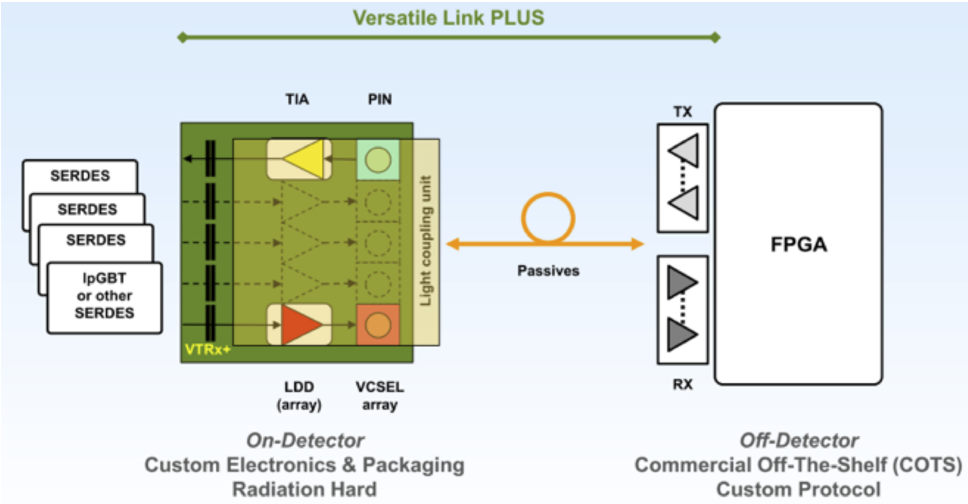

Figure 1: Versatile Link Plus (VL+) Architecture.

The link operation is described in Part 1: System specification, while link components have their dedicated specification in Part 2: Components. This document, Part 2.1.3, describes the specifications and environmental requirements for the quad laser driver for use in front-end Versatile Link Plus transceiver modules. The VL+ front-end components are placed on detector, at the front-end, and are therefore subjected to the harshest environmental conditions and must be capable of reliable operation under those conditions.
The VTRx+ modules may contain the following custom developed or qualified parts (depending upon VTRx+ variant) and channel location (Tx = transmitter, Rx = receiver, TRx = transceiver):

1. VCSEL laser diode array or single die(Tx)
2. Radiation tolerant laserdriver ASICs in quad-channel format (Tx).
3. PIN diode single die (Rx)
4. Radiation tolerant transimpedance amplifier (TIA) in single-channel format (Rx).

Back-end components are placed off detector, outside the harsh radiation and magnetic field environments to which the front-end components are subjected. No specific form factor is required by the project – the user is free to select from a variety of commercially available products which however must meet the VL+ performance specfications for back-end components. A variety of devices are expected to be available for use as parallel back-end components and these have been evaluated for recommendations for edge mounted and mid-board mounted products. All back-end Tx, Rx, and TRx modules are commercial devices compliant to 10 Gbps standards. When used in the VL+, the Rx channels operate at data rates up to 10 Gbps in the uplink direction (in which signals propagate from front-end to back-end) and Tx channels operate nominally at 2.5 Gbps in the downlink direction (in which signals propagate from back-end to front-end).
The link supports multi-mode (MM) operation with a center-wavelength of 850nm. The fiber cables are commercial laser optimized MM fibers, with a radiation resistant section inside the detector if required by the final application.
The link is naturally bi-directional. However, matching the number of front-end to back-end (uplink) and back-end to front-end (downlink) transmissions is not a requirement. It is therefore possible to have separate multi-channel front-end transmitters and single-channel front-end transceivers in the system.

The Quad Laser Driver described in this document is a quad-channel ASIC that will fit inside the VTRx+ module as shown in figure 2. The channel-pitch of 250 um is required to match a VCSEL array coupled to optical fibre ribbon.

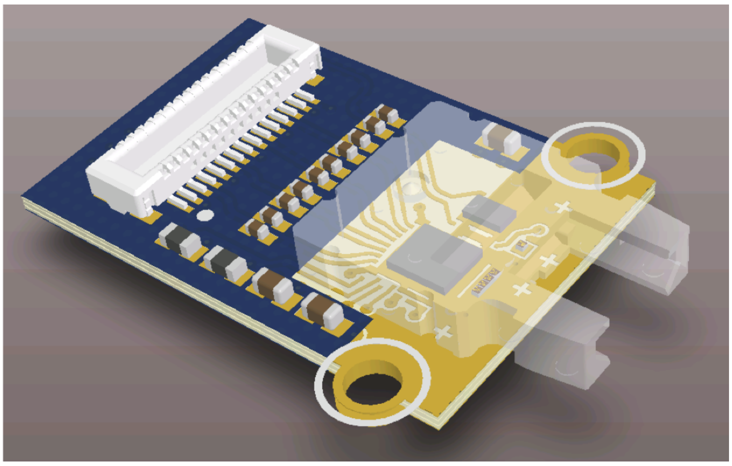

Figure 2: VTRx+ module implementation cartoon, showing the possible position of the Quad Laser Driver as the larger of the two grey boxes on the PCB.

1 General Specifications

Table 1: VL+ Quad Laser Driver general specifications.

#	Specification	Min.	Typ.	Max.	Unit
1.1.1	Datarate	1 (TBC)	5	10	Gb/s
1.1.2	Number of Channels	4		4	

Figure 3: VL+ Quad Laser Driver overview schematic showing main functional blocks.

2 Mechanical Specifications

Outline mechanical dimensions are given in table 2 and the pad frame of the Quad Laser Driver is shown in figure 4. The overall chip dimensions are 1695 µm by 1900 µm. Pad pitch and size are chosen to ease wire-bonding and thus ultimately the module integration. Power, Ground, and configuration bond pads are mirrored so as to allow connection from one side or the other in case more than one quad laser driver dice is placed in an optical module in close proximity. The high-speed input and output channel pitch is 250 µm for integration with VCSEL arrays on that pitch. Pad pitch is 100 µm, which leads to a pad separation of 30 µm. Power and ground pads have been enlarged where possible to allow multiple bond wires to be placed on them. Pad assignment and dimensions are given in table 3

Table 2: VL+ Quad Laser Driver mechanical specifications.

#	Specification	Min.	Typ.	Max.	Unit
2.1.1	Die length		1900		um
2.1.2	Die width		1695		um
2.1.3	Die thickness[a]		200		um
2.1.4	Number of pads			42	

[a] Final production target. Prototype dies are 275 um thick.

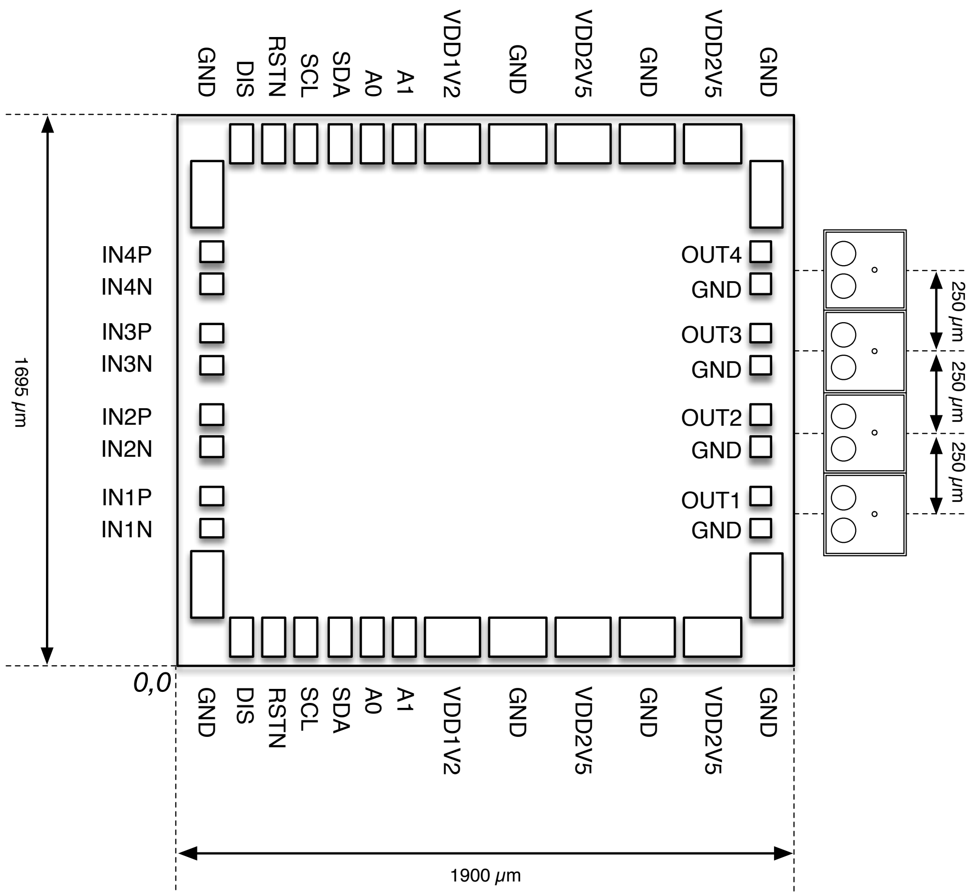

Figure 4: Quad Laser Driver pad frame with dimensions. Pad pitch is 100 µm. Schematic representation of 4-channel VCSEL array shown for reference.

Table 3: VL+ Quad Laser Driver pad details. Positions are pad centres relative to origin in figure 4.

Pad Name	X position (µm)	Y position (µm)	Width (µm)	Height (µm)	Description
GND	86.925	253.225	100	200	Ground connection
DIN1-	95.620	425.725	66	54	Inverting CML input for channel 1
DIN1+	95.620	525.725	66	54	Non-inverting CML input for channel 1
DIN2-	95.620	675.725	66	54	Inverting CML input for channel 2
DIN2+	95.620	775.725	66	54	Non-inverting CML input for channel 2
DIN3-	95.620	925.725	66	54	Inverting CML input for channel 3
DIN3+	95.620	1025.725	66	54	Non-inverting CML input for channel 3
DIN4-	95.620	1175.725	66	54	Inverting CML input for channel 4
DIN4+	95.620	1275.725	66	54	Non-inverting CML input for channel 4
GND	81.120	1448.225	100	200	Ground connection
DIS	196.120	1610.810	70	116	Active-high optical output disable for all channels
RSTN	296.120	1610.810	70	116	Active-low chip reset
SCL	396.120	1610.810	70	116	I^2C clock input, external pull-up to 1.2 V required
SDA	496.120	1610.810	70	116	I^2C data input/output, external pull-up to 1.2 V required
A0	596.120	1610.810	70	116	I^2C address bit 5 of $<6:0>$, internal pull-down
A1	696.120	1610.810	70	116	I^2C address bit 6 of $<6:0>$, internal pull-down
VDD12	846.120	1610.810	170	116	Analogue power at 1.2 V for all functions except output stage
GND	1046.120	1610.810	170	116	Ground connection
VDD25	1246.120	1610.810	170	116	Analogue power at 2.5 V to power output stage with sufficient voltage headroom for VCSEL
GND	1446.120	1610.810	170	116	Ground connection
VDD25	1646.120	1610.810	170	116	Analogue power at 2.5 V to power output stage with sufficient voltage headroom for VCSEL
GND	1811.120	1448.225	100	200	Ground connection
OUT4	1796.620	1275.725	66	54	Current-mode high-speed modulated output for VCSEL Anode connection of channel 4
GND	1796.620	1175.725	66	54	Ground connection for VCSEL Cathode
OUT3	1796.620	1025.725	66	54	Current-mode high-speed modulated output for VCSEL Anode connection of channel 3
GND	1796.620	925.725	66	54	Ground connection for VCSEL Cathode
OUT2	1796.620	775.725	66	54	Current-mode high-speed modulated output for VCSEL Anode connection of channel 2
GND	1796.620	675.725	66	54	Ground connection for VCSEL Cathode
OUT1	1796.620	525.725	66	54	Current-mode high-speed modulated output for VCSEL Anode connection of channel 1
GND	1796.620	425.725	66	54	Ground connection for VCSEL Cathode
GND	1811.120	253.225	100	200	Ground connection
VDD25	1646.120	92.185	170	116	Analogue power at 2.5 V to power output stage with sufficient voltage headroom for VCSEL
GND	1446.120	92.185	170	116	Ground connection
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A0	596.120	92.185	70	116	I^2C address bit 5 of $<6:0>$, internal pull-down
SDA	496.120	92.185	70	116	I^2C data input/output, external pull-up to 1.2 V required
SCL	396.120	92.185	70	116	I^2C clock input, external pull-up to 1.2 V required
RSTN	296.120	92.185	70	116	Active-low chip reset
DIS	196.120	92.185	70	116	Active-high optical output disable for all channels

3 Interface Specifications

Table 4: VL+ Quad Laser Driver interface specifications.

#	Specification	Min.	Typ.	Max.	Unit
3.1.1	Supply Voltage 2V5	2.25	2.5	2.75	V
3.1.2	Supply Current 2V5[a]		50		mA
3.1.3	Supply Current 2V5[b]		100		mA
3.2.1	Supply Voltage 1V2	1.08	1.2	1.32	V
3.2.2	Supply Current 1V2[a]		50		mA
3.2.3	Supply Current 1V2[b]		100		mA

[a] 8 mA bias, 4 mA modulation, all channels on, pre-emphasis disabled
[b] 12 mA bias, 6 mA modulation, all channels on, pre-emphasis enabled

4 Electrical Specifications

Table 5: VL+ Quad Laser Driver functional specifications at data-rate of 10 Gb/s. Bias current is defined as the logical ONE level and modulation current is the difference between logical ZERO and ONE levels.

#	Specification	Min.	Typ.	Max.	Unit
4.1.1	Input rise/fall time[a]		30	40	ps
4.1.2	Differential Input Voltage	200		1200	mV
4.1.3	Differential Input return loss				
	(DC to 5 GHz)		-16		dB
	(5GHz $<$f $>$10GHz)		$-14+13.33\log_{10}(f/5/5)$		dB
	(10 GHz to 20 GHz)		-3		dB
4.2.1	Power Supply Rejection Ratio[b]	50			dB
4.2.2	Control Pin V_{low}	-0.5	0	0.6	V
4.2.3	Control Pin V_{high}	1.0	1.2	1.4	V
4.3.1	Output bias current	0		15	mA
4.3.2	Output bias step size	95	100	105	µA
4.3.3	Output bias zero offset	0		100	µA
4.3.4	Output voltage[c]	Vdd (3.2.1) - 0.2			V
4.4.1	Output rise/fall time[a,d]		24	30	ps
4.4.2	Total Jitter[e,f]			22	ps
4.4.3	Deterministic Jitter[e,f]			8	ps
4.4.4	Laser dynamic impedance		50	100	■
4.4.5	Output modulation current[d]	0		10	mA
4.4.6	Output modulation step size[d]	95	100	105	µA
4.4.7	Output modulation zero offset[d]	0		100	µA
4.4.8	Output Eye Mask[g]		Fig.5		

[a] 20-80%
[b] In frequency range 1 kHz to 10 MHz.
[c] At nominal supply voltage 1V2 and 2V5.
Implies a voltage headroom for the bias output of minimum 200 mV.
[d] Measured with OMA test pattern (Alternating 1’s and 0’s at 1/8 of the target bit rate of 10 Gb/s).
[e] at BER = 1×10^{-12}.
[f] Measured with PRBS7 test pattern.
[g] Measured with PRBS23 test pattern.

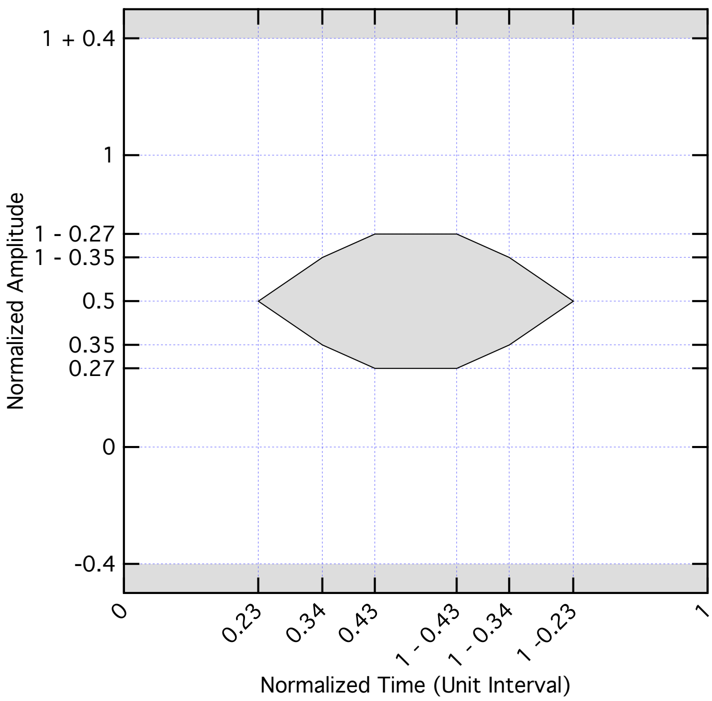

Figure 5: VL+ Quad Laser Driver Output mask.

5 Environmental Specifications

Table 6: VTRx+ module environmental specifications.

#	Specification	Min.	Typ.	Max.	Unit
5.1.1	Total Ionising Dose			1	MGy
5.1.2	Total Neutron Fluence[a]			1×10^{15}	cm^{-2}
5.1.3	Total Hadron Fluence[a]			1×10^{15}	cm^{-2}
5.1.4	SEU cross-section			TBD[b]	cm^2
5.2.1	Operating Temperature[c]	-35		+60	℃
5.3.1	Magnetic Field			4	T

[a] The radiation qualification will be carried out in a beam facility providing neutrons with a mean energy of 20 MeV, where both of the above total fluence conditions are simulated by exposure to 3×10^{15} neutrons/cm^2 (TBC).

[b] The figure of merit here would be that the SEU rate should be significantly less than one upset per day in the worst case HL-LHC Tracker radiation environment.

[c] Ambient temperature.

6 Configuration

At power-up the quad LDD is configured with default driver settings which allows the device to be fully operational. However, the user can change these settings by programming the chip through its I2C-compatible control interface. The 7-bit slave address of the chip is composed of two fields. The most significant five bits (A6..A2) are hard-wired to "10100", while the least significant two bits (A1 and A0) can be set by the user. Therefore, valid slave addresses range from 0x50 to 0x53. The user-selectable address pins have internal pull-downs, thus the default slave address is 0x50 when the address pins are left unconnected.

6.1 Initial Power-Up

At power-up, all internal memory elements are reset (including the I^2C interface logic). The power-up default states of all the registers are set according to Table 7.
The on-chip Power-on-Reset (POR) circuit holds the device in reset until the supply voltage (VDD-1.2V) is high enough to deactivate the POR circuit (i.e., release the device from reset). The reset is kept active by the POR circuit at least for 100 µs. The power on reset time depends on the rise time of the power supply line. If the power supply ramps slowly, the reset time may be longer to ensure proper reset. When the device exits the POR condition (releases reset), the digital part of the device is operational. This is not necessarily true for the analog part.

6.2 Reset behaviour

The $\overline{\text{RST}}$ (RSTN) input has the same impact on the circuit as the internally generated POR signal. An active RSTN signal (low level) voids any I^2C transaction and brings all registers to the default values.

6.3 I^2C interface

The I^2C-bus provides 2-way, 2-line communication between different ICs or modules. It supports *Slave* configuration with the *General Call* address optional feature. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Please note that there are pull-up resistors in the quad LDD pads, however their values are 40 k■, which may be too much for systems in which the net capacitance is high. Data transfer may be initiated only when the bus is not busy. During a multibyte access, when the address pointer reaches the end of the register space (0xFF) it wraps around to location 0x00.

Start and stop conditions

Both data (SDA) and clock (SCL) lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH is defined as the stop condition (P) (see Figure 6).

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Figure 8). The acknowledge bit is a HIGH level put on the bus by the transmitter (master) while generating an extra acknowledge related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the

slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.
A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Write operation

A write to the quad LDD starts with the master issuing the START condition and transmitting the quad LDD slave address with the $R\overline{W}$ bit set low.
After the quad LDD acknowledges the slave address and write bit, the master transmits a register address, which sets the internal address pointer. The master may then transmit zero or more bytes of data, with the quad LDD acknowledging each byte received. The internal address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write. An example transaction is depicted on Figure 9. One can use the multi register write operation to configure the whole chip in one I^2C transaction.

Read operation

A read from the quad LDD starts with the master issuing the START condition and transmitting the quad LDD slave address with the $R\overline{W}$ bit set high. The quad LDD acknowledges the slave address. Typically, the master reads one or more bytes from the quad LDD, each byte being acknowledged by the master upon reception with the exception of the last byte. After all registers are read, the master issues a STOP condition. An example transaction is depicted in Figure 10. One can use the multi register read operation to read back the whole chip configuration in one I^2C transaction.
After every stop condition, the chip will start a new readout from address 0x00. In order to read from an arbitrary register, a additional write sequence is necessary to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the quad LDD, the master must generate another start condition. The master now initiates a current address read by sending a device address with the $R\overline{W}$ select bit high. The quad LDD acknowledges the device address and serially clocks out the data (may be more than one word). Once the master does not want to read more data it does not acknowledge the last word and it generates the STOP condition. An example transaction is depicted in Figure 11.

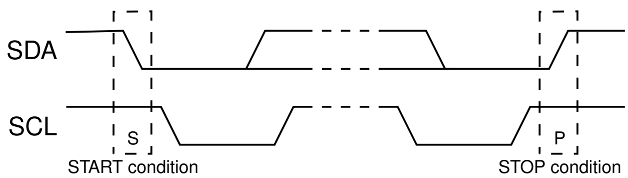

Figure 6: I^2C Definition of start and stop conditions.

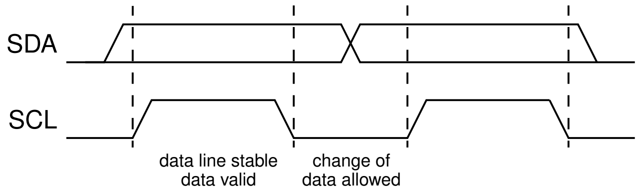

Figure 7: I^{2}C Bit transfer.

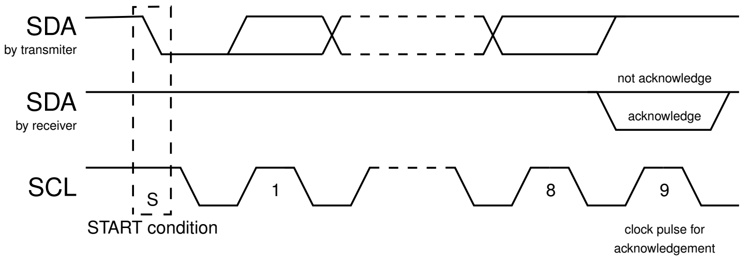

Figure 8: Acknowledgment on the I^{2}C bus.

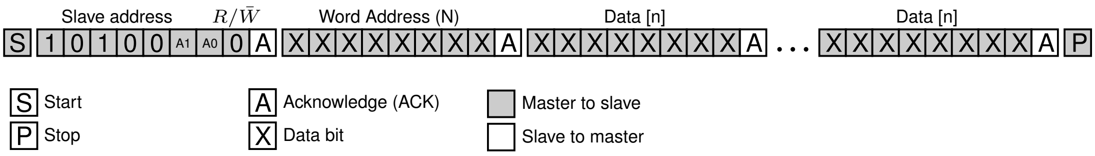

Figure 9: I^{2}C Data write.

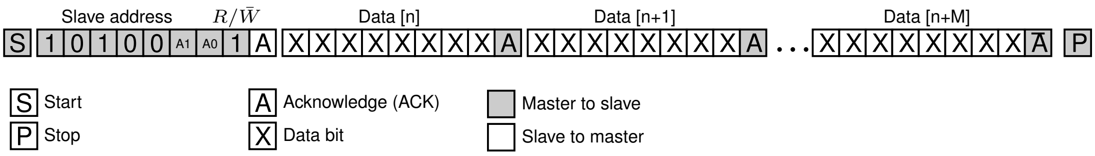

Figure 10: I^{2}C Data read from current pointer location.

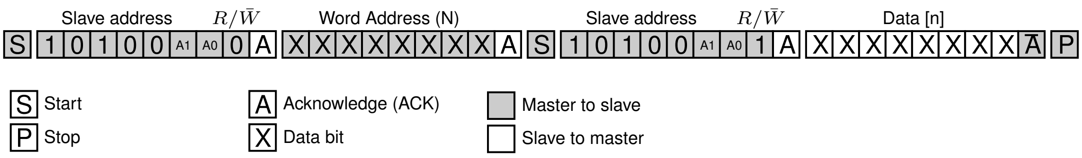

Figure 11: I^{2}C Data read from an arbitrary location.

Table 7: Register map.

NAME	**ADDR**	**MODE**	**DEF.**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GCR	0x00	R/W	0x01					CH4EN	CH3EN	CH2EN	CH1EN
reserved	0x01	R/W	0x00								
SDACNT	0x02	R/W	0x01							DRVSDA	SDADS
CH1BIAS	0x03	R/W	0x30		CH1BIAS[6:0]						
CH1MOD	0x04	R/W	0xA0	CH1MODEN	CH1MOD[6:0]						
CH1EMP	0x05	R/W	0x00				CH1EMPF	CH1EMPR	CH1EMPA[2:0]		
CH2BIAS	0x06	R/W	0x30		CH2BIAS[6:0]						
CH2MOD	0x07	R/W	0xA0	CH2MODEN	CH2MOD[6:0]						
CH2EMP	0x08	R/W	0x00				CH2EMPF	CH2EMPR	CH2EMPA[2:0]		
CH3BIAS	0x09	R/W	0x30		CH3BIAS[6:0]						
CH3MOD	0x0A	R/W	0xA0	CH3MODEN	CH3MOD[6:0]						
CH3EMP	0x0B	R/W	0x00				CH3EMPF	CH3EMPR	CH3EMPA[2:0]		
CH4BIAS	0x0C	R/W	0x30		CH4BIAS[6:0]						
CH4MOD	0x0D	R/W	0xA0	CH4MODEN	CH4MOD[6:0]						
CH4EMP	0x0E	R/W	0x00				CH4EMPF	CH4EMPR	CH4EMPA[2:0]		
reserved	0x0F	R/W	0x00								
reserved	0x10	R/W	0x00								
reserved	0x11	R/W	0x07								
reserved	0x12	R/W	0x00								
reserved	0x13	R/W	0x00								
STATUS	0x14	R	–					DIS	PORC	PORB	PORA
ID	0x15	R	–	CHIPID[3:0] = 0x1				REVID[3:0] = 0x5			
UID0	0x16	R	–	UID[7:0]							
UID1	0x17	R	–	UID[15:8]							
UID2	0x18	R	–	UID[23:16]							
UID3	0x19	R	–	UID[31:24]							
SEU0	0x1A	R/CLR	–	SEUCNT[7:0]							
SEU1	0x1B	R/CLR	–	SEUCNT[15:8]							
SEU2	0x1C	R/CLR	–	SEUCNT[23:16]							
SEU3	0x1D	R/CLR	–	SEUCNT[31:24]							

6.4 Register Descriptions

Detailed descriptions of register functionalities are given below, where x represents one of the four LDD channels 1, 2, 3 or 4.
To ensure correct chip operation, no register named ”reserved” should not be changed to anything but the default value.

Global Control Register (GCR) – Address 0x00

7	6	5	4	3	2	1	0
– r/w	– r/w	– r/w	– r/w	CH4EN r/w	CH3EN r/w	CH2EN r/w	CH1EN r/w

Bit	Name	Default	Description
0	CH1EN	1	Channel 1 Enable.
1	CH2EN	0	Channel 2 Enable.
2	CH3EN	0	Channel 3 Enable.
3	CH4EN	0	Channel 4 Enable.
7:4	–	0x0	unused

Note that it is not possible to completely turn off any given channel, there will always be a bias current corresponding to 1 LSB flowing in the output of the LDQ10. This is to ensure chip reliability.

SDA Control Register (ODC) – Address 0x02

7	6	5	4	3	2	1	0
– r/w	– r/w	– r/w	– r/w	– r/w	– r/w	DRVSDA r/w	SDADS r/w

Bit	Name	Default	Description
0	SDADS	1	SDA Driving Strength (0-low, 1-high). Could be lowered to try to reduce rise times and their associated EMI.
1	DRVSDA	0	Drive SDA. Do not change unless advised to do so by the support team.
7:2	–	0x0	unused

Channel x Bias Current Register (CHxBIAS) – Address 0x03/0x06/0x09/0x0C

7	6	5	4	3	2	1	0
– r/w	CHxBIAS[6:0] r/w						

Bit	Name	Default	Description
6:0	CHxBias	0x30	Biasing current step size is given in specification # 4.3.2. Note that setting 0 and 1 are functionally equivalent and correspond to 1 unit of the bias current step. The bias generator is enabled by setting the corresponding channel enable bit in the GCR.
7	–	0	unused

Channel x Modulation Current Register (CHxMOD) – Address 0x04/0x07/0x0A/0x0D

7	6	5	4	3	2	1	0
CHxMODEN r/w	CHxMOD[6:0] r/w						

Bit	Name	Default	Description
6:0	CHxMOD	0x20	Modulation current step size is given in specification # 4.4.6.
7	CHxMODEN	1	Modulation current generator enable.

Channel x Emphasis Amplitude Register (CHxEMP) – Address 0x05/0x08/0x0B/0x0E

7	6	5	4	3	2	1	0
– r/w	– r/w	– r/w	CHxEMPF r/w	CHxEMPR r/w	CHxEMPAMP[2:0] r/w		

Bit	Name	Default	Description
2:0	CHxEMPAMP	0	Pre-emphasis amplitude.
3	CHxEMPR	0	Rising edge pre-emphasis enable.
4	CHxEMPF	0	Falling edge pre-emphasis enable.
7:5	–	0	unused

Status register (STATUS) – Address 0x14

7	6	5	4	3	2	1	0
– r/w	– r/w	– r/w	– r/w	DIS r/w	PORC r/w	PORB r/w	PORA r/w

Bit	Name	Default	Description
0	PORA	–	Power-on Reset A.
1	PORB	–	Power-on Reset B.
2	PORC	–	Power-on Reset C.
3	DIS	–	Mirror of external DIS input state.
7:4	–	–	reserved

ID register (ID) – Address 0x15

7	6	5	4	3	2	1	0
CHIPID[3:0] r				REVID[3:0] r			

Bit	Name	Default	Description
3:0	REVID	–	Chip revision number (production version is 5)
7:4	CHIPID	–	Chip type (LDQ10 is 1)

Unique ID registers (UID0:3) – Addresses 0x16 to 0x19

7	6	5	4	3	2	1	0
UIDy[7:0] r							

Bit	Name	Default	Description
7:0	UIDy	–	The four registers yield a unique 32-bit chip ID that is set during production testing to allow traceability of chip and module.

SEU counter registers (SEU0:3) – Addresses 0x1A to 0x1D

7	6	5	4	3	2	1	0
SEUy[7:0] r/clr							

Bit	Name	Default	Description
7:0	SEUy	–	The four registers yield the contents of the SEU counter. Writing any value to any of the four registers clears the counter.

7 Tolerance to single event upsets

For correct laser driver operation, it is important that the behaviour of the chip (the contents of the configuration registers in particular) will not be upset by single event effects. To avoid malfunction, the digital block uses Triple Modular Redundancy (TMR).