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Configuring HPS2 SC Bits

Description of HPS slow control registers and their addressing. Meaning of control bits, and their programming for operation on FEB2.

1. HPS2 SC architecture

Slow control (SC) registers of HPS have the same architecture and the same I2C slave circuit as ALFE, but usage of control bits is different. HPS is configured with 15 SC registers, 8-bit each. Each SC register is filled with writing to 3 intermediate on-chip registers called R0, R1 and R2, i.e. by generating sequence of 3 I2C frames which are explained in Fig. 1.

Figure 1: *I2C sequence to write one SC register.*

Chip ID is determined by connections of 4 HPS address pins to ground or to 1.2V. If those 4 pins are floating, the default address is 1010 (there are internal pull-up and pull-down resistors). In this case addresses of R0-R2 are 1010000 = 80, 1010001 = 81, and 1010010 = 82. Data byte of R0 is SC register address (0…14); data byte of R1 is always 0; data byte of R2 is content of corresponding SC register. In total 15x3 = 45 I2C transactions required to fill all 15 SC registers.

2. Bits assignment

HPS SC bits are listed in Tab. 1; shown in the Tab is the net names, as used in the HPS schematics and chip layout. Bits marked "x" are not used, their content is not important, in further examples I set them to 0. Blue font denotes bits connecting/disconnecting dedicated HPS pins to corresponding points of the circuit. This is used during QC test to measure voltages at those points, in normal operation these bits must be 0. Green text indicates bits enabling/disabling opamp or a group of opamps. In normal operation these bits are set to 1.

Table 1: *Usage of HPS SC bits.0 – least significant, 7- most significant bit.*

SC register	7	6	5	4	3	2	1	0	Comment
0	en_probe_vcm	ON_g10	ON_ref_bg	ON_pa	ON_lg_s1	ON_hg_s1	ON_lg_s2	ON_hg_s2	Opamps
1	x	x	dac_g10<0>	dac_g10<1>	dac_g10<2>	dac_g10<3>	dac_g10<4>	dac_g10<5>	G20
2	cr_hg_s1<2>	cr_hg_s1<1>	cr_hg_s1<0>	x	rc_hg_s1<3>	rc_hg_s1<2>	rc_hg_s1<1>	rc_hg_s1<0>	SH HG T1
3	rc_hg_s2<3>	rc_hg_s2<2>	rc_hg_s2<1>	rc_hg_s2<0>	rc_lg_s2<3>	rc_lg_s2<2>	rc_lg_s2<1>	rc_lg_s2<0>	SH T2
4	cr_lg_s1<2>	cr_lg_s1<1>	cr_lg_s1<0>	x	rc_lg_s1<3>	rc_lg_s1<2>	rc_lg_s1<1>	rc_lg_s1<0>	SH LG T1
5	x	x	ON_ref_sum	en_sum<4>	en_sum<3>	en_sum<2>	en_sum<1>	ON_sum	TS
6	dac_VDC_hg<5>	dac_VDC_hg<4>	dac_VDC_hg<3>	dac_VDC_hg<2>	dac_VDC_hg<1>	dac_VDC_hg<0>	ON_ch	gain	CH1
7	dac_VDC_lg<5>	dac_VDC_lg<4>	dac_VDC_lg<3>	dac_VDC_lg<2>	dac_VDC_lg<1>	dac_VDC_lg<0>	probe_g10	input_res	
8	dac_VDC_hg<5>	dac_VDC_hg<4>	dac_VDC_hg<3>	dac_VDC_hg<2>	dac_VDC_hg<1>	dac_VDC_hg<0>	ON_ch	gain	CH2
9	dac_VDC_lg<5>	dac_VDC_lg<4>	dac_VDC_lg<3>	dac_VDC_lg<2>	dac_VDC_lg<1>	dac_VDC_lg<0>	probe_g10	input_res	
10	dac_VDC_hg<5>	dac_VDC_hg<4>	dac_VDC_hg<3>	dac_VDC_hg<2>	dac_VDC_hg<1>	dac_VDC_hg<0>	ON_ch	gain	CH3
11	dac_VDC_lg<5>	dac_VDC_lg<4>	dac_VDC_lg<3>	dac_VDC_lg<2>	dac_VDC_lg<1>	dac_VDC_lg<0>	probe_g10	input_res	
12	dac_VDC_hg<5>	dac_VDC_hg<4>	dac_VDC_hg<3>	dac_VDC_hg<2>	dac_VDC_hg<1>	dac_VDC_hg<0>	ON_ch	gain	CH4
13	dac_VDC_lg<5>	dac_VDC_lg<4>	dac_VDC_lg<3>	dac_VDC_lg<2>	dac_VDC_lg<1>	dac_VDC_lg<0>	probe_g10	input_res	
14	cmd_gain_sum	x	dac_VDC_sum<5>	dac_VDC_sum<4>	dac_VDC_sum<3>	dac_VDC_sum<2>	dac_VDC_sum<1>	dac_VDC_sum<0>	TS

Brown text shows bits configuring preshaper (PS) gain ("gain") and connections of HPS channels to trigger sum (TS) ("en_sum<CH#>"). These bits are identical for all 32 ASICs of FEB2 and defined by FEB2 routing, i.e. connection of HEC longitudinal segments (LS) to ASIC channels. PS has two gain modes: G1 (used for HEC LS 1, 2), and G2 (used for LS 3, 4). To form trigger, LS4 is not used because it adds very low signal). Tab. 2 shows example in case if FEB2 is routed as the top layer of the present FEB. Another fixed bit is "*cmd_gain_sum*", this is gain of TS circuit, either gain-1 (bit = 1) or gain-3 (bit = 0). It is defined by location of chip at one of FEB2 in the HEC FE crate. Gain-3 is configured for low-eta region (FEB-1,2) and gain-1 is used for high-eta region (FEB-3,4,5,6). Exact boundary between gain-1 and gain-3 to be set as it is in the present HEC readout.

Table 2: *PS gain and TS connection.*

HPS ch.	HEC LS	PS gain	"gain"	"en_sum"
CH1	LS4	G2	1	0
CH2	LS3	G2	1	1
CH3	LS2	G1	0	1
CH4	LS1	G1	0	1

All other bits (black font) are to configure HPS characteristics, their values vary from chip to chip and determined in QC test. This is shown in Tab. 3 where these bits are marked as "C". As a result, two registers, #0 and #5 are the same for all ASICs, other registers are individual for each chip.

Table 3: *Content of SC registers.*

SC register	7	6	5	4	3	2	1	0	Decimal
0	0	1	1	1	1	1	1	1	127
1	0	0	C	C	C	C	C	C	C
2	C	C	C	0	C	C	C	C	C
3	C	C	C	C	C	C	C	C	C
4	C	C	C	0	C	C	C	C	C
5	0	0	1	1	1	1	0	1	61
6	C	C	C	C	C	C	1	1	C
7	C	C	C	C	C	C	0	C	C
8	C	C	C	C	C	C	1	1	C
9	C	C	C	C	C	C	0	C	C
10	C	C	C	C	C	C	1	0	C
11	C	C	C	C	C	C	0	C	C
12	C	C	C	C	C	C	1	0	C
13	C	C	C	C	C	C	0	C	C
14	C	0	C	C	C	C	C	C	C

Optimal configuration of each ASIC is based on measurements in QC test. These measurements include:

1. DAC scan of *G10* amplifier (another name is *G20*), the additional amplifier with gain 17-22 included in the high-gain branch of the shaper. This DAC adjusts DC point at *G20* output (desired value ~1V). Optimal DAC code is the content of SC register #1.
2. Registers #2-4 configure shaper time constants, 3 constants of $CR\text{-}RC^2$ (3 bits for *CR*, 4 bits for *RC* stage-1 and 4 bits for *RC* stage 2) are common to 4 channels, but different for low gain (bits …*_lg_*...) and high gain (bits …*_hg_*...) branches. These values are determined from corresponding scans.
3. Registers #6,7 contain 6 bits of DAC shifting baselines of CH1 low-gain output (bits …*lg*…) and high-gain output (bits …*hg*…). They are determined from DAC scans; optimal value provides 0.6V difference between negative and positive outputs. The least significant bit of register #7 controls input impedance of the channel, in preproduction batch *input_res* = 1 for all channels of all ASICs.
4. Registers #8,9; #10,11; #12,13 are the same but for HPS CH2, CH3, CH4 respectively.
5. The last register #14 contains 6 bits of DAC, shifting baseline of TS output. Its value is found from corresponding scan; the value depends on TS gain (bit-7 of this register) and on the number of HPS channels connected to the summing circuit. These values are available for both gains and for 2, 3, 4 channels connected.

3. SC data files

One of QC output is a file *Bnnnn.txt* (one per chip, *nnnn* being chip number as labelled on the package) with 6 SC configurations (two TS gains and 3 TS connections). This file can not be used directly for FEB2 configuration because it is generated for different conditions:

1. All probes are enabled.
2. PS in G1 mode for all channels.

Configuration file for the chip on FEB2 *BFnnnn.txt* is generated from that QC file leaving 2 configurations – with TS gain-1 (column 1) and TS gain-3 (column 2), with 3 HPS channels connected to TS. Each column is 15 numbers representing decimal code of 15 SC registers. One of these two configurations to be used depending on FEB position in FE crate. Screenshot of BF file is shown in Fig. 2.

The file is created with MLAB script *SCfeb.m* which reads B-file, takes column 2 (TS gain-1 with 3 channels) and column 5 (gain-3 with 3 channels), then go through 15 SC registers making recalculations:

1. SC0 changed to 127
2. SC1-4 unchanged
3. SC5 changed to 61
4. SC6,8 add 1 (switch to PS G2 mode)
5. SC7,9,11,13 subtract 2 (disable probe of G20 output)
6. SC10,12 unchanged (PS is already in G1 mode)
7. SC14 unchanged (TS gain is already fixed to right value in each column)

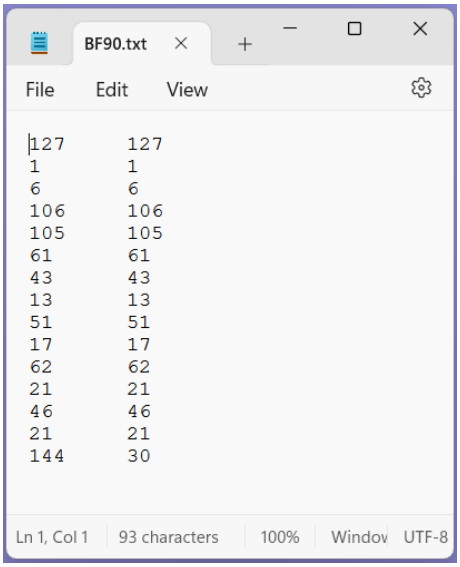

Figure 2: *Example of configuration file.*