ALFE2 datasheet

Revisions

Revision number	Key changes	Drafted by	Revision date
0.22	Added package mark	T. Liu	10/30/2022
0.21	Added bias network	T. Liu	10/23/2022
0.2	Added pinout and I2C interface	T. Liu	10/14/2022
0.1	Initial draft	D. Matakias	4/20/2022

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1. Description

ALFE2 is a 4-channel low-noise analog front-end ASIC designed for the readout of the Liquid Argon Calorimeter in the ATLAS detector on the HL-LHC. ALFE2 comprises four front-end (FE) channels. Each channel contains a Pre-Amplifier (PA) and a CR-$(RC)^2$ shaper (SH). Each shaper has two separate gain paths, Low Gain (LG) and High Gain (HG). Two different gains can be simultaneously read out to provide full dynamic-range coverage and the optimum resolution for small signals. ALFE2 includes a Trigger Sum (TS) output. The TS output has a CR-RC shaper stage with configurable gain and channel switch. Each output of ALFE2 is digitized by an ADC at a sampling rate of 40 MSPS for continuous readout. ALFE2 integrates a band-gap reference (BGR) voltage and a DAC to generate bias voltages for the preamplifiers and shapers without any external current sources. ALFE2 implements an I^2C target block for slow control and configuration.

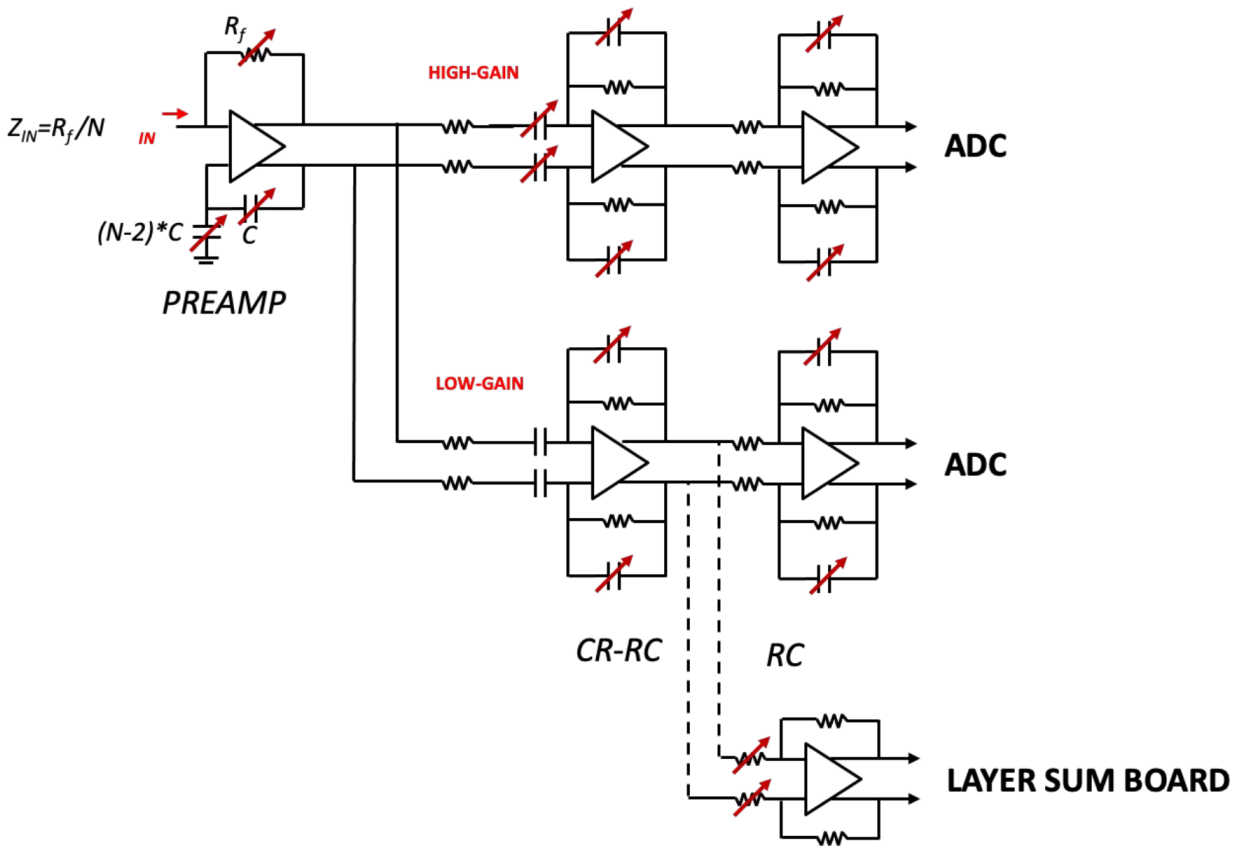

Figure 1: Functional block diagram of ALFE2.

2. Package and pinout

2.1 Package

ALFE2 is packaged in a Ball Grid Array (BGA) package. Each chip has 14×14 balls with a pitch of 0.80 mm. The package size is 12 mm×12 mm×1.473 mm (height). The mechanical drawing of the BGA package is shown in Figure 2. Photographs of packaged chips are shown in Figure 3. The top left of Figure 3 is the top view of a chip. The top right of Figure 3 is the bottom view. The bottom of Figure 3 is a tray with 72 chips.

A QR code and three text lines are etched on the top surface of each chip. The nominal and maximum etching depths are 10 µm and 20 µm, respectively. The QR code occupies an 8 mm×8 mm area. The QR code (Version 1) has 21×21 modules with a Q redundancy of 25%. The text lines contain the following information:

- The first line is ALFE2 YYWW, where ALFE2 is the ASIC name and YYWW is the date code. YY and WW represent the year 20YY and the week index of the year when the chip is packaged.
- The second line is BNL/IN2P3, the institutes of ASIC developers.
- The last line is the serial number. The serial number is composed of a lot number from 001 to 999 and a serial number in the lot from 00001 to 99999. The lot number and the serial number in the lot are separated with a hyphen.

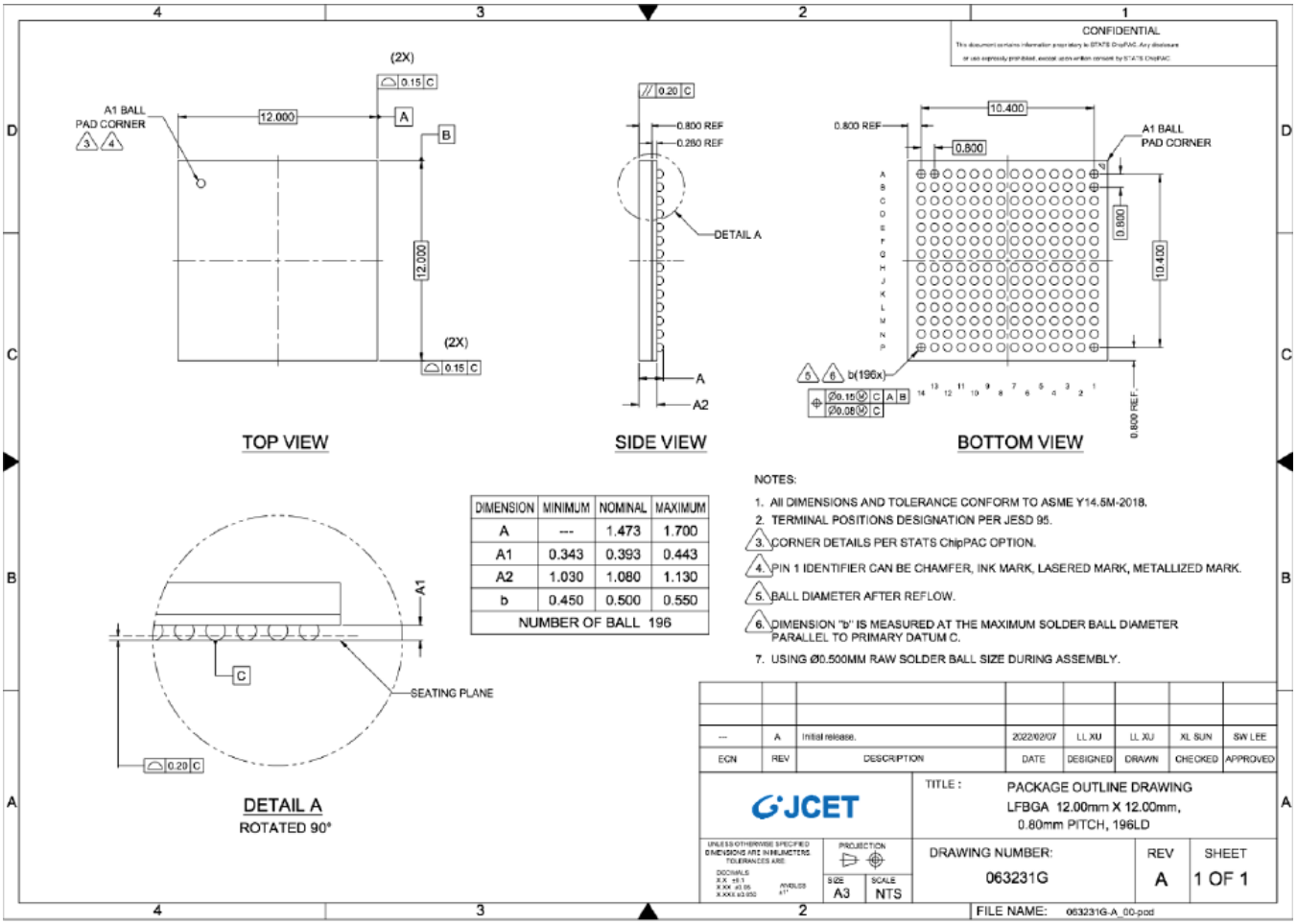

Figure 2. Mechanical drawing of the BGA package of ALFE2.

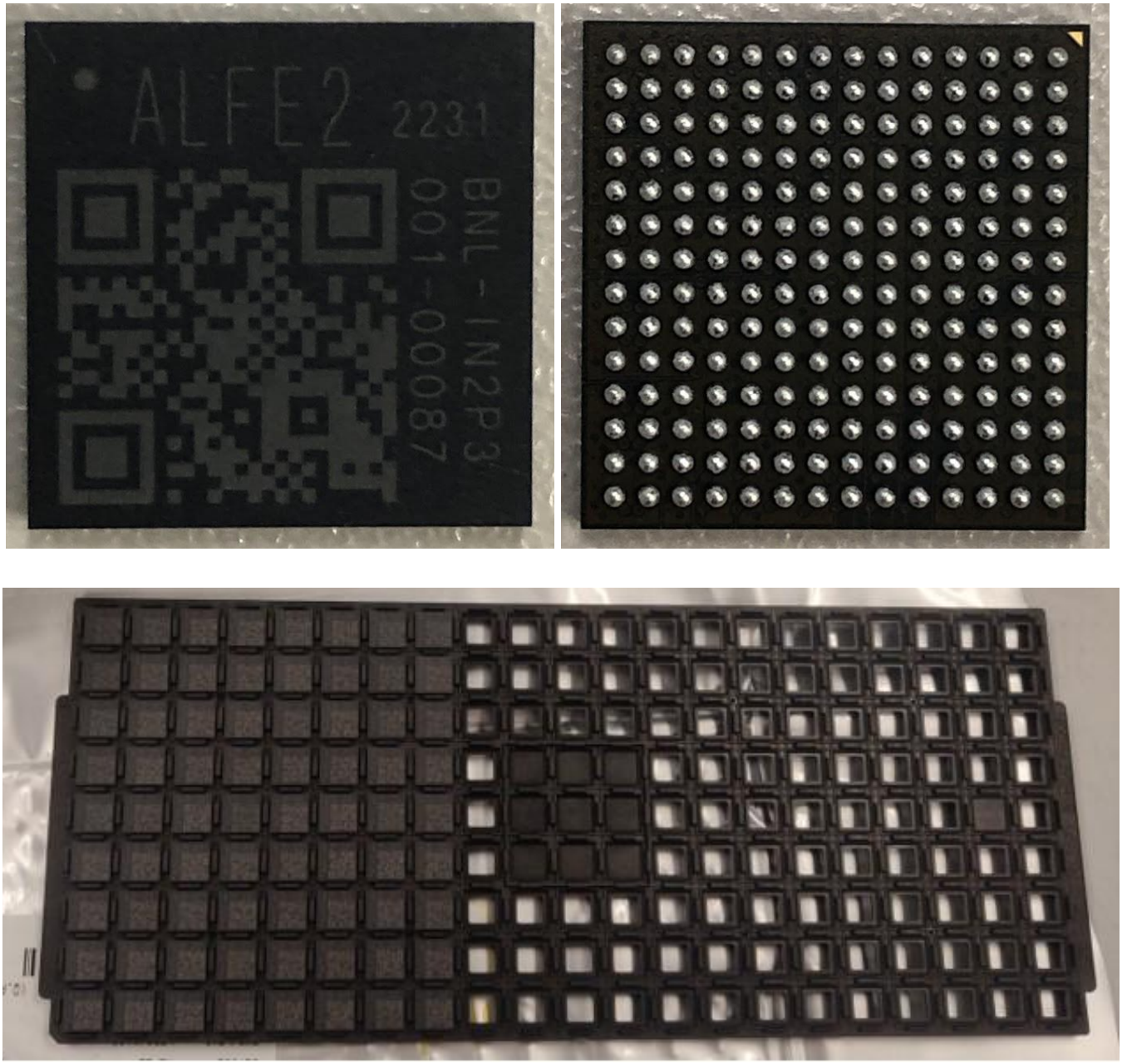

Figure 3. Photographs of packaged ALFE2 chips. The top left is the top view of a chip. The top right is the bottom view. The bottom is a tray with 72 chips.

2.2 Pinout (top view, balls down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS_GND	N1MA2P5_PA<0>	VB_FC_PA<0>	VB_FC_SH	N5UA_SH<0>	N1UA_SH<0>	I2C_RSTB	CK40_P	CK40_N	I2C_SDA	I2C_SCL	I2C_En	VSS_GND	VSS_GND	A
B	IN<0>	VSS_GND	VCM_PA	VB_IB_SH	N5UA_SH<1>	N1UA_SH<1>	I2C_ERROR	VB_CMFB_SH	VB_NAB_SH	VDD1P2_SH_LG	VDD1P2_SH_LG	VSS_GND	OUTP_LG<0>	OUTN_LG<0>	B
C	IN<0>	VSS_GND	VDD1P2_PA	N1MA2P5_PA<1>	VB_FC_PA<1>	vb_fb0_idcp_pa	n1mAi_sh	VB_PAB_SH	VSS_GND	VDD1P2_SH_HG<0>	VDD1P2_SH_HG<0>	VSS_GND	OUTP_HG<0>	OUTN_HG<0>	C
D	VSS_GND	VDD1P2_PA	VDD1P2_PA	VSS_GND	VDD2P5_ESD_TOP	VDD2P5_PA	VB_IT_SH	VDD1P2_DAC	VDD1P2_I2C	VSS_GND	VSS_GND	vcm_sh	VSS_GND	VSS_GND	D
E	IN<1>	VSS_GND	VDD1P2_PA	p1mAi_2p5_pa	PA_ESD	VDD2P5_PA	VSS_GND	VDD1P2_DAC	VDD1P2_I2C	VDD1P2_SH_HG<1>	VDD1P2_SH_HG<1>	VSS_GND	OUTP_HG<1>	OUTN_HG<1>	E
F	IN<1>	VSS_GND	VDD1P2_PA	VDD1P2_PA	VSS_GND	VDD2P5_PA	VSS_GND	p5uA_sh<1>	p5uA_sh<0>	VDD1P2_SH_LG	VDD1P2_SH_LG	VSS_GND	OUTP_LG<1>	OUTN_LG<1>	F
G	VSS_GND	n1mA2p5_pa<0>	vb_it_pa	VDD1P2_PA	VSS_GND	VDD2P5_PA	VSS_GND	VSS_GND	p10uA_sh<1>	p10uA_sh<0>	VDD1P2_SH_TS	VDD1P2_SH_TS	VSS_GND	VSS_GND	G
H	VSS_GND	vb_ib_pa	n1mAi_pa	VDD1P2_PA	VSS_GND	VDD2P5_PA	VSS_GND	p1uA_sh<1>	p1uA_sh<0>	VDD1P2_SH_LG	VDD1P2_SH_LG	VSS_GND	OUTP_LG<2>	OUTN_LG<2>	H
J	IN<2>	VSS_GND	VDD1P2_PA	VDD1P2_PA	VSS_GND	VDD2P5_PA	VSS_GND	VSS_GND	VSS_GND	VDD1P2_SH_HG<2>	VDD1P2_SH_HG<2>	VSS_GND	OUTP_HG<2>	OUTN_HG<2>	J
K	IN<2>	VSS_GND	VDD1P2_PA	VSS_GND	PA_ESD	VDD2P5_PA	SH_ESD	VSS_GND	VSS_GND	VSS_GND	VSS_GND	ext_vref_dac	VSS_GND	VSS_GND	K
L	VSS_GND	VDD1P2_PA	VDD1P2_PA	VSS_GND	VDD2P5_ESD_BOT	VDD2P5_PA	SH_ESD	VSS_GND	VSS_GND	VDD1P2_SH_HG<3>		VSS_GND	OUTP_HG<3>	OUTN_HG<3>	L
M	IN<3>	VSS_GND	VDD1P2_PA	N1MA2P5_PA<1>	vb_fb0_idcp_pa	VSS_GND	VSS_GND	N5UA_SH<0>	N1UA_SH<0>	VDD1P2_SH_LG	VDD1P2_SH_LG	VSS_GND	OUTP_LG<3>	OUTN_LG<3>	M
N	IN<3>	VSS_GND	VDD1P2_PA	VCM_PA	VB_IB_SH	VB_FC_SH	VB_NAB_SH	VB_PAB_SH	P5UA_SH<0>	VCM_SH	I2C_ADDR<2>	I2C_ADDR<3>	VSS_GND	VSS_GND	N
P	VSS_GND	N1MA2P5_PA<0>	VB_FC_PA<1>	VB_FC_PA<0>	VB_CMFB_SH	N10UA_SH<1>	N10UA_SH<0>	VB_IT_SH	P1UA_SH<0>	I2C_ADDR<0>	I2C_ADDR<1>	VSS_GND	OUTP_SUM	OUTN_SUM	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4. ALFE2 pinout (top view, balls down).

2.3 Pin list (by pin position)

Table 1. Pin list (by pin position)

Ball pos	Pin name	Type	Description
A1	VSS_GND	Power	ground
A2	N1MA2P5_PA<0>	Power	external bias current
A3	VB_FC_PA<0>	Power	external bias voltage
A4	VB_FC_SH	Power	external bias voltage
A5	N5UA_SH<0>	Power	external bias current
A6	N1UA_SH<0>	Power	external bias current
A7	I2C_RSTB	Digital input	I2C reset, active low
A8	CK40_P	Digital input	I2C clock input, positive
A9	CK40_N	Digital input	I2C clock input, negative
A10	I2C_SDA	Digital I/O	I2C data, open drain
A11	I2C_SCL	Digital input	I2C clock
A12	I2C_En	Digital input	Not connected

A13	VSS_GND	Power	ground
A14	VSS_GND	Power	ground
B1	IN<0>	Analog input	analog input channel 0
B2	VSS_GND	Power	ground
B3	VCM_PA	Power	external bias voltage
B4	VB_IB_SH	Power	external bias voltage
B5	N5UA_SH<1>	Power	external bias current
B6	N1UA_SH<1>	Power	external bias current
B7	I2C_ERROR	Digital output	I2C error state
B8	VB_CMFB_SH	Power	external bias voltage
B9	VB_NAB_SH	Power	external bias voltage
B10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
B11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
B12	VSS_GND	Power	ground
B13	OUTP_LG<0>	Analog output	Analog output, low gain, channel 0, positive
B14	OUTN_LG<0>	Analog output	Analog output, low gain, channel 0, negative
C1	IN<0>	Analog input	analog input channel 0
C2	VSS_GND	Power	ground
C3	VDD1P2_PA	Power	Power, 1.2 V, PA
C4	N1MA2P5_PA<1>	Power	external bias current
C5	VB_FC_PA<1>	Power	external bias voltage
C6	vb_fb0_idcp_pa	Power	external bias voltage
C7	n1mAi_sh	Power	external bias current
C8	VB_PAB_SH	Power	external bias voltage
C9	VSS_GND	Power	ground
C10	VDD1P2_SH_HG<0>	Power	Power, 1.2 V, shaper, high gain, channel 0
C11	VDD1P2_SH_HG<0>	Power	Power, 1.2 V, shaper, high gain, channel 0
C12	VSS_GND	Power	ground
C13	OUTP_HG<0>	Analog output	Analog output, high gain, channel 0, positive
C14	OUTN_HG<0>	Analog output	Analog output, high gain, channel 0, negative
D1	VSS_GND	Power	ground
D2	VDD1P2_PA	Power	Power, 1.2 V, PA
D3	VDD1P2_PA	Power	Power, 1.2 V, PA
D4	VSS_GND	Power	ground
D5	VDD2P5_ESD_TOP	Power	Power, 2.5 V, ESD, bottom
D6	VDD2P5_PA	Power	Power, 2.5 V, PA
D7	VB_IT_SH	Power	external bias voltage
D8	VDD1P2_DAC	Power	Power 1.2 V, DAC
D9	VDD1P2_I2C	Power	Power, 1.2 V, I2C

D10	VSS_GND	Power	ground
D11	VSS_GND	Power	ground
D12	vcm_sh	Power	external bias voltage
D13	VSS_GND	Power	ground
D14	VSS_GND	Power	ground
E1	IN<1>	Analog input	analog input channel 1
E2	VSS_GND	Power	ground
E3	VDD1P2_PA	Power	Power, 1.2 V, PA
E4	p1mAi_2p5_pa	Power	external bias current
E5	PA_ESD	Power	Power ESD, PA
E6	VDD2P5_PA	Power	Power, 2.5 V, PA
E7	VSS_GND	Power	ground
E8	VDD1P2_DAC	Power	Power, 1.2 V, DAC
E9	VDD1P2_I2C	Power	Power, 1.2 V, I2C
E10	VDD1P2_SH_HG<1>	Power	Power, 1.2 V, shaper, high gain, channel 1
E11	VDD1P2_SH_HG<1>	Power	Power, 1.2 V, shaper, high gain, channel 1
E12	VSS_GND	Power	ground
E13	OUTP_HG<1>	Analog output	Analog output, high gain, channel 1, positive
E14	OUTN_HG<1>	Analog output	Analog output, high gain, channel 1, negative
F1	IN<1>	Analog input	analog input channel 1
F2	VSS_GND	Power	ground
F3	VDD1P2_PA	Power	Power, 1.2 V, PA
F4	VDD1P2_PA	Power	Power, 1.2 V, PA
F5	VSS_GND	Power	ground
F6	VDD2P5_PA	Power	Power, 2.5 V, PA
F7	VSS_GND	Power	ground
F8	p5uA_sh<1>	Power	external bias current
F9	p5uA_sh<0>	Power	external bias current
F10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
F11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
F12	VSS_GND	Power	ground
F13	OUTP_LG<1>	Analog output	Analog output, low gain, channel 1, positive
F14	OUTN_LG<1>	Analog output	Analog output, low gain, channel 1, negative
G1	VSS_GND	Power	ground
G2	n1mA2p5_pa<0>	Power	external bias current
G3	vb_it_pa	Power	external bias voltage
G4	VDD1P2_PA	Power	Power, 1.2 V, PA
G5	VSS_GND	Power	ground
G6	VDD2P5_PA	Power	Power, 2.5 V, PA

G7	VSS_GND	Power	ground
G8	VSS_GND	Power	ground
G9	p10uA_sh<1>	Power	external bias current
G10	p10uA_sh<0>	Power	external bias current
G11	VDD1P2_SH_TS	Power	Power, 1.2 V, shaper, trigger sum
G12	VDD1P2_SH_TS	Power	Power, 1.2 V, shaper, trigger sum
G13	VSS_GND	Power	ground
G14	VSS_GND	Power	ground
H1	VSS_GND	Power	ground
H2	vb_ib_pa	Power	external bias voltage
H3	n1mAi_pa	Power	external bias current
H4	VDD1P2_PA	Power	Power, 1.2 V, PA
H5	VSS_GND	Power	ground
H6	VDD2P5_PA	Power	Power, 2.5 V, PA
H7	VSS_GND	Power	ground
H8	p1uA_sh<1>	Power	external bias current
H9	p1uA_sh<0>	Power	external bias current
H10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
H11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
H12	VSS_GND	Power	ground
H13	OUTP_LG<2>	Analog output	Analog output, low gain, channel 2, positive
H14	OUTN_LG<2>	Analog output	Analog output, low gain, channel 2, negative
J1	IN<2>	Analog input	analog input channel 2
J2	VSS_GND	Power	ground
J3	VDD1P2_PA	Power	Power, 1.2 V, PA
J4	VDD1P2_PA	Power	Power, 1.2 V, PA
J5	VSS_GND	Power	ground
J6	VDD2P5_PA	Power	Power, 2.5 V, PA
J7	VSS_GND	Power	ground
J8	VSS_GND	Power	ground
J9	VSS_GND	Power	ground
J10	VDD1P2_SH_HG<2>	Power	Power, 1.2 V, shaper, high gain, channel 2
J11	VDD1P2_SH_HG<2>	Power	Power, 1.2 V, shaper, high gain, channel 2
J12	VSS_GND	Power	ground
J13	OUTP_HG<2>	Analog output	Analog output, high gain, channel 2, positive
J14	OUTN_HG<2>	Analog output	Analog output, high gain, channel 2, negative
K1	IN<2>	Analog input	analog input channel 2
K2	VSS_GND	Power	ground

K3	VDD1P2_PA	Power	Power, 1.2 V, PA
K4	VSS_GND	Power	ground
K5	PA_ESD	Power	Power ESD, PA
K6	VDD2P5_PA	Power	Power, 2.5 V, PA
K7	SH_ESD	Power	Power ESD, shaper
K8	VSS_GND	Power	ground
K9	VSS_GND	Power	ground
K10	VSS_GND	Power	ground
K11	VSS_GND	Power	ground
K12	ext_vref_dac	Power	External reference voltage
K13	VSS_GND	Power	ground
K14	VSS_GND	Power	ground
L1	VSS_GND	Power	ground
L2	VDD1P2_PA	Power	Power, 1.2 V, PA
L3	VDD1P2_PA	Power	Power, 1.2 V, PA
L4	VSS_GND	Power	ground
L5	VDD2P5_ESD_BOT	Power	Power, 2.5 V, ESD, bottom
L6	VDD2P5_PA	Power	Power, 2.5 V, PA
L7	SH_ESD	Power	Power ESD, shaper
L8	VSS_GND	Power	ground
L9	VSS_GND	Power	ground
L10	VDD1P2_SH_HG<3>	Power	Power, 1.2 V, shaper, high gain, channel 3
L11	VDD1P2_SH_HG<3>	Power	Power, 1.2 V, shaper, high gain, channel 3
L12	VSS_GND	Power	ground
L13	OUTP_HG<3>	Analog output	Analog output, high gain, channel 3, positive
L14	OUTN_HG<3>	Analog output	Analog output, high gain, channel 3, negative
M1	IN<3>	Analog input	analog input channel 3
M2	VSS_GND	Power	ground
M3	VDD1P2_PA	Power	Power, 1.2 V, PA
M4	N1MA2P5_PA<1>	Power	external bias current
M5	vb_fb0_idcp_pa	Power	external bias voltage
M6	VSS_GND	Power	ground
M7	VSS_GND	Power	ground
M8	N5UA_SH<0>	Power	external bias current
M9	N1UA_SH<0>	Power	external bias current
M10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
M11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
M12	VSS_GND	Power	ground

M13	OUTP_LG<3>	Analog output	Analog output, low gain, channel 3, positive
M14	OUTN_LG<3>	Analog output	Analog output, low gain, channel 3, negative
N1	IN<3>	Analog input	analog input channel 3
N2	VSS_GND	Power	ground
N3	VDD1P2_PA	Power	Power, 1.2 V, PA
N4	VCM_PA	Power	external bias voltage
N5	VB_IB_SH	Power	external bias voltage
N6	VB_FC_SH	Power	external bias voltage
N7	VB_NAB_SH	Power	external bias voltage
N8	VB_PAB_SH	Power	external bias voltage
N9	P5UA_SH<0>	Power	external bias current
N10	VCM_SH	Power	external bias voltage
N11	I2C_ADDR<2>	Digital input	I2C address input, bit 2
N12	I2C_ADDR<3>	Digital input	I2C address input, bit 3
N13	VSS_GND	Power	ground
N14	VSS_GND	Power	ground
P1	VSS_GND	Power	ground
P2	N1MA2P5_PA<0>	Power	external bias current
P3	VB_FC_PA<1>	Power	external bias voltage
P4	VB_FC_PA<0>	Power	external bias voltage
P5	VB_CMFB_SH	Power	external bias voltage
P6	N10UA_SH<1>	Power	external bias current
P7	N10UA_SH<0>	Power	external bias current
P8	VB_IT_SH	Power	external bias voltage
P9	P1UA_SH<0>	Power	external bias current
P10	I2C_ADDR<0>	Digital input	I2C address input, bit 0
P11	I2C_ADDR<1>	Digital input	I2C address input, bit 1
P12	VSS_GND	Power	ground
P13	OUTP_SUM	Analog output	Analog output, trigger sum, positive
P14	OUTN_SUM	Analog output	Analog output, trigger sum, negative

2.4 Pin list (by pin names)

Table 2. Pin list (by pin names)

Ball pos	Pin name	Type	Description
A9	CK40_N	Digital input	I2C clock input, negative
A8	CK40_P	Digital input	I2C clock input, positive

K12	ext_vref_dac	Power	External reference voltage
P10	I2C_ADDR<0>	Digital input	I2C address input, bit 0
P11	I2C_ADDR<1>	Digital input	I2C address input, bit 1
N11	I2C_ADDR<2>	Digital input	I2C address input, bit 2
N12	I2C_ADDR<3>	Digital input	I2C address input, bit 3
A12	I2C_En	Digital input	Not connected
B7	I2C_ERROR	Digital output	I2C error state
A7	I2C_RSTB	Digital input	I2C reset, active low
A11	I2C_SCL	Digital input	I2C clock
A10	I2C_SDA	Digital I/O	I2C data, open drain
B1	IN<0>	Analog input	analog input channel 0
C1	IN<0>	Analog input	analog input channel 0
E1	IN<1>	Analog input	analog input channel 1
F1	IN<1>	Analog input	analog input channel 1
J1	IN<2>	Analog input	analog input channel 2
K1	IN<2>	Analog input	analog input channel 2
M1	IN<3>	Analog input	analog input channel 3
N1	IN<3>	Analog input	analog input channel 3
P7	N10UA_SH<0>	Power	external bias current
P6	N10UA_SH<1>	Power	external bias current
A2	N1MA2P5_PA<0>	Power	external bias current
G2	n1mA2p5_pa<0>	Power	external bias current
P2	N1MA2P5_PA<0>	Power	external bias current
C4	N1MA2P5_PA<1>	Power	external bias current
M4	N1MA2P5_PA<1>	Power	external bias current
H3	n1mAi_pa	Power	external bias current
C7	n1mAi_sh	Power	external bias current
A6	N1UA_SH<0>	Power	external bias current
M9	N1UA_SH<0>	Power	external bias current
B6	N1UA_SH<1>	Power	external bias current
A5	N5UA_SH<0>	Power	external bias current
M8	N5UA_SH<0>	Power	external bias current
B5	N5UA_SH<1>	Power	external bias current
C14	OUTN_HG<0>	Analog output	Analog output, high gain, channel 0, negative
E14	OUTN_HG<1>	Analog output	Analog output, high gain, channel 1, negative
J14	OUTN_HG<2>	Analog output	Analog output, high gain, channel 2, negative
L14	OUTN_HG<3>	Analog output	Analog output, high gain, channel 3, negative

B14	OUTN_LG<0>	Analog output	Analog output, low gain, channel 0, negative
F14	OUTN_LG<1>	Analog output	Analog output, low gain, channel 1, negative
H14	OUTN_LG<2>	Analog output	Analog output, low gain, channel 2, negative
M14	OUTN_LG<3>	Analog output	Analog output, low gain, channel 3, negative
P14	OUTN_SUM	Analog output	Analog output, trigger sum, negative
C13	OUTP_HG<0>	Analog output	Analog output, high gain, channel 0, positive
E13	OUTP_HG<1>	Analog output	Analog output, high gain, channel 1, positive
J13	OUTP_HG<2>	Analog output	Analog output, high gain, channel 2, positive
L13	OUTP_HG<3>	Analog output	Analog output, high gain, channel 3, positive
B13	OUTP_LG<0>	Analog output	Analog output, low gain, channel 0, positive
F13	OUTP_LG<1>	Analog output	Analog output, low gain, channel 1, positive
H13	OUTP_LG<2>	Analog output	Analog output, low gain, channel 2, positive
M13	OUTP_LG<3>	Analog output	Analog output, low gain, channel 3, positive
P13	OUTP_SUM	Analog output	Analog output, trigger sum, positive
G10	p10uA_sh<0>	Power	external bias current
G9	p10uA_sh<1>	Power	external bias current
E4	p1mAi_2p5_pa	Power	external bias current
H9	p1uA_sh<0>	Power	external bias current
P9	P1UA_SH<0>	Power	external bias current
H8	p1uA_sh<1>	Power	external bias current
F9	p5uA_sh<0>	Power	external bias current
N9	P5UA_SH<0>	Power	external bias current
F8	p5uA_sh<1>	Power	external bias current
E5	PA_ESD	Power	Power ESD, PA
K5	PA_ESD	Power	Power ESD, PA
K7	SH_ESD	Power	Power ESD, shaper
L7	SH_ESD	Power	Power ESD, shaper
B8	VB_CMFB_SH	Power	external bias voltage
P5	VB_CMFB_SH	Power	external bias voltage
C6	vb_fb0_idcp_pa	Power	external bias voltage
M5	vb_fb0_idcp_pa	Power	external bias voltage
A3	VB_FC_PA<0>	Power	external bias voltage
P4	VB_FC_PA<0>	Power	external bias voltage
C5	VB_FC_PA<1>	Power	external bias voltage
P3	VB_FC_PA<1>	Power	external bias voltage

A4	VB_FC_SH	Power	external bias voltage
N6	VB_FC_SH	Power	external bias voltage
H2	vb_ib_pa	Power	external bias voltage
B4	VB_IB_SH	Power	external bias voltage
N5	VB_IB_SH	Power	external bias voltage
G3	vb_it_pa	Power	external bias voltage
D7	VB_IT_SH	Power	external bias voltage
P8	VB_IT_SH	Power	external bias voltage
B9	VB_NAB_SH	Power	external bias voltage
N7	VB_NAB_SH	Power	external bias voltage
C8	VB_PAB_SH	Power	external bias voltage
N8	VB_PAB_SH	Power	external bias voltage
B3	VCM_PA	Power	external bias voltage
N4	VCM_PA	Power	external bias voltage
D12	vcm_sh	Power	external bias voltage
N10	VCM_SH	Power	external bias voltage
D8	VDD1P2_DAC	Power	Power 1.2 V, DAC
E8	VDD1P2_DAC	Power	Power, 1.2 V, DAC
D9	VDD1P2_I2C	Power	Power, 1.2 V, I2C
E9	VDD1P2_I2C	Power	Power, 1.2 V, I2C
C3	VDD1P2_PA	Power	Power, 1.2 V, PA
D2	VDD1P2_PA	Power	Power, 1.2 V, PA
D3	VDD1P2_PA	Power	Power, 1.2 V, PA
E3	VDD1P2_PA	Power	Power, 1.2 V, PA
F3	VDD1P2_PA	Power	Power, 1.2 V, PA
F4	VDD1P2_PA	Power	Power, 1.2 V, PA
G4	VDD1P2_PA	Power	Power, 1.2 V, PA
H4	VDD1P2_PA	Power	Power, 1.2 V, PA
J3	VDD1P2_PA	Power	Power, 1.2 V, PA
J4	VDD1P2_PA	Power	Power, 1.2 V, PA
K3	VDD1P2_PA	Power	Power, 1.2 V, PA
L2	VDD1P2_PA	Power	Power, 1.2 V, PA
L3	VDD1P2_PA	Power	Power, 1.2 V, PA
M3	VDD1P2_PA	Power	Power, 1.2 V, PA
N3	VDD1P2_PA	Power	Power, 1.2 V, PA
C10	VDD1P2_SH_HG<0>	Power	Power, 1.2 V, shaper, high gain, channel 0
C11	VDD1P2_SH_HG<0>	Power	Power, 1.2 V, shaper, high gain, channel 0
E10	VDD1P2_SH_HG<1>	Power	Power, 1.2 V, shaper, high gain, channel 1
E11	VDD1P2_SH_HG<1>	Power	Power, 1.2 V, shaper, high gain, channel 1

J10	VDD1P2_SH_HG<2>	Power	Power, 1.2 V, shaper, high gain, channel 2
J11	VDD1P2_SH_HG<2>	Power	Power, 1.2 V, shaper, high gain, channel 2
L10	VDD1P2_SH_HG<3>	Power	Power, 1.2 V, shaper, high gain, channel 3
L11	VDD1P2_SH_HG<3>	Power	Power, 1.2 V, shaper, high gain, channel 3
B10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
B11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
F10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
F11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
H10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
H11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
M10	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
M11	VDD1P2_SH_LG	Power	Power, 1.2 V, shaper, low gain
G11	VDD1P2_SH_TS	Power	Power, 1.2 V, shaper, trigger sum
G12	VDD1P2_SH_TS	Power	Power, 1.2 V, shaper, trigger sum
L5	VDD2P5_ESD_BOT	Power	Power, 2.5 V, ESD, bottom
D5	VDD2P5_ESD_TOP	Power	Power, 2.5 V, ESD, bottom
D6	VDD2P5_PA	Power	Power, 2.5 V, PA
E6	VDD2P5_PA	Power	Power, 2.5 V, PA
F6	VDD2P5_PA	Power	Power, 2.5 V, PA
G6	VDD2P5_PA	Power	Power, 2.5 V, PA
H6	VDD2P5_PA	Power	Power, 2.5 V, PA
J6	VDD2P5_PA	Power	Power, 2.5 V, PA
K6	VDD2P5_PA	Power	Power, 2.5 V, PA
L6	VDD2P5_PA	Power	Power, 2.5 V, PA
A1	VSS_GND	Power	ground
A13	VSS_GND	Power	ground
A14	VSS_GND	Power	ground
B2	VSS_GND	Power	ground
B12	VSS_GND	Power	ground
C2	VSS_GND	Power	ground
C9	VSS_GND	Power	ground
C12	VSS_GND	Power	ground
D1	VSS_GND	Power	ground
D4	VSS_GND	Power	ground
D10	VSS_GND	Power	ground
D11	VSS_GND	Power	ground
D13	VSS_GND	Power	ground
D14	VSS_GND	Power	ground
E2	VSS_GND	Power	ground

E7	VSS_GND	Power	ground
E12	VSS_GND	Power	ground
F2	VSS_GND	Power	ground
F5	VSS_GND	Power	ground
F7	VSS_GND	Power	ground
F12	VSS_GND	Power	ground
G1	VSS_GND	Power	ground
G5	VSS_GND	Power	ground
G7	VSS_GND	Power	ground
G8	VSS_GND	Power	ground
G13	VSS_GND	Power	ground
G14	VSS_GND	Power	ground
H1	VSS_GND	Power	ground
H5	VSS_GND	Power	ground
H7	VSS_GND	Power	ground
H12	VSS_GND	Power	ground
J2	VSS_GND	Power	ground
J5	VSS_GND	Power	ground
J7	VSS_GND	Power	ground
J8	VSS_GND	Power	ground
J9	VSS_GND	Power	ground
J12	VSS_GND	Power	ground
K2	VSS_GND	Power	ground
K4	VSS_GND	Power	ground
K8	VSS_GND	Power	ground
K9	VSS_GND	Power	ground
K10	VSS_GND	Power	ground
K11	VSS_GND	Power	ground
K13	VSS_GND	Power	ground
K14	VSS_GND	Power	ground
L1	VSS_GND	Power	ground
L4	VSS_GND	Power	ground
L8	VSS_GND	Power	ground
L9	VSS_GND	Power	ground
L12	VSS_GND	Power	ground
M2	VSS_GND	Power	ground
M6	VSS_GND	Power	ground
M7	VSS_GND	Power	ground
M12	VSS_GND	Power	ground

N2	VSS_GND	Power	ground
N13	VSS_GND	Power	ground
N14	VSS_GND	Power	ground
P1	VSS_GND	Power	ground
P12	VSS_GND	Power	ground

3. Electrical interface

ALFE2 power domains are listed in Table 3. The shaper power supply is split into the HG, LG, and TS branches on ALFE2. This is to mitigate potential crosstalk from the HG branch to the LG and SUM branches when the HG branch saturates. Since there are internal connections (current mirrors) among the HG, LG, and TS branches, it is critical to connect Pins VCC1V2_SH_LG/HG/TS together to the same power plane. Any voltage difference among these pins will be amplified and appear as the noise at the output stage of ALFE2. The I2C and DAC may be optionally isolated from the 1.2 V power plane with a ferrite bead (tests on the ALFE2 prototype board did not yield any performance difference).

Table 3. Power domains of ALFE2

Pin names	Voltage (V)	Nominal Current (mA)	Domain	Notes
VCC1V2_DAC	1.2	5	Digital	Internal DAC supply.
VCC1V2_I2C	1.2			I2C block supply.
VCC1V2_PA	1.2	85	1.2 V PA	PA input stage
VCC2V5_PA	2.5	102	2.5 V PA	PA output stage. Increases by ~3mA for 25 Ω configuration
VCC1V2_SH_LG	1.2	101	Shaper	Shaper low-gain channels
VCC1V2_SH_HG		91		Shaper high-gain channels
VCC1V2_SH_TS		18		Shaper trigger sum. Increases by ~4 mA when channel gains are set to 3.

ALFE2 needs three currents, each with a nominal value of 1 mA, to properly bias its internal circuits. The power consumption of ALFE2 is linearly dependent on these bias currents. ALFE2 contains an internal triple-channel 6-bit DAC and a BGR to generate the DAC reference voltage for ALFE2 bias. This is the intended mode of operation. The user may indirectly monitor the currents of the PA 1.2 V, PA 2.5 V, and shaper 1.2 V domains by measuring the voltage on Pins n1mAi_pa, p1mAi_2p5_pa, and n1mAi_sh, respectively. ALFE2 can use external bias currents. The user may also choose to bypass the BGR and externally provide a DAC reference voltage on the ext_vref_dac pin. This is intended for test purposes. The block diagram of the bias network and external circuits is shown in Figure 5.

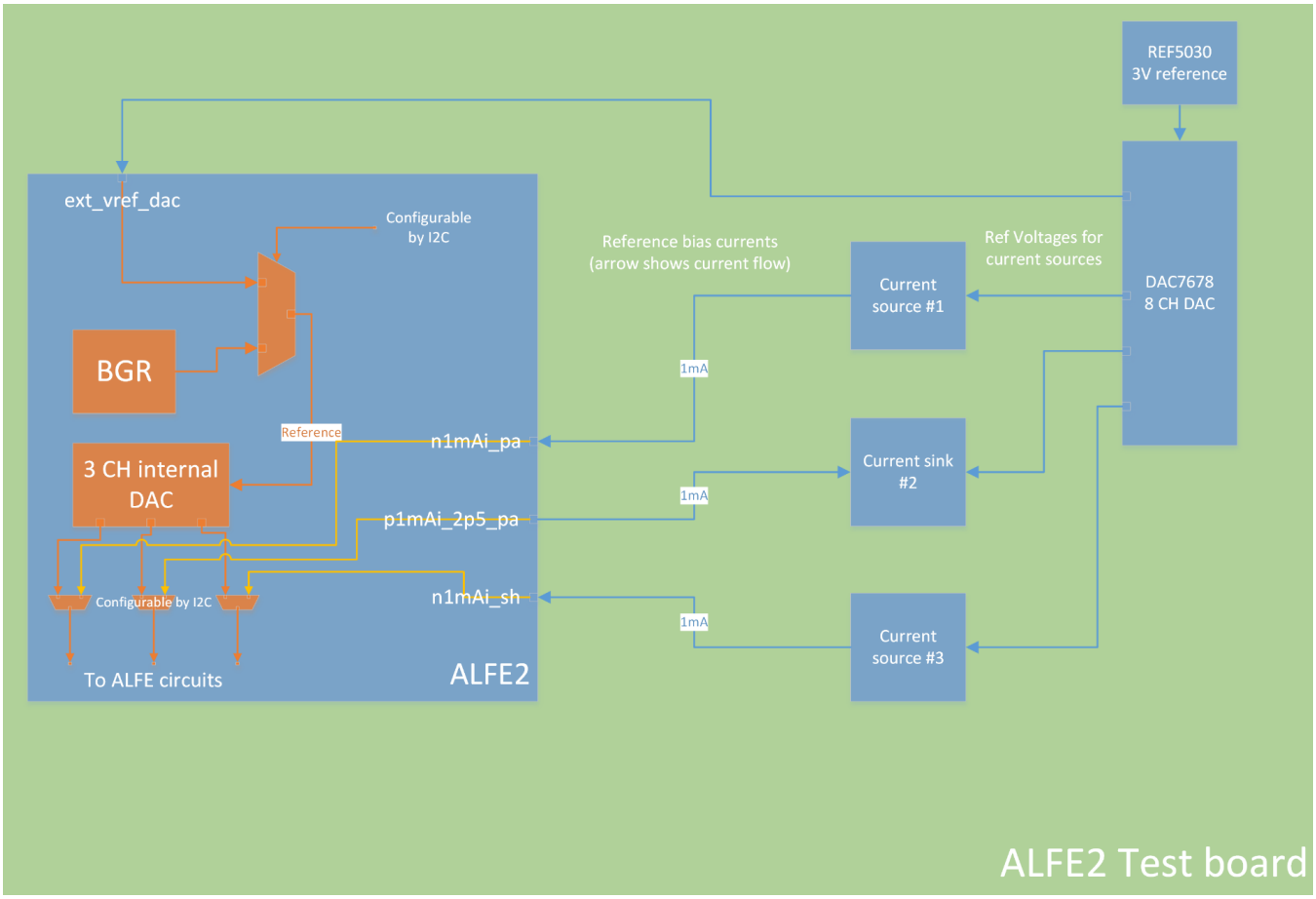

Figure 5. Block diagram of the bias network and external circuits.

4. I2C interface

4.1 I2C protocol

The ALFE2 chip has 16 8-bit internal registers. These registers can be written or read via an I2C interface. Each register has an address from 0 to 15 (4'hF). The definition of the registers is listed in Section 4.2.

These registers cannot be written or read directly. Instead, the internal registers are accessed via eight control registers. The block diagram of the I2C target functional block is shown in Figure 6. To access the control register, the I2C address is defined as {ADDR[3:0], Rctrl [2:0], R/W}. The address pins ADDR[3:0] are the four Most Significant Bits (MSBs). The last LSB (R/W) is 1 for a read operation or 0 for a write operation. The remaining three bits Rctrl[2:0] select one of eight control registers (from R0 to R7). The control registers are defined in Table 4.

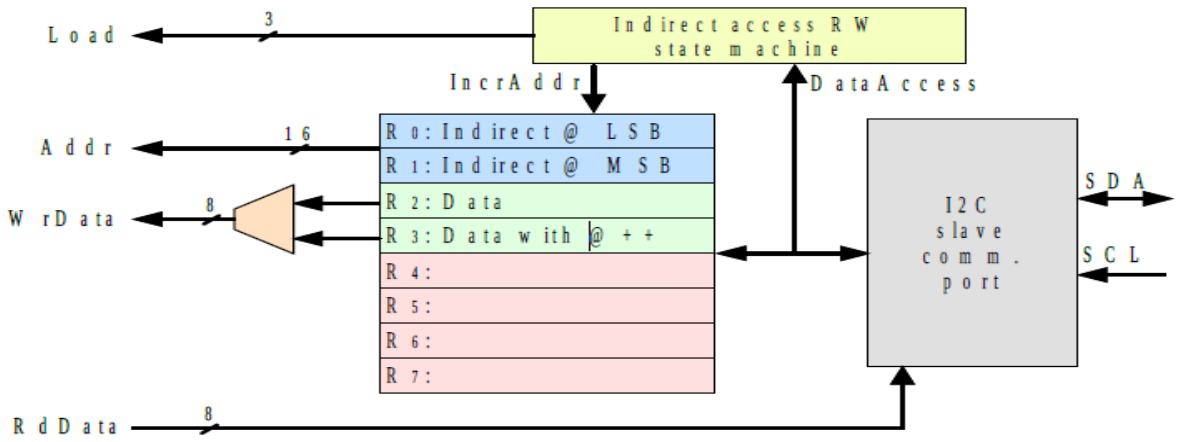

Figure 6. Block diagram of Internal I2C functional block.

Table 4. Functions of control registers (R0–R7).

Rctrl[2:0]	Functions of control registers (the meaning of the following byte)
000 (R0)	Register address (LSB byte)
001 (R1)	Register address (MSB byte) (8'H00 since ALFE2 has only 16 registers)
010 (R2)	Data byte
011 (R3)	Data byte with automatic address increment after each access
100-111 (R4-R7)	Reserved

The I2C interface of ALFE2 has two operational modes. One can access a single register or multiple consecutive registers. In the former mode, one writes a byte to a single register to read a byte from a register. In the latter mode, one writes or reads a register block. After each writing or reading, the internal register address automatically increases for the following writing or reading.

The procedure of writing a byte to a single register is shown in Figure 7. The procedure of writing a single register includes three I2C operations. Each operation has the following steps:

1) The controller transmits a START command (marked as S in the figure).
2) The controller transmits four address pins, three bits to select R0, R1, or R2, and the 8th R/W bit that is set to zero (write).
3) The ALFE2 acknowledges if its target address is identified (marked as A in the figure). If no target acknowledges (NA), the controller transmits a STOP command to end the operation.
4) The controller transmits a byte to Register R0, R1, or R2.
5) The ALFE2 acknowledges if its target address is identified.
6) The controller transmits a STOP command (marked as P in the figure).

In the figure, the commands in green are controlled by the controller, while the commands in blue are controlled by the target. To set a specific 8-bit word in the chip, the user must write in the R0 register and in the R1 register to select the register address, and then write the data in the R2 register.

S	Dev_Addr[3:0]	000, R0	W	A	Reg_Addr[7:0]	A	P
S	Dev_Addr[3:0]	001, R1	W	A	8'b0000_0000	A	P
S	Dev_Addr[3:0]	010, R2	W	A	Byte_to_be_writtten[7:0]	A	P

Figure 7. Procedure to write a single register.

An example waveform of writing a byte of 9 to Chip address 5, Register 4 is shown in Figures 8–11. Figure 8 shows the waveform on an oscilloscope. Figures 9–11 display zoomed waveforms. The data in the R0 register are the register address of 4. The data in the R1 register are 0. The data in the R2 register are the value (0x09) one wants to write into the register.

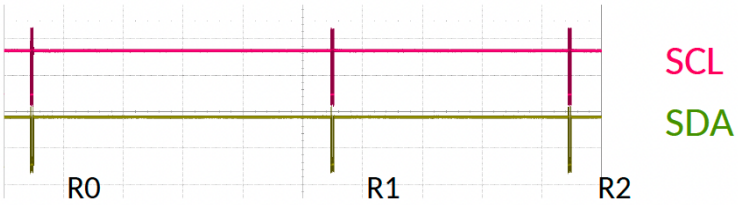

Figure 8. Oscilloscope waveform of an I2C write frame.

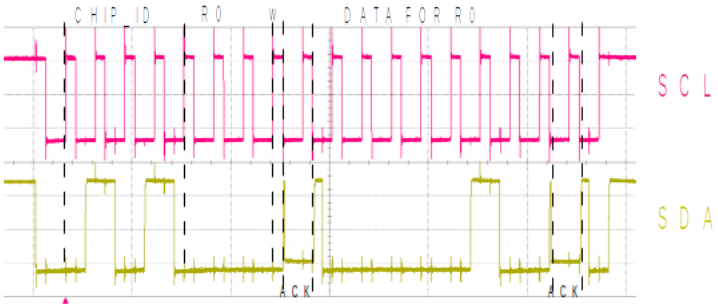

Figure 9: Zoomed waveform of the Register R0

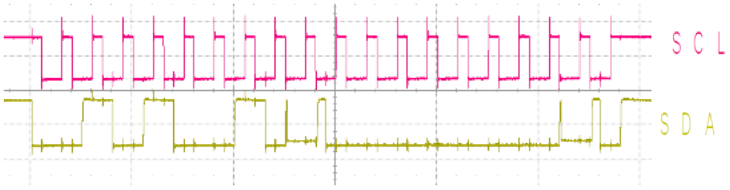

Figure 10: Zoomed waveform of the Register R1

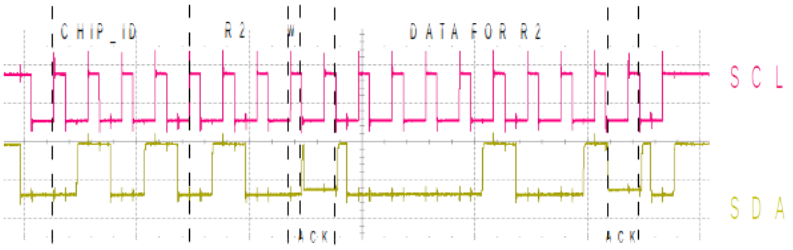

Figure 11. Zoomed waveform of the Register R2.

The procedure of reading a byte from a single register is shown in Figure 12. The procedure of reading a single register includes three I2C operations. To read a byte from a specific register, one must write in the R0 register and in the R1 register to select the register, and then read the data from the R2 register.

S	Dev_Addr[3:0]	000, R0	W	A	Reg_Addr[7:0]	A	P
S	Dev_Addr[3:0]	001, R1	W	A	8'b0000_0000	A	P
S	Dev_Addr[3:0]	010, R2	R	A	Byte_read_back[7:0]	NA	P

Figure 12. Procedure to write a single register.

An example of reading a byte from Chip address 5, Register 9 is shown in Figures 13–16. Figure 13 shows the waveform on an oscilloscope. Figures 14–16 display zoomed waveforms. The data in the R0 register is the register address of 9. The data in the R1 register are 0. The data in the R2 register are the value (0x73) that is read back.

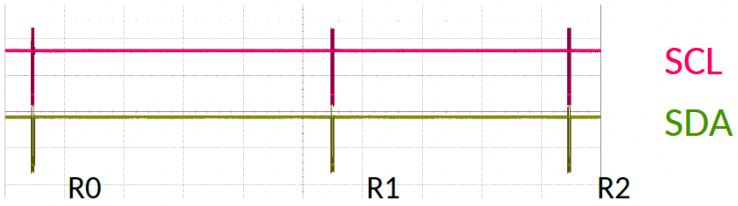

Figure 13. Oscilloscope signals of frame READ.

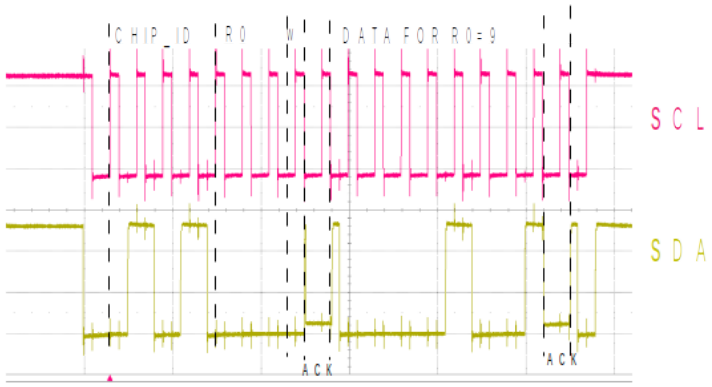

Figure 14. ZOOM on the Register R0

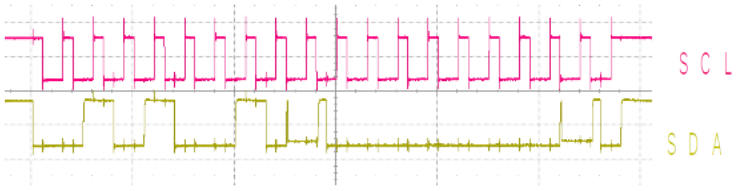

Figure 15. ZOOM on the Register R1.

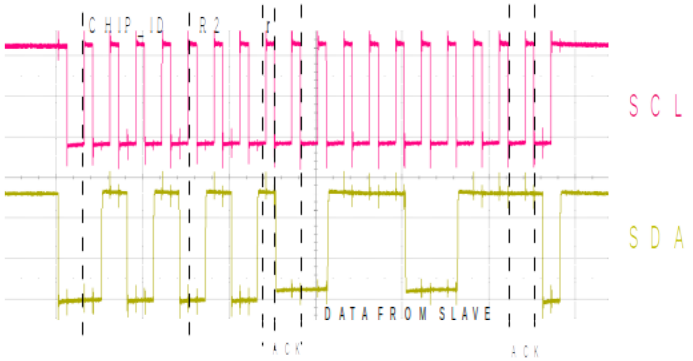

Figure 16. ZOOM on the Register R2.

The user can also write or read at consecutive register addresses. In this mode, rather than writing or reading the R2 register, the user successively writes or reads the R3 register. The procedure of writing or reading in consecutive addresses is shown in Figures 17 and 18.

S	Dev_Addr[3:0]	000, R0	W	A	Reg_Addr[7:0]	A	P
S	Dev_Addr[3:0]	001, R1	W	A	8'b0000_0000	A	P
S	Dev_Addr[3:0]	011, R3	W	A	Byte0_to_be_writtten[7:0]	A	P
S	Dev_Addr[3:0]	011, R3	W	A	Byte1_to_be_writtten[7:0]	A	P
S	Dev_Addr[3:0]	011, R3	W	A	Byte2_to_be_writtten[7:0]	A	P
S	Dev_Addr[3:0]	011, R3	W	A	Byte3_to_be_writtten[7:0]	A	P
S	Dev_Addr[3:0]	011, R3	W	A	Byte4_to_be_writtten[7:0]	A	P

Figure 17. Procedure of consecutive write operations.

S	Dev_Addr[3:0]	000, R0	W	A	Reg_Addr[7:0]	A	P
S	Dev_Addr[3:0]	001, R1	W	A	8'b0000_0000	A	P
S	Dev_Addr[3:0]	011, R3	R	A	Byte0_read_back[7:0]	NA	P
S	Dev_Addr[3:0]	011, R3	R	A	Byte1_read_back[7:0]	NA	P
S	Dev_Addr[3:0]	011, R3	R	A	Byte2_read_back[7:0]	NA	P
S	Dev_Addr[3:0]	011, R3	R	A	Byte3_read_back[7:0]	NA	P
S	Dev_Addr[3:0]	011, R3	R	A	Byte4_read_back[7:0]	NA	P

Figure 18. Procedure of consecutive read operations.

4.2 Register map

ALFE2 uses unary coding or thermometer code for most of its control registers. The remaining bits directly interface with the ALFE2 circuits (e.g., enable signal).

Some ALFE2 control registers are split into multiple registers. Therefore, multiple I2C transactions are necessary to access them. An example of an ALFE2 control register being split into two registers is shown in Figure 19.

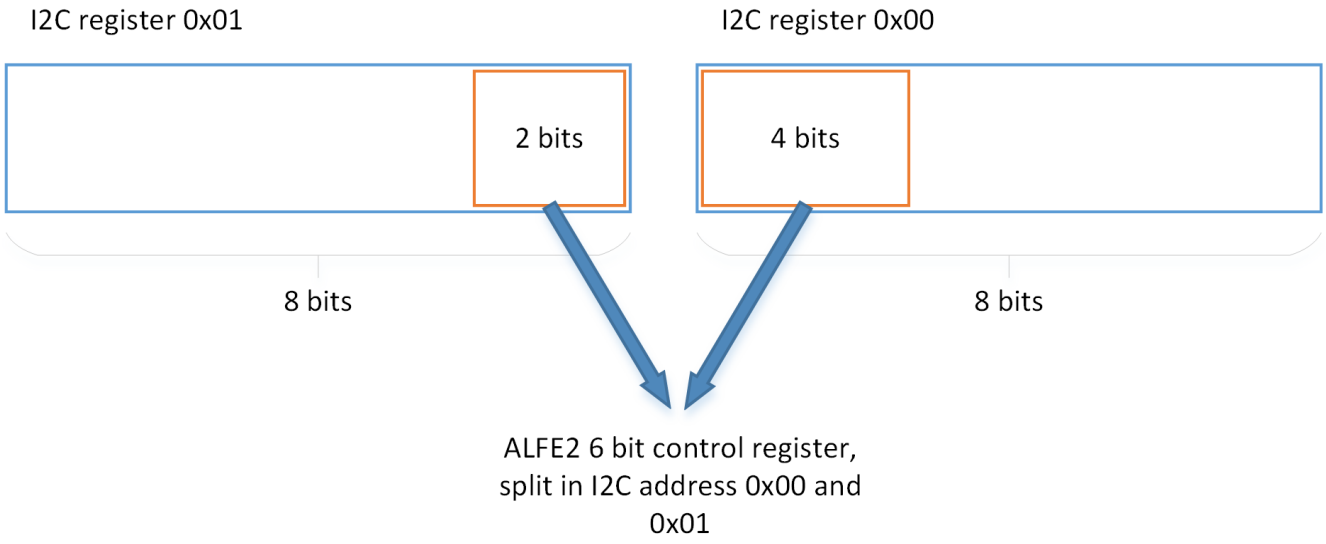

Figure 19. Example of an ALFE2 register being split into two registers. The highlighted bits do not correspond to an actual ALFE2 register.

Register 0x00

Address	Control Name	Description	Bits	Default after reset
0x00	ch_pwr	Channel power down register. Each bit represents one channel. 0b0 channel is powered on 0b1 channel is powered off The most significant bit of the register corresponds to channel 3. [CH3, CH2, CH1, CH0]	[3:0]	0x0
	pa_fb_r0	Sets the preamplifier feedback resistance #0. Used to switch between 50 Ω and 25 Ω modes.	[5:4]	0b01

		0b01 50 Ω mode 0b11 25 Ω mode		
	pa_fb_c0	Sets the preamplifier feedback capacitance #0. Used to switch between 50 Ω and 25 Ω modes. 0b01 50 Ω mode 0b11 25 Ω mode	[7:6]	0b01

Register 0x01

Address	Control Name	Description	Bits	Default after reset
0x01	pa_out_offset	Sets the offset current at the preamplifier output. Used to switch between 50 Ω and 25 Ω modes. 0x1 50 Ω mode 0xF 25 Ω mode	[3:0]	0x1
	pa_fb_c1	Sets the preamplifier's feedback capacitance #1. Used to switch between 50 Ω and 25 Ω modes. 0b01 50 Ω mode 0b11 25 Ω mode	[5:4]	0b01
	imped_coarse	Input impedance coarse tuning. Used to switch between 50 Ω and 25 Ω modes. 0b11 50 Ω mode 0b00 25 Ω mode	[7:6]	0b11

Registers 0x02, 0x03, 0x04

Address	Control Name	Description	Bits	Default after reset
0x02, 0x03, 0x04	imped_fine	Input impedance fine tuning. The tuning of the input impedance is done to account for process variations that might affect the input impedance of the chip. The register uses unary coding. Only 22 different values are possible. The register is split between 3 I2C addresses. To read/write this register all these registers must be accessed. 0x0007FF 50 Ω mode 0x000FFF 25 Ω mode	0x04: [4:0] 0x03: [7:0] 0x02: [7:0]	0x0000FF

Registers 0x04, 0x05, 0x06

Address	Control Name	Description	Bits	Default after reset
0x04	pa_fb_r1	Sets the preamplifier feedback resistance #1. Used to switch between 50 Ω and 25 Ω modes. 0b1 50 Ω mode 0b0 25 Ω mode	[5]	0b1
0x04, 0x05	pa_output_dc	Fine adjustment of the preamplifier output DC level.	0x05: [5:0] 0x04: [7:6]	0x1F
0x05, 0x06	sh_pt	Adjusts the shaper peaking time. The register uses unary coding. Only 11 values are possible.	0x06: [7:0] 0x05: [7:6]	0x01F

Registers 0x07, 0x08

Address	Control Name	Description	Bits	Default after reset
0x07	en_sh_lg_gain_boost	Tune the LG output gain on the shaper stage. This option is intended to be used for the 25 Ω configuration. This option does not affect the high-gain outputs. The peaking time is slightly affected. 0b1 Enable gain boost 0b0 Disable gain boost	[0]	0b0
0x07, 0x08	sh_output_dc	Adjusts the DC level of the output pins. The register uses unary coding. Only 16 different DC levels are possible.	0x08: [7:0] 0x07: [7:1]	0x03FF

Register 0x09

Address	Control Name	Description	Bits	Default after reset
0x09	sh_sum_pwr	Sum power down register. 0b0 sum is powered on 0b1 sum is powered off	[0]	0b0
	sh_sum_gain_ch0	Individual control of the gain of each channel for the sum output. The register uses unary coding. Only 4 different	[3:1]	0b001
	sh_sum_gain_ch1		[6:4]	0b001

		values are possible.		

Register 0x09 (continued), 0x0A, 0x0B, 0x0C

Address	Control Name	Description	Bits	Default after reset
0x09, 0x0A	sh_sum_gain_ch2	Individual control of the gain of each channel for the sum output. The register uses unary coding. Only 4 different values are possible.	0x0A: [1:0] 0x09: [7]	0b001
0x0A	sh_sum_gain_ch3		[4:2]	0b001
0x0A, 0x0B, 0x0C	sh_sum_output	Adjusts the DC level of the sum pin. The register uses unary coding. Only 16 different DC levels are possible.	0x0C: [3:0] 0x0B: [7:0] 0x0A: [7:5]	0x03FF

Register 0x0C (continued), 0x0D, 0x0E

Address	Control Name	Description	Bits	Default after reset
0x0C, 0x0D	dacn0_cur	Tuning of the current source bias current (1V2 PA domain). Tuning may be necessary due to process variations. This register uses binary format.	0x0D: [1:0] 0x0C: [7:4]	0x30
0x0D	dacn1_cur	Tuning of the current source bias current (1V2 SH and SUM domain). Tuning may be necessary due to process variations. This register uses binary format.	[7:2]	0x30
0x0E	dacp1_cur	Tuning of the current sink bias current (2V5 PA domain). Tuning may be necessary due to process variations. This register uses binary format.	[5:0]	0x0F

Register 0x0E (continued), 0x0F

Address	Control Name	Description	Bits	Default after reset
0x0E	bgr_sel	Select the source for the internal DAC reference. 0b01 Use BGR for the DAC reference 0b11 User voltage provided to the ext_ref_dac pin.	[7:6]	0b11

		0b10 and 0b00 Do not use. This will disconnect both BGR and ext_ref_dac pin.		
0x0F	pa1v2_cur	1V2 PA domain current reference selection. 0b0 External current reference. In this case, the user must provide a 1 mA reference current to the corresponding pin. 0b1 Internal current reference (default)	[0]	0b1
	sh1v2_cur	1V2 SH and SUM domain current reference selection. 0b0 External current reference. In this case, the user must provide a 1 mA reference current to the corresponding pin. 0b1 Internal current reference (default)	[1]	0b1
	pa2v5_cur	2V5 PA domain current reference selection. 0b0 External current reference. In this case, the user must provide a 1 mA reference current to the corresponding pin. 0b1 Internal current reference (default)	[2]	0b1
	unused	N/C. Does not affect chip operation.	[7:3]	0x00

4.3 Example control register configurations

After the power-up and I2C reset, the ALFE2 registers are set to their default values. To operate the chip as intended, some register values must be changed. Two example configurations are given, for 25 Ω and 50 Ω input impedance. These example configurations are labeled as the 25 Ω and 50 Ω modes and are listed in Table 5.

Table 5. Example configurations.

Control name	Default value (reset)	50 Ω mode	25 Ω mode
ch_pwr	0x0	0x0	0x0
pa_fb_r0	0b01	0b01	0b11
pa_fb_c0	0b01	0b01	0b11
pa_out_offset	0x1	0x1	0xF
pa_fb_c1	0b01	0b01	0b11
imped_coarse	0b11	0b11	0b00
imped_fine	0x0000FF	0x0007FF	0x000FFF
pa_fb_r1	0b1	0b1	0b0
pa_output_dc	0x1F	0x1F	0x1F
sh_pt	0x01F	0x0F	0x07
en_sh_lg_gain_boost	0b0	0b0	0b0
sh_output_dc	0x03FF	0x03FF	0x03FF
sh_sum_pwr	0b0	0b0	0b0
sh_sum_gain_ch0	0b001	0b001	0b001
sh_sum_gain_ch1	0b001	0b001	0b001
sh_sum_gain_ch2	0b001	0b001	0b001
sh_sum_gain_ch3	0b001	0b001	0b001
sh_sum_output	0x03FF	0x03FF	0x03FF
dacn0_cur	0x30	0x30	0x30
dacn1_cur	0x30	0x30	0x30
dacp1_cur	0x0F	0x0F	0x0F

bgr_sel	0b11	0b01	0b01
pa1v2_cur	0b1	0b1	0b1
sh1v2_cur	0b1	0b1	0b1
pa2v5_cur	0b1	0b1	0b1