

LSB2 pre-prototypes

Saclay, Pittsburgh

Adaptation of PA/Sh output dynamic range to LTDB input

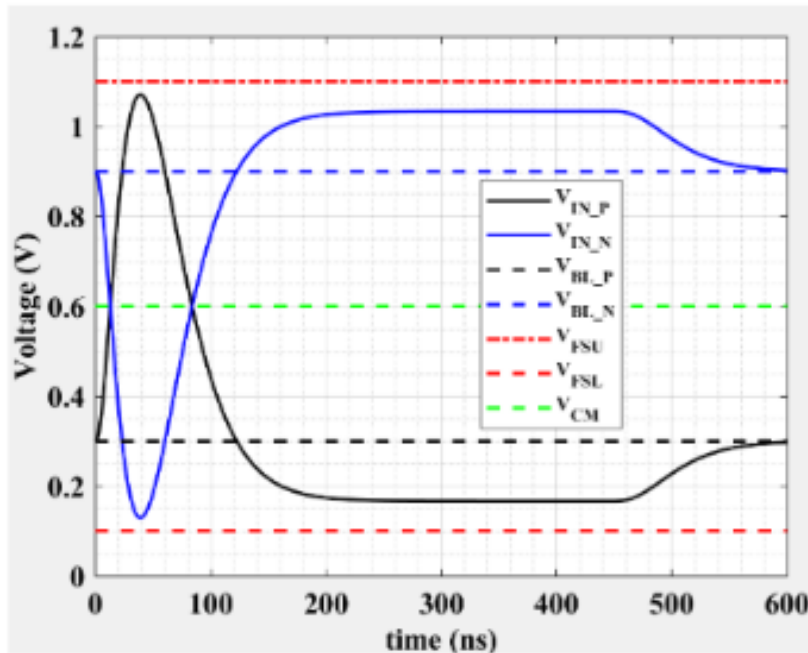
PA/Sh output is differential
output swing 2V
Common mode 600 mV

LTDB input (i.e. LSB output) is single-ended
LTDB Input swing is about 5V (-1.8/3.2) typical

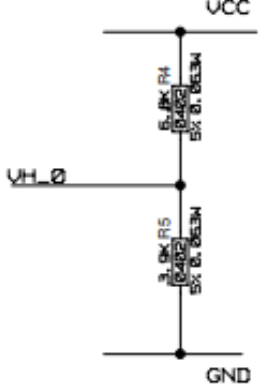
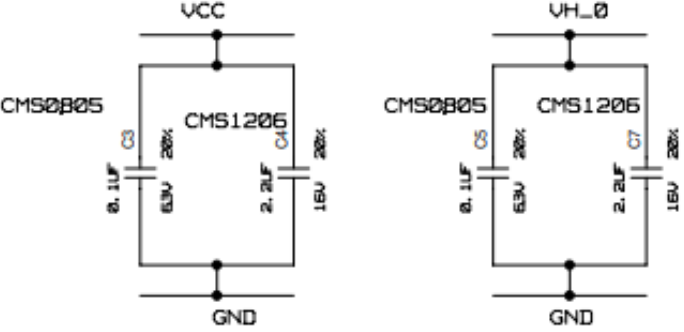
LSB2 have to implement a gain of 2.2 or 3.3 (depending upon calorimeter region), plus differential to single-end conversion

LSB2 pre-prototypes have gain 2 or 3, can be modified to 2.2/3.3 .

Most of the signals do not need summing (already done at the Pa/Sh level on its trigger outputs). Pre-prototype LSB2s have no summing implemented, only differential to single end conversion plus gain

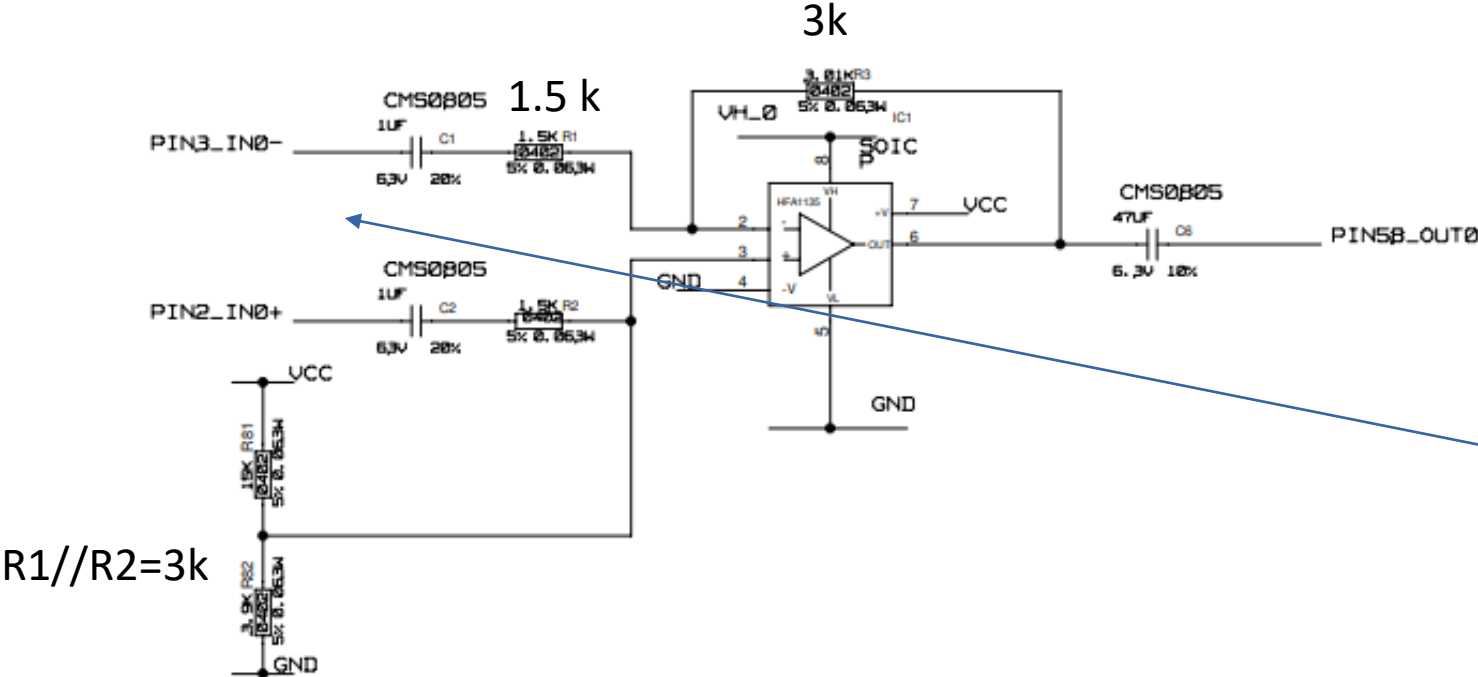


Implemented schematics



Coupling is AC at input and AC at output

One HFA 1135 per channel, implemented as a single supply differential amplifier with input level shifting (3.5 V)

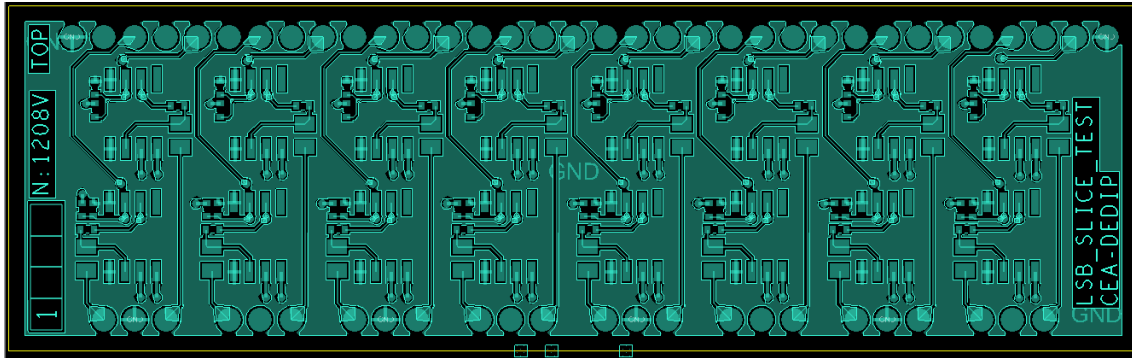


R1//R2=3k

100 ohms adaptation resistor to be added manually

Implementation

GND Diff inputs on this side GND



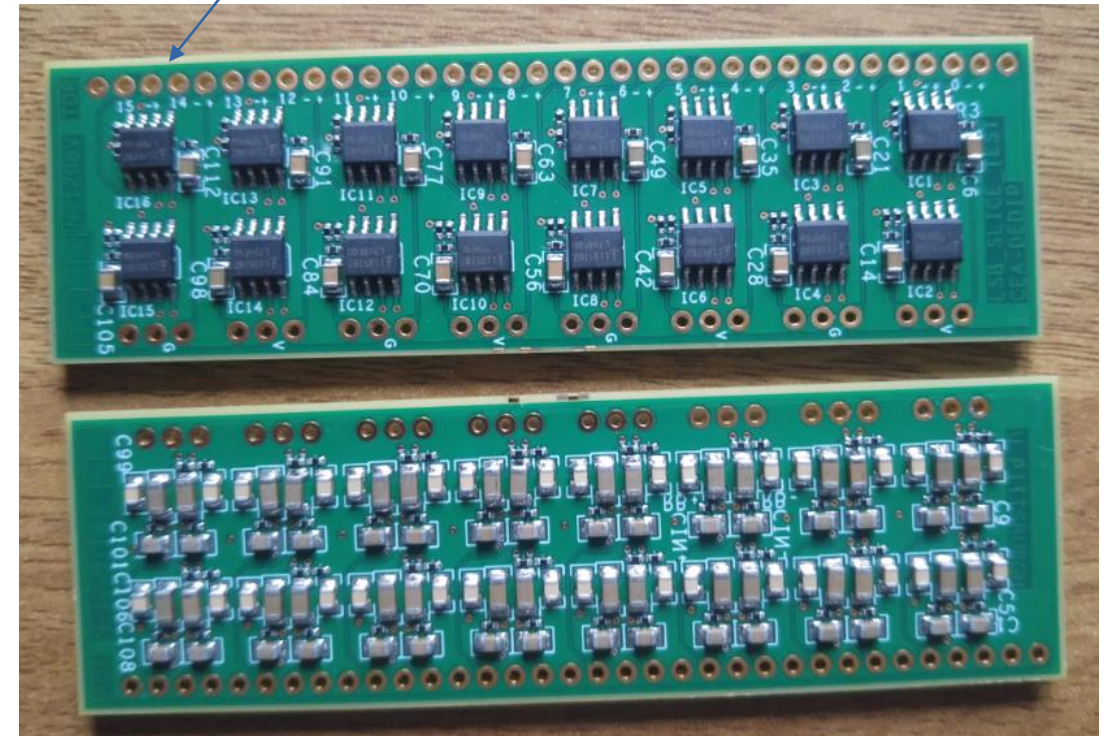
SE outputs + power and GND on this side

Four layer PCB

- Signal top
- GND
- Power
- Signal bottom

- Halogen free PCB material
- Total thickness ≈ 1.5 mm
- Capacitors are 0805 or 1206
- Resistors are 0402

100 ohms resistors added manually here



- Same form factor as phase-0 and phase-1 LSBs
- Same connection pins as Phase-0 (mfg Advanced Interconnect)
- Can be mounted on the FEB2 slice test board

What needs to be done to prepare the integration test on the slice test board ?

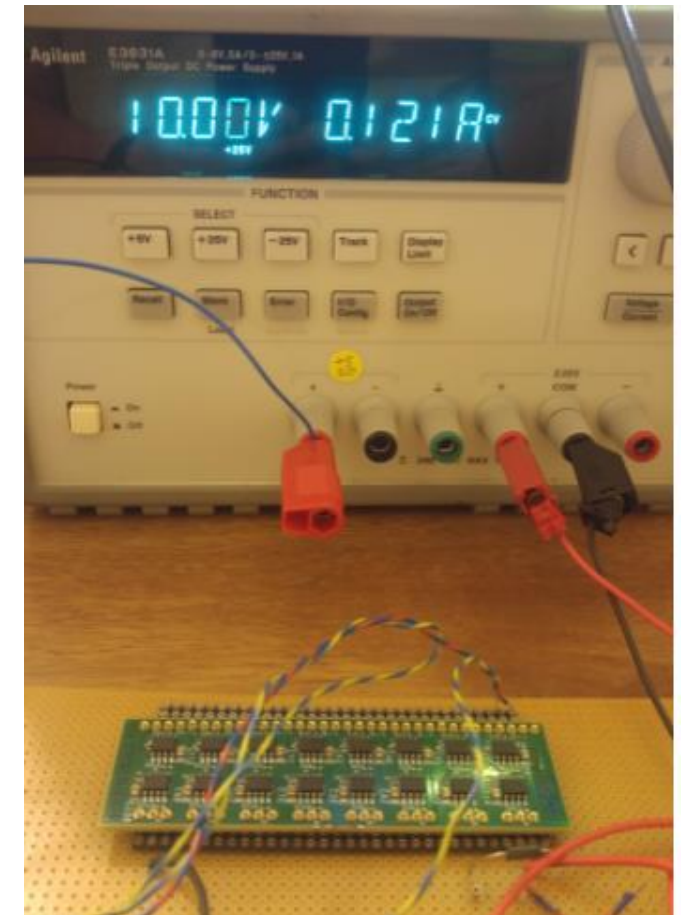
- Aim is to have two boards available : gain 2.2, gain 3.3
 - One already has the 100 ohms termination resistors added, need to prepare an other one
 - Check (again) polarization points
 - Change gain from 2 to 2.2, and from 3 to 3.3
 - Should be done by mid July
- Plan to mate at Saclay an existing pre-prototype with ALFE from CV4
 - Should be done by mid July
- To be done with the pre-prototype board once at Nevis :
 - Power consumption measurement
 - Polarization points on each opamp : V_{cc} , V_H , V_L , $IN+$, $IN-$
 - Noise measurement on the 10 V power line

Backup slides

Lab measurements

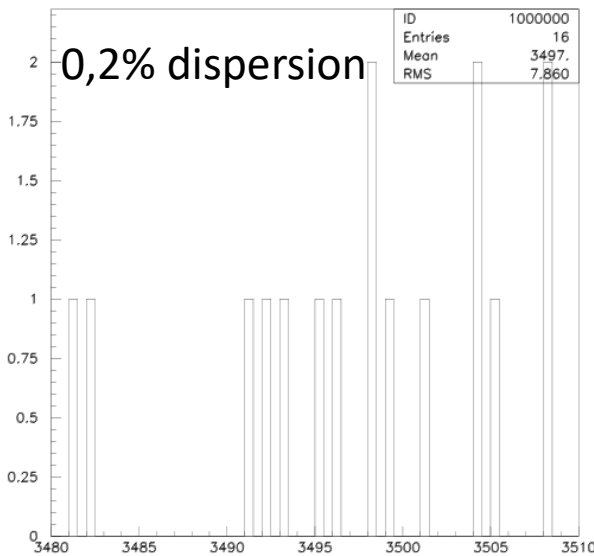
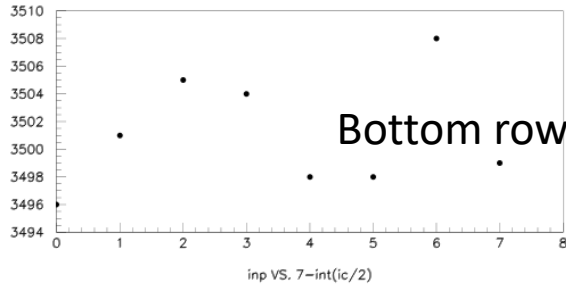
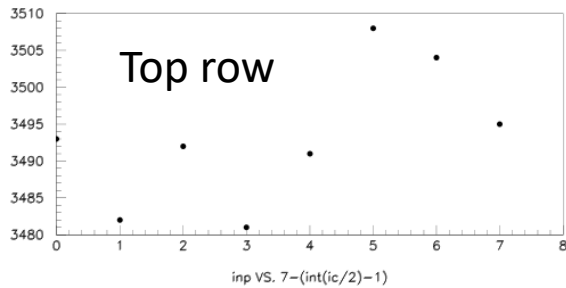
Power consumption

- Test setup
 - RTM 3004 Rohde & Schwarz oscilloscope, 1 GHz BW
 - Agilent E3631 A power supply
- Measured 121 mA for 16 channels, under $V_{cc}=10\text{ V} \rightarrow 7.6\text{ mA/channel}$.
- LTSpice prediction : 6.5 mA/channel \rightarrow OK
- Observed some tendency of the power consumption to increase with increasing temperature (a few mA increase when board gets somewhat hot (40 °C ?))

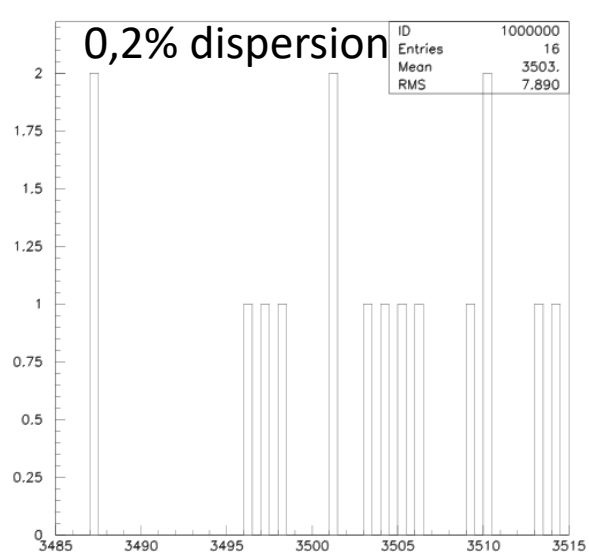
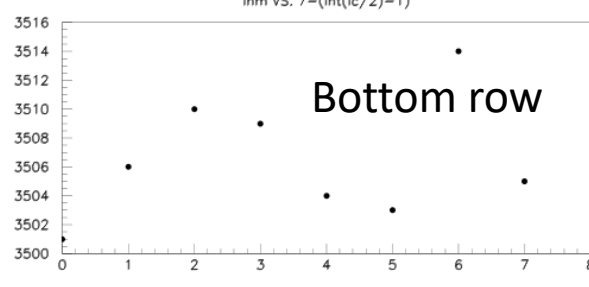
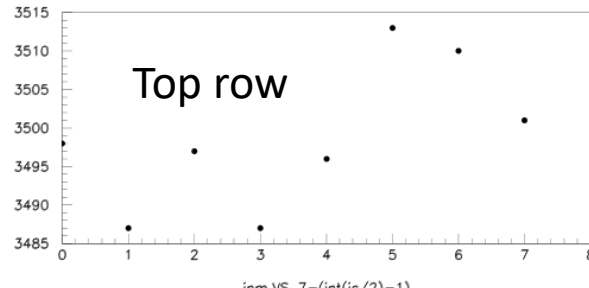


Static polarisation data

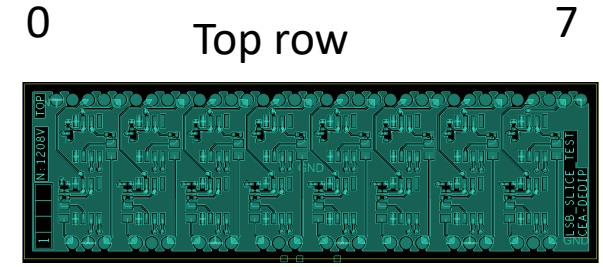
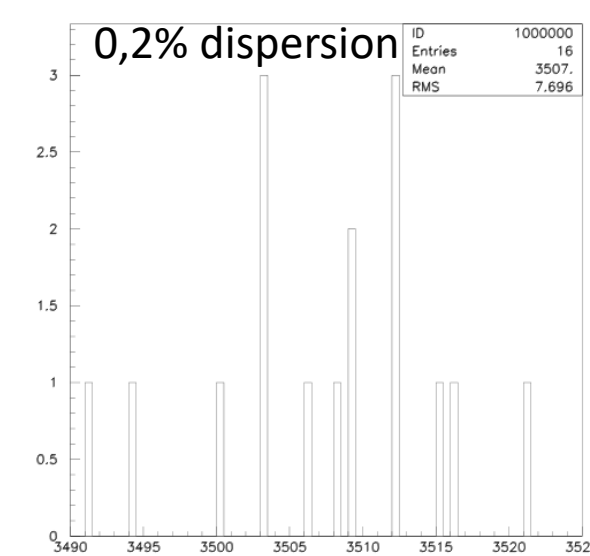
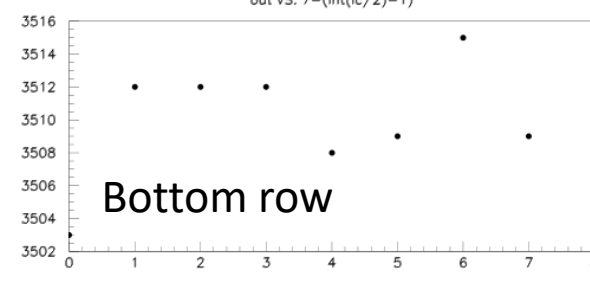
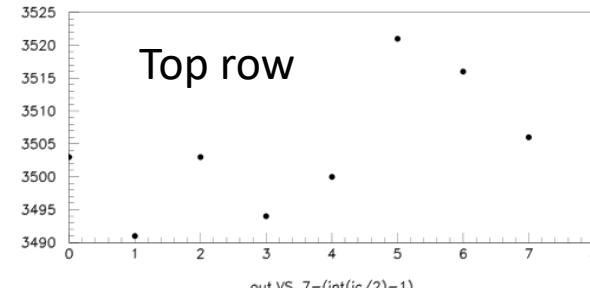
HFA IN+



HFA IN-



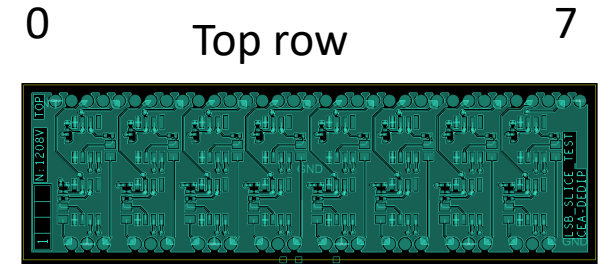
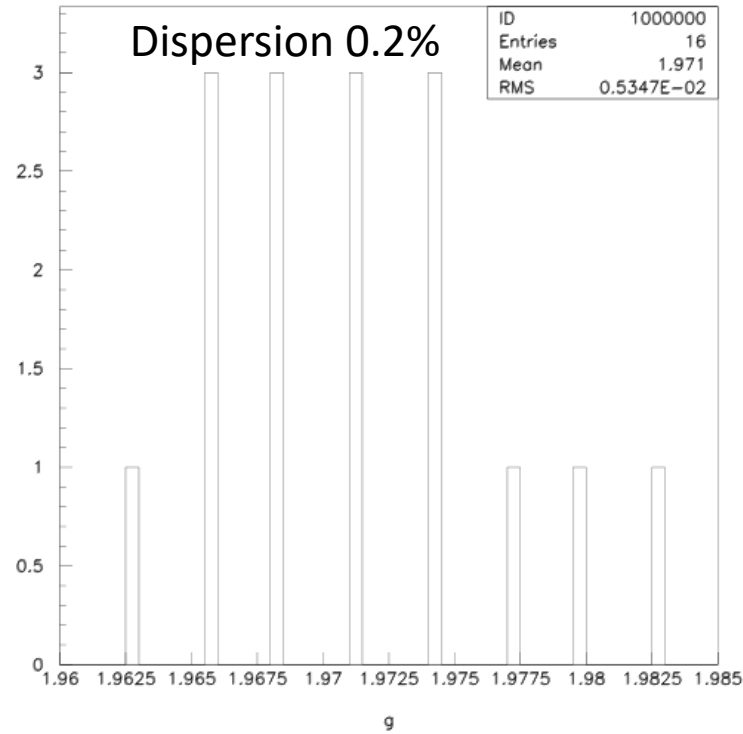
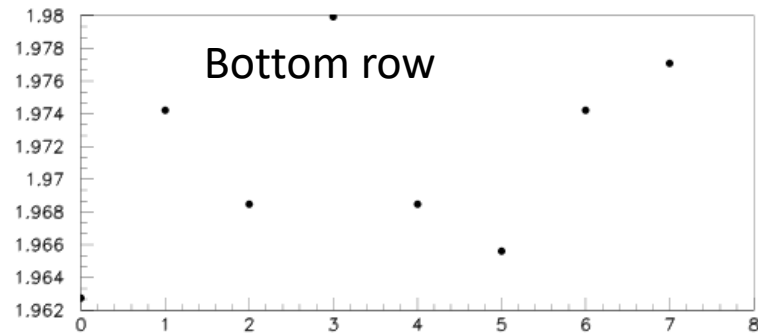
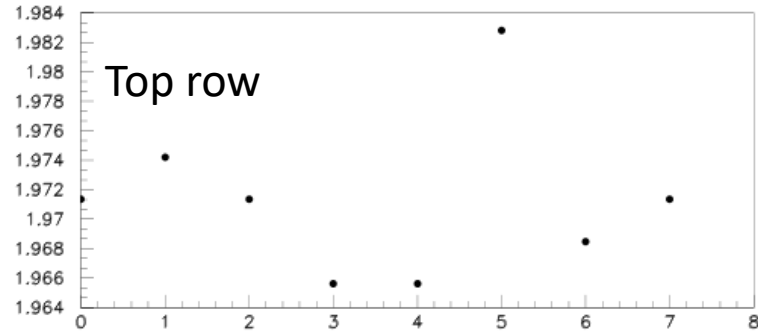
HFA OUT



Bottom row

- Resistors are at 1% precision
- No trend visible as a function of position on the PCB → OK

Gain uniformity (1 MHz sine, 250 mVpp)

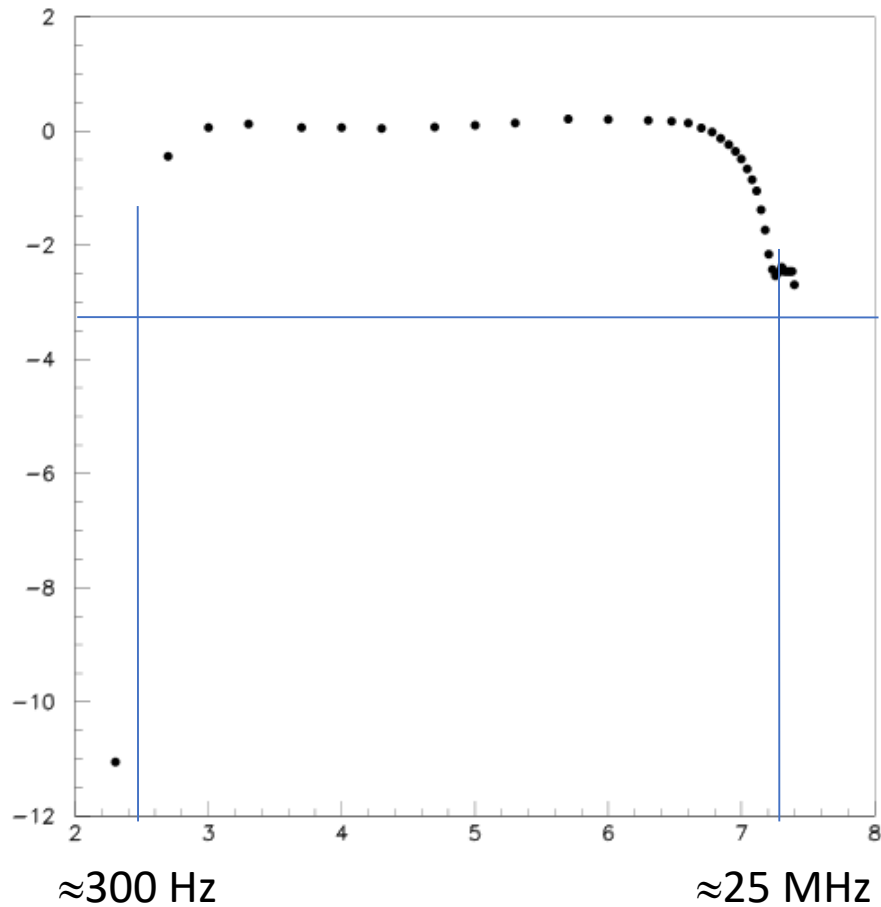


Bottom row

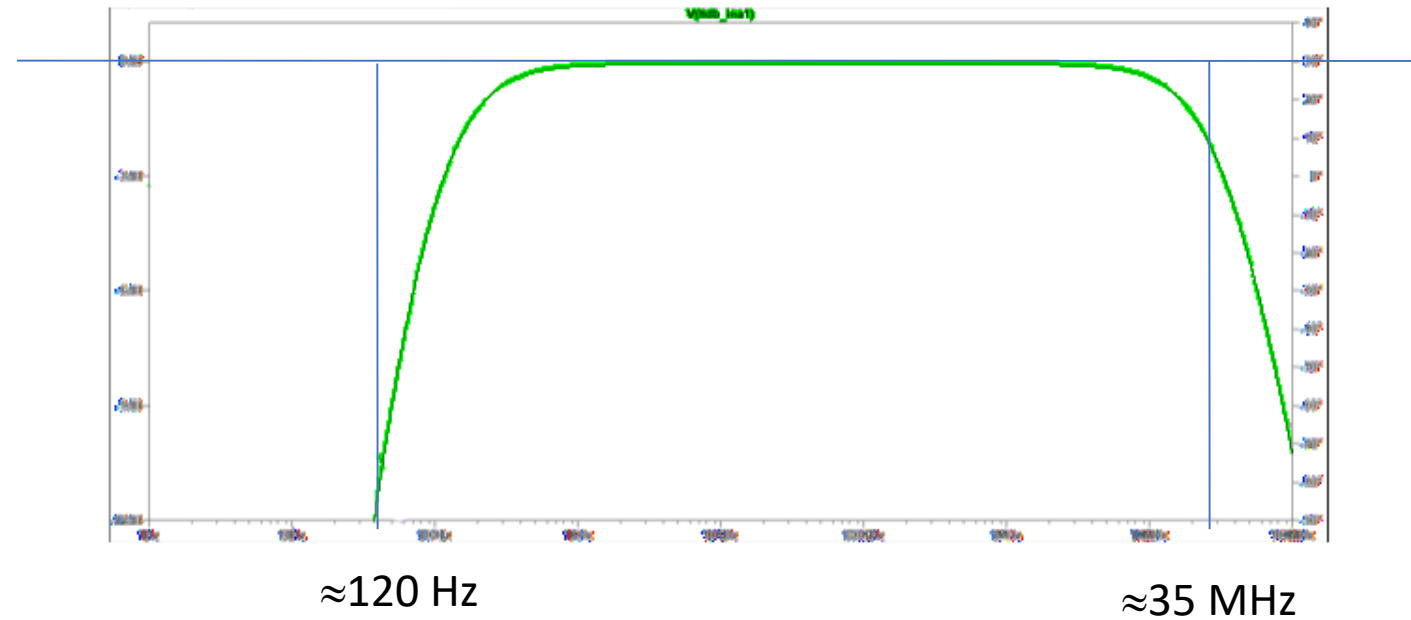
Gain uniformity is OK

Bode diagram

- Measured using a sine wave, amplitude 1.12 Vpp, frequency from 100 Hz to 25 MHz

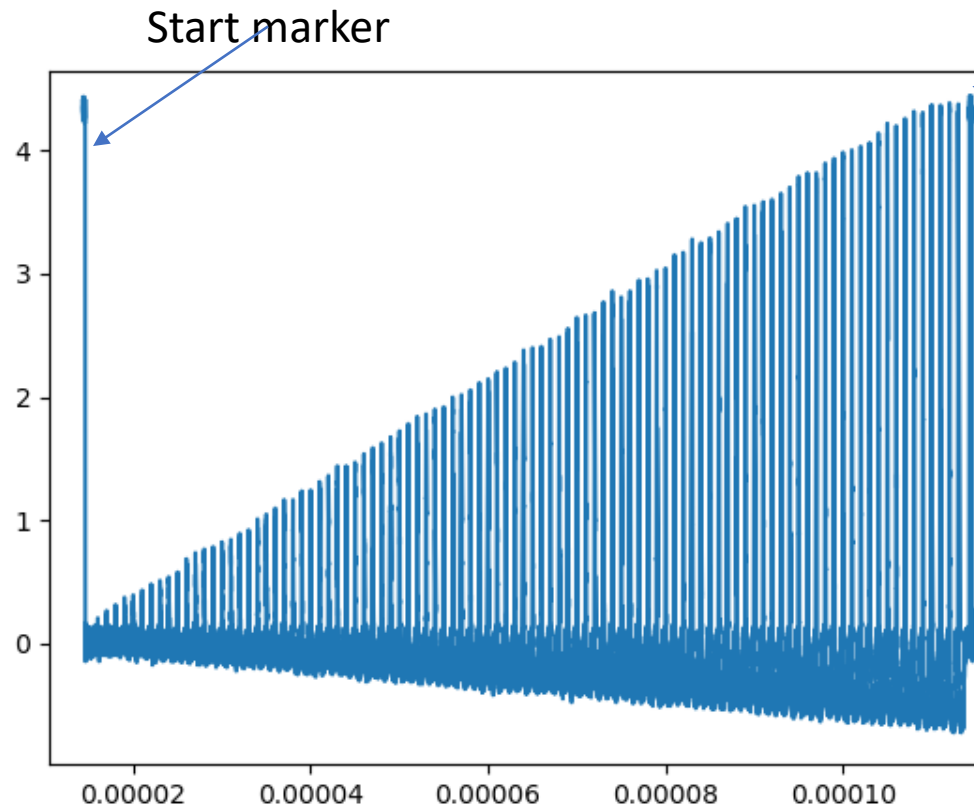


LTSpice simulation

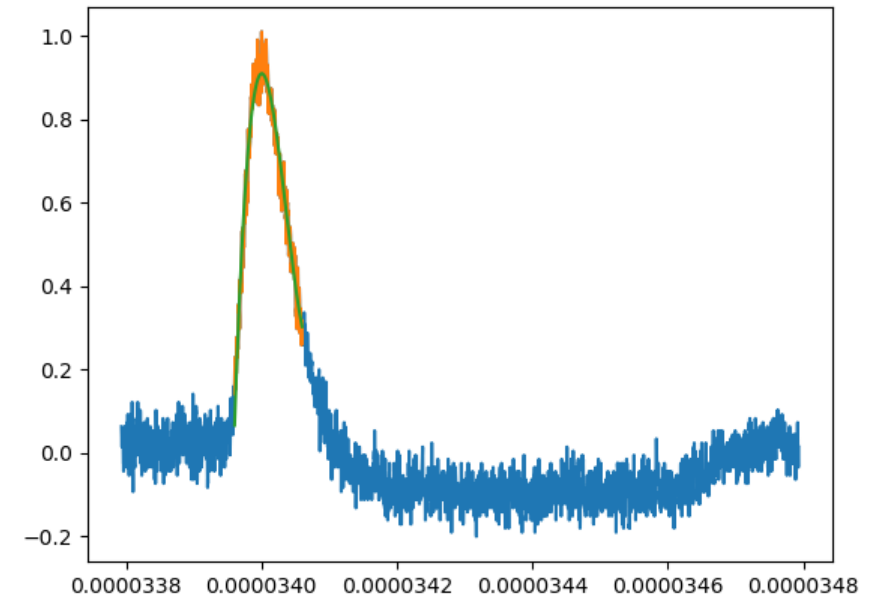


Linearity : measurement technique

- Send a ramp of linearly increasing pulses (100 pulses)
- Fit the peak to a 5th order polynomial
- Find value of max



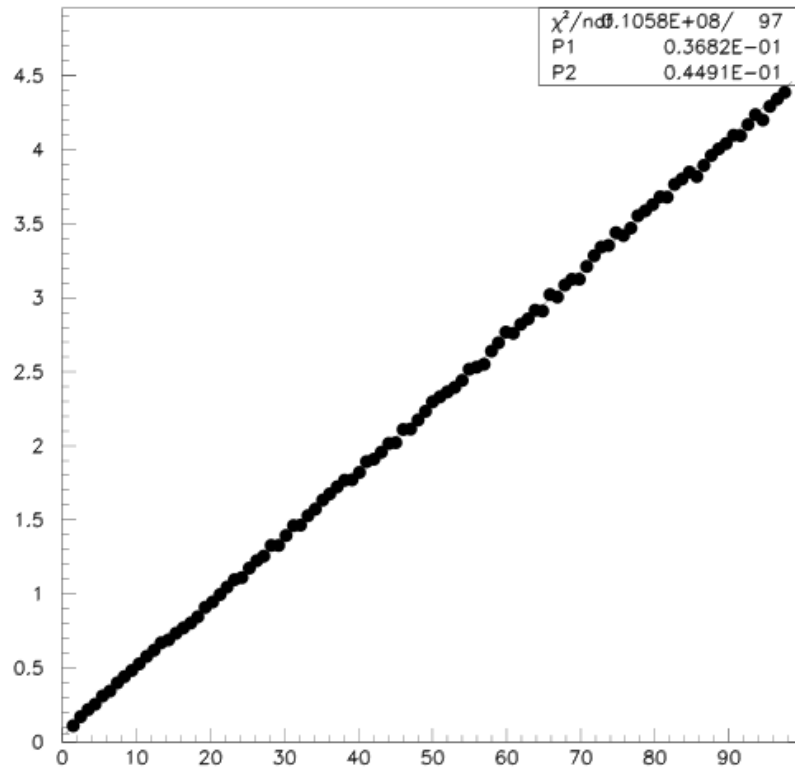
Saturation occurs around 4.5 V on positive lobe : OK



Signal is quite noisy due to poor injection (flying wires)
Not relevant for linearity study

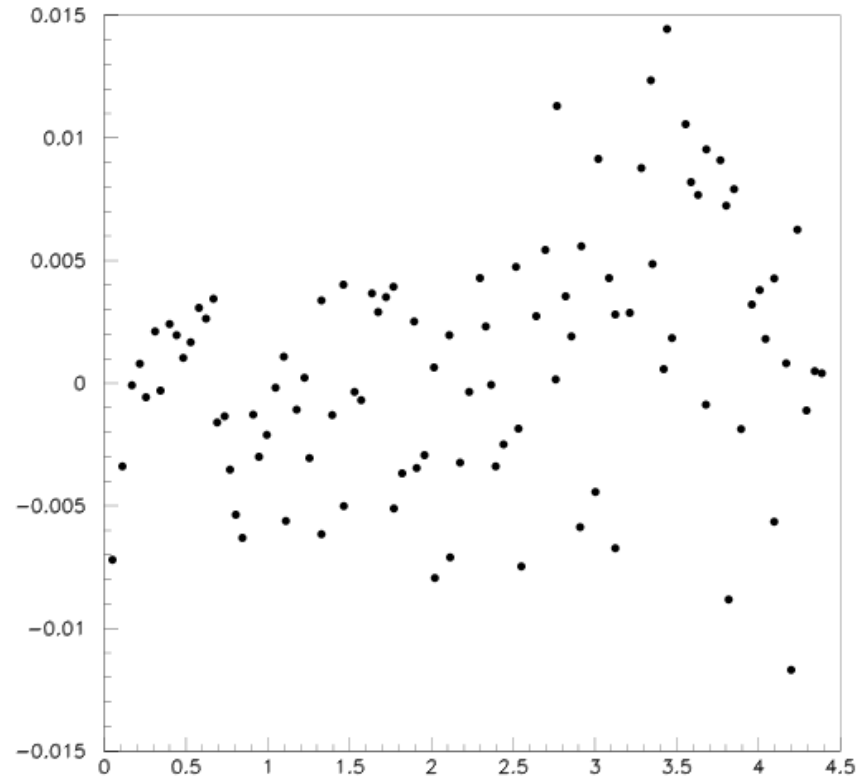
Linearity : result

Pulse amplitude (V)



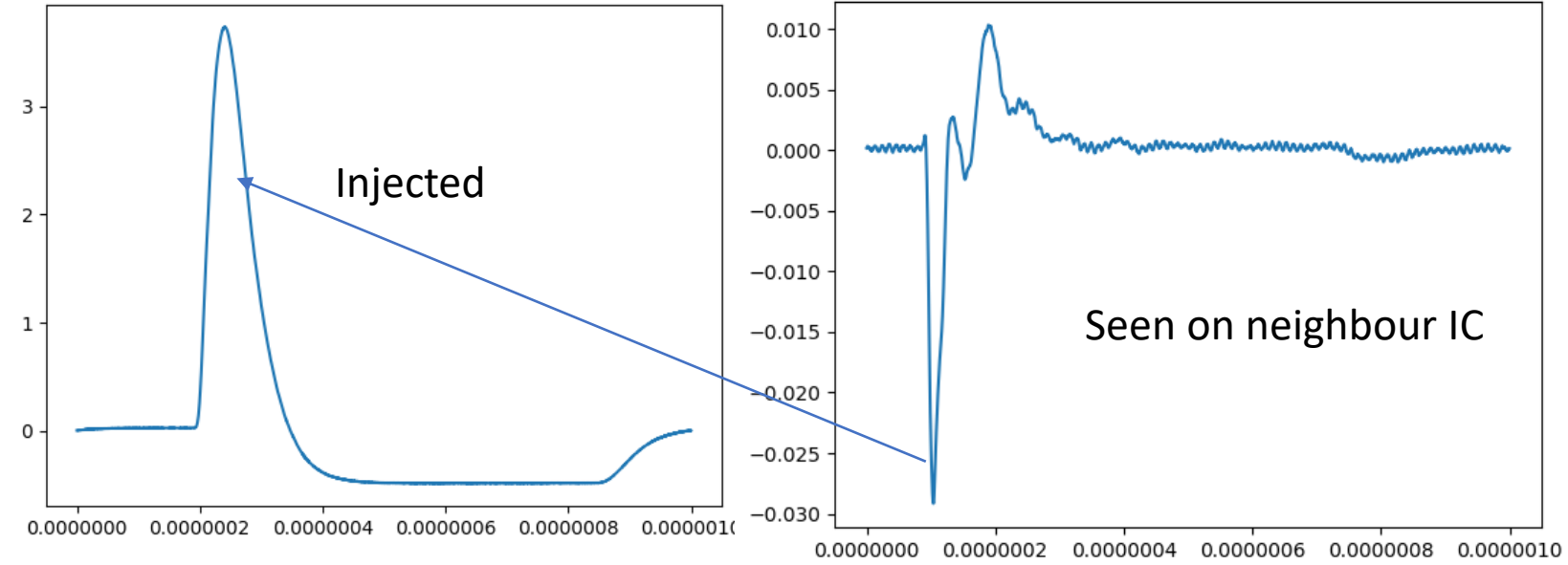
Pulse number

Residuals/4.5 V == INL



Pulse amplitude

Crosstalk measurements



Observed features

- Crosstalk fraction $30/3500=0.9\%$
- Almost same fraction observed between all channels
- Crosstalk is mostly capacitive, i.e. higher at high frequencies

