FEB2 block diagrams

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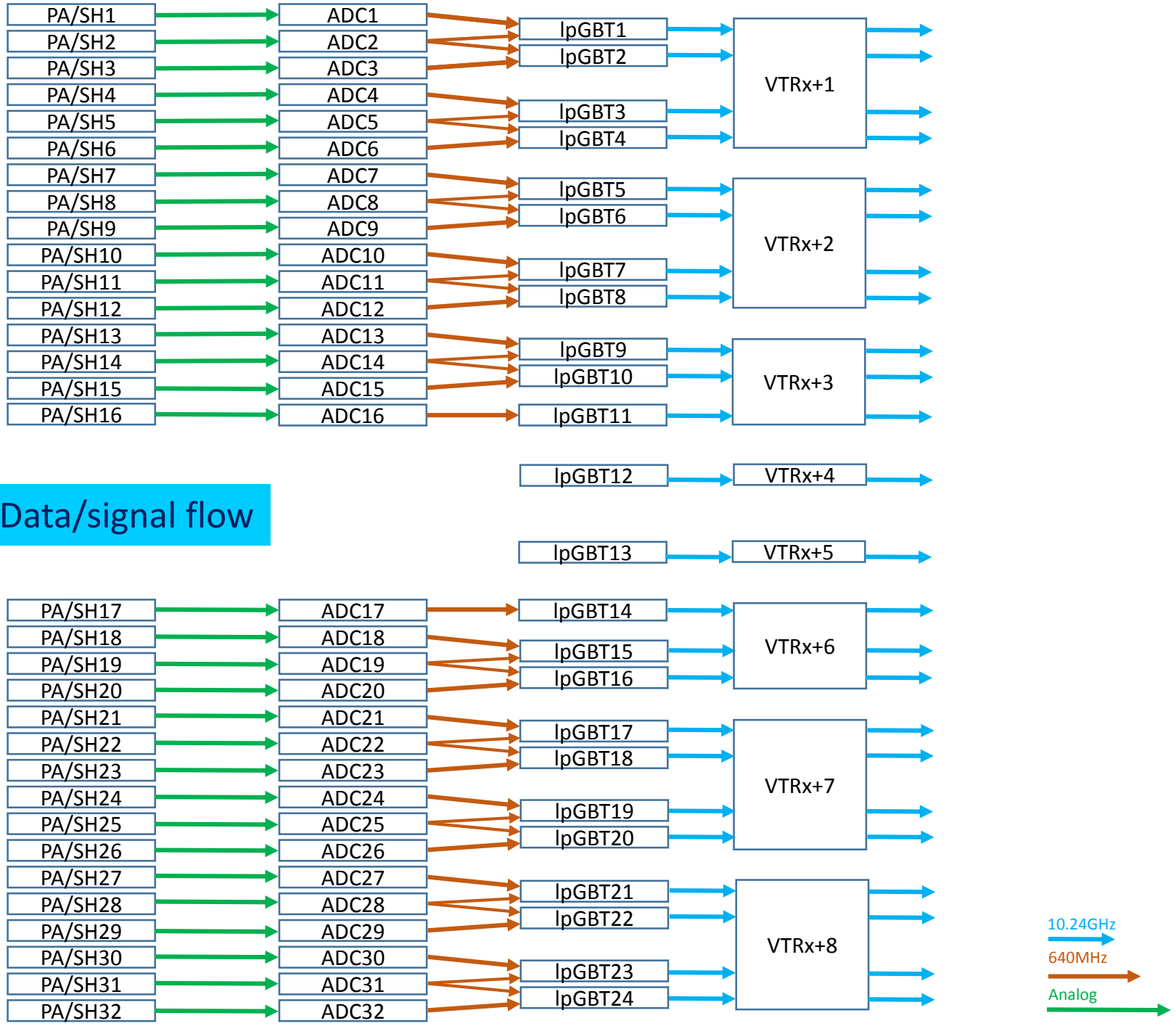
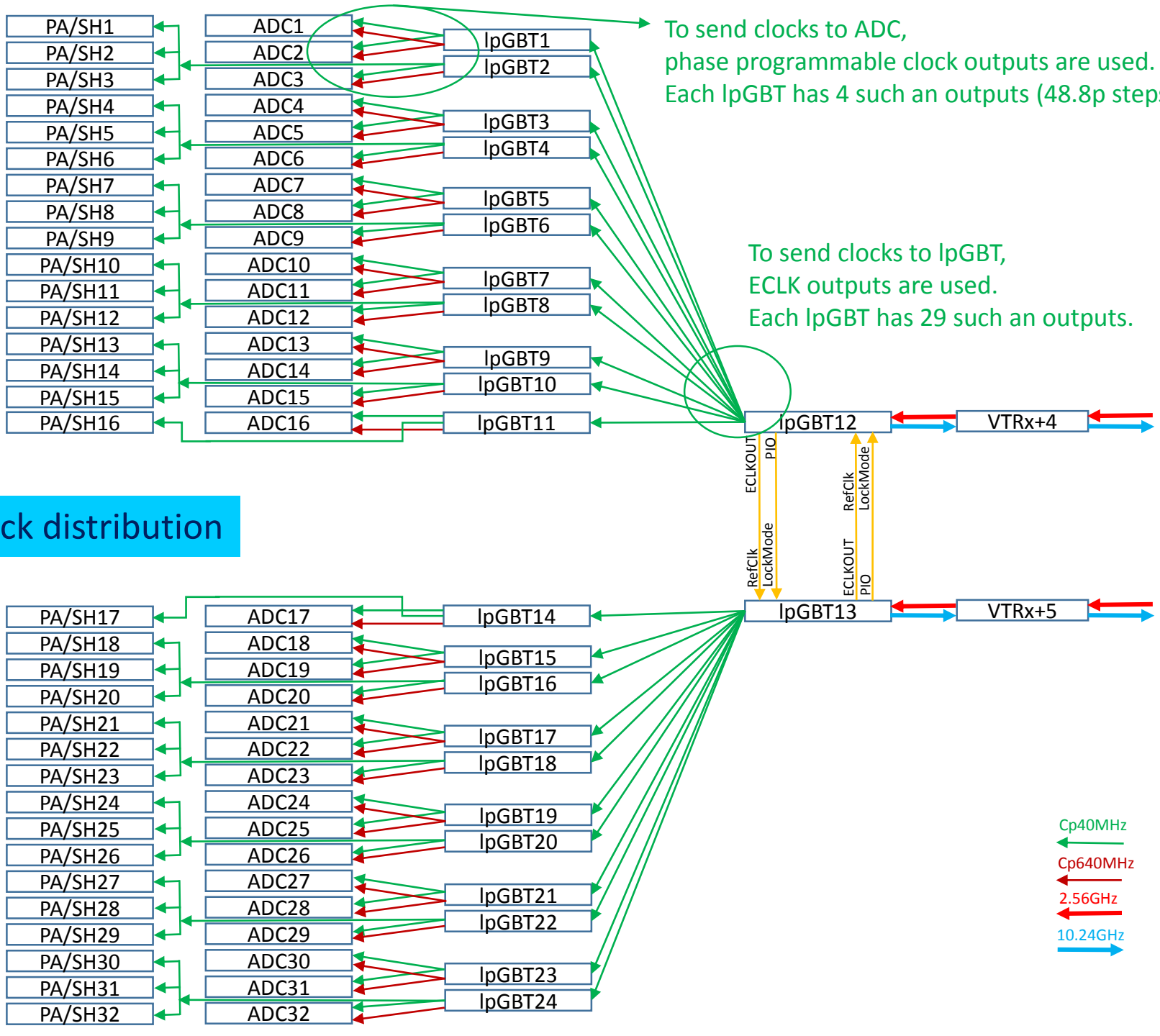
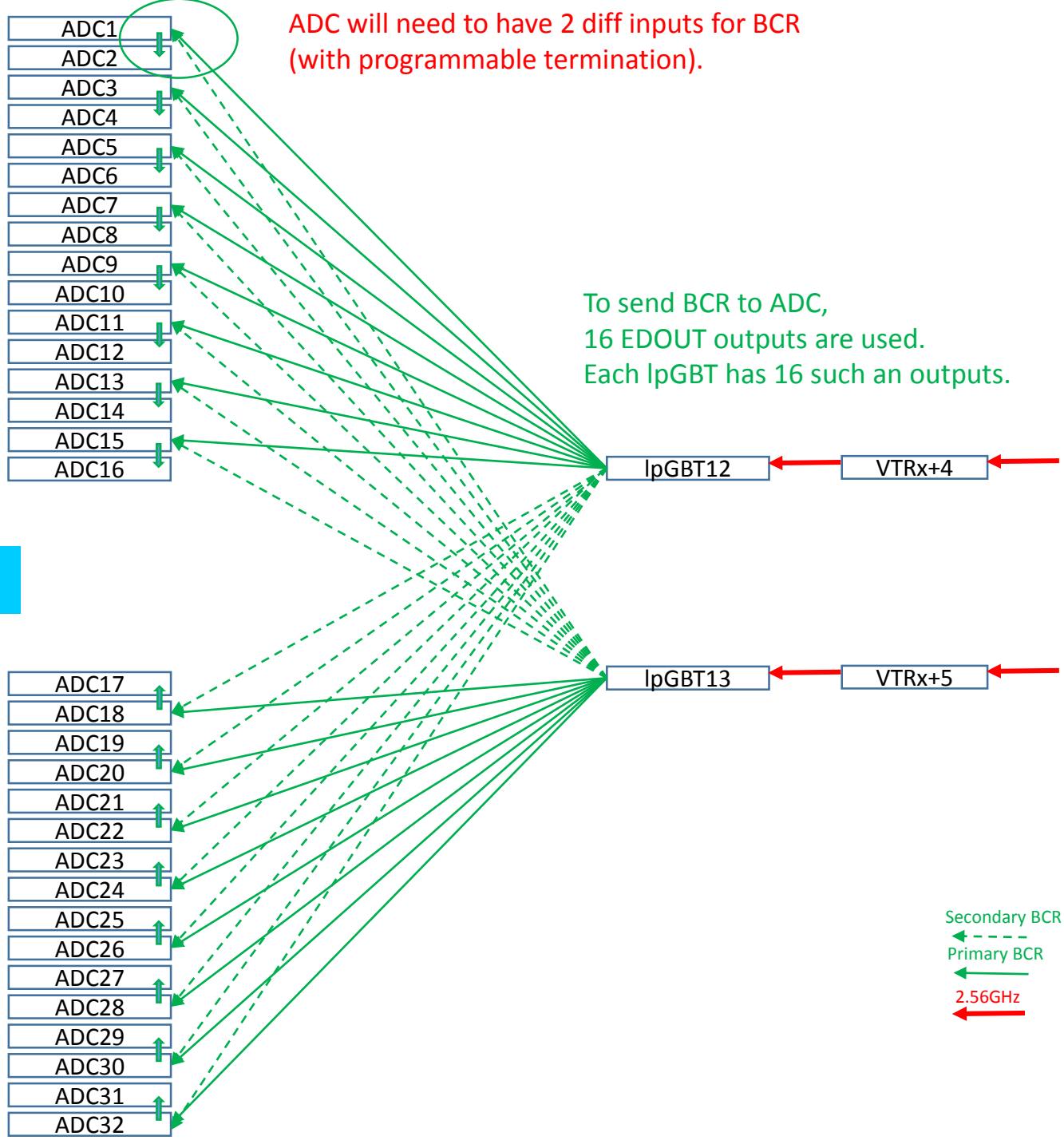
Data/signal flow

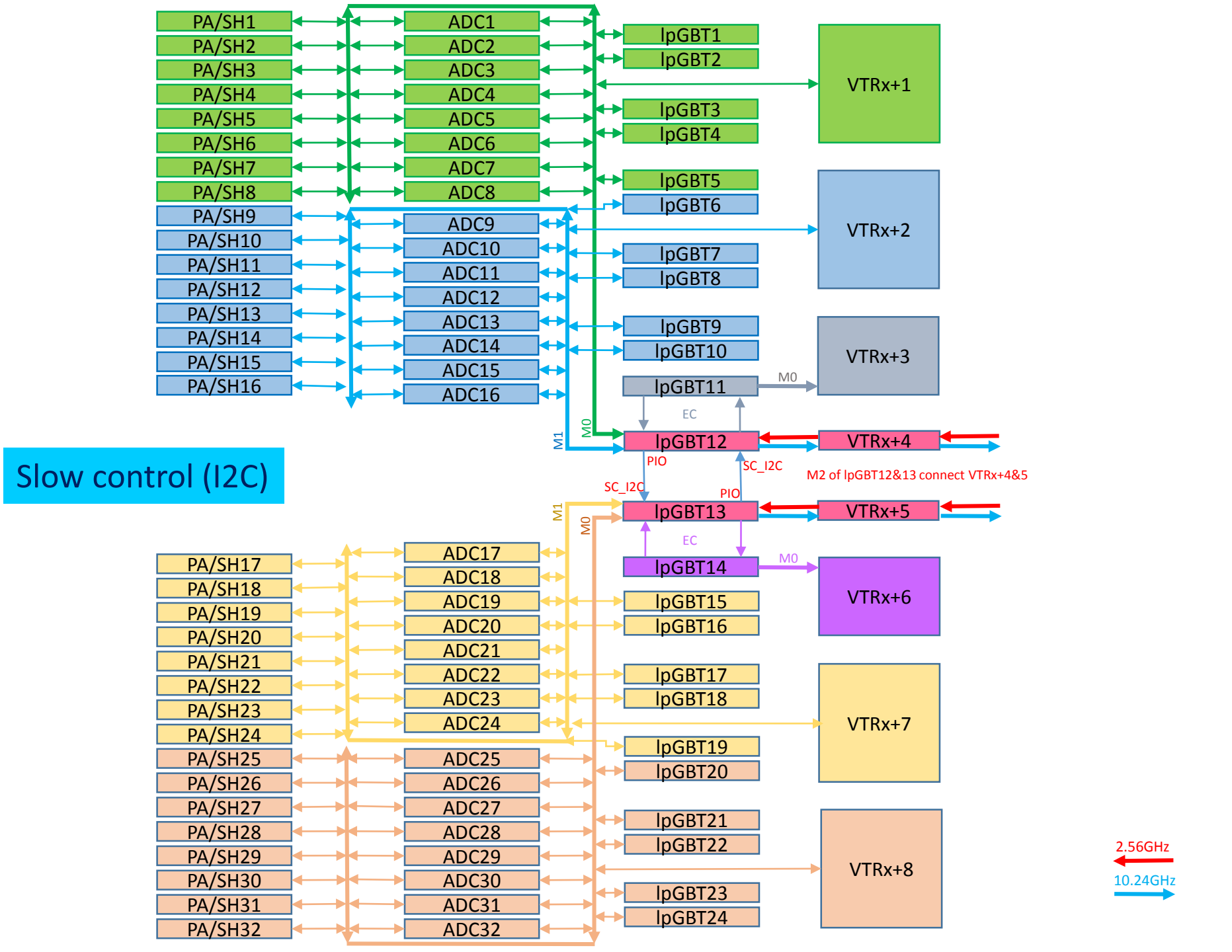


Clock distribution

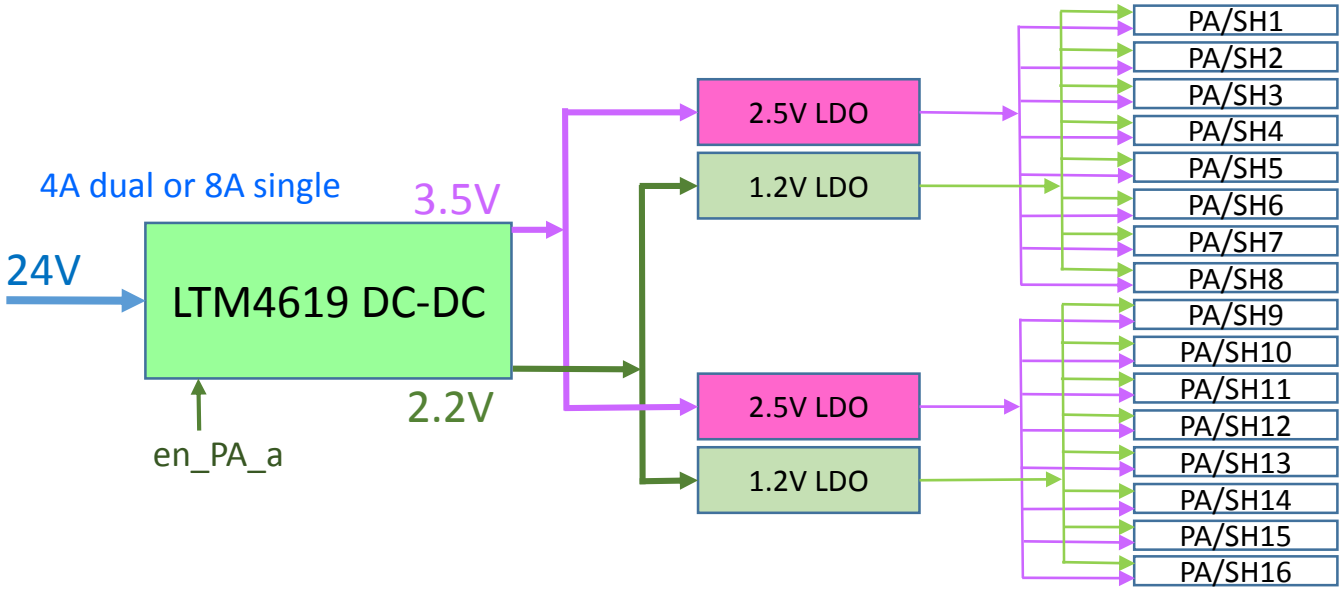


BCR distribution



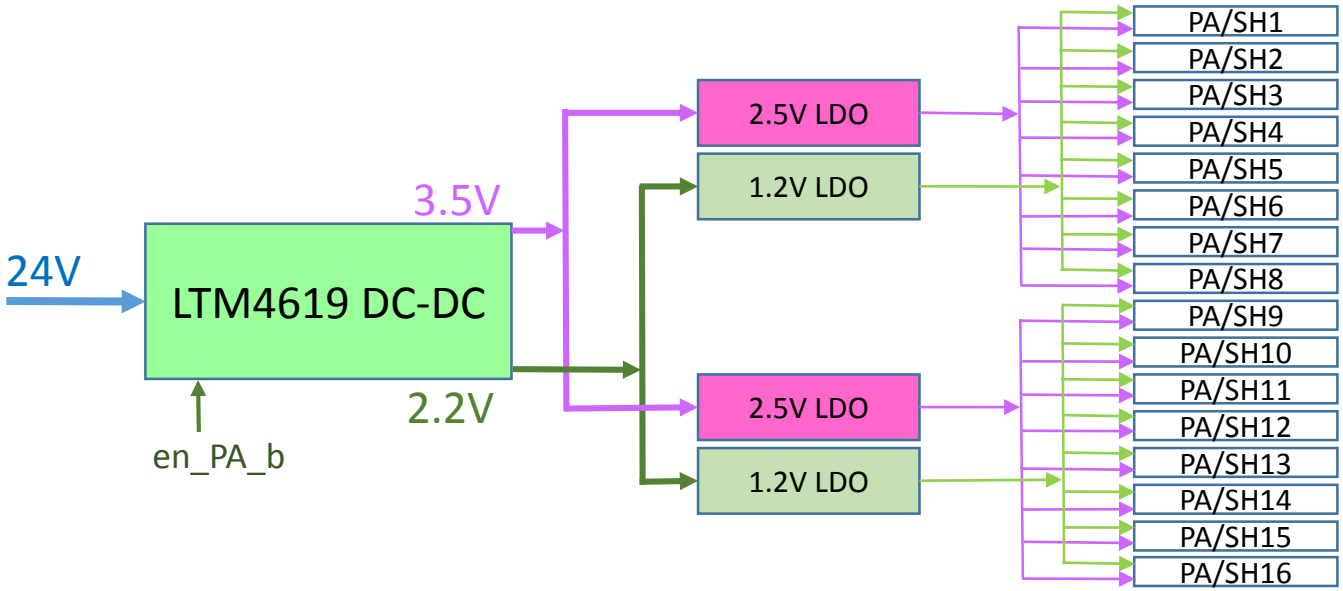


Slow control (I2C)

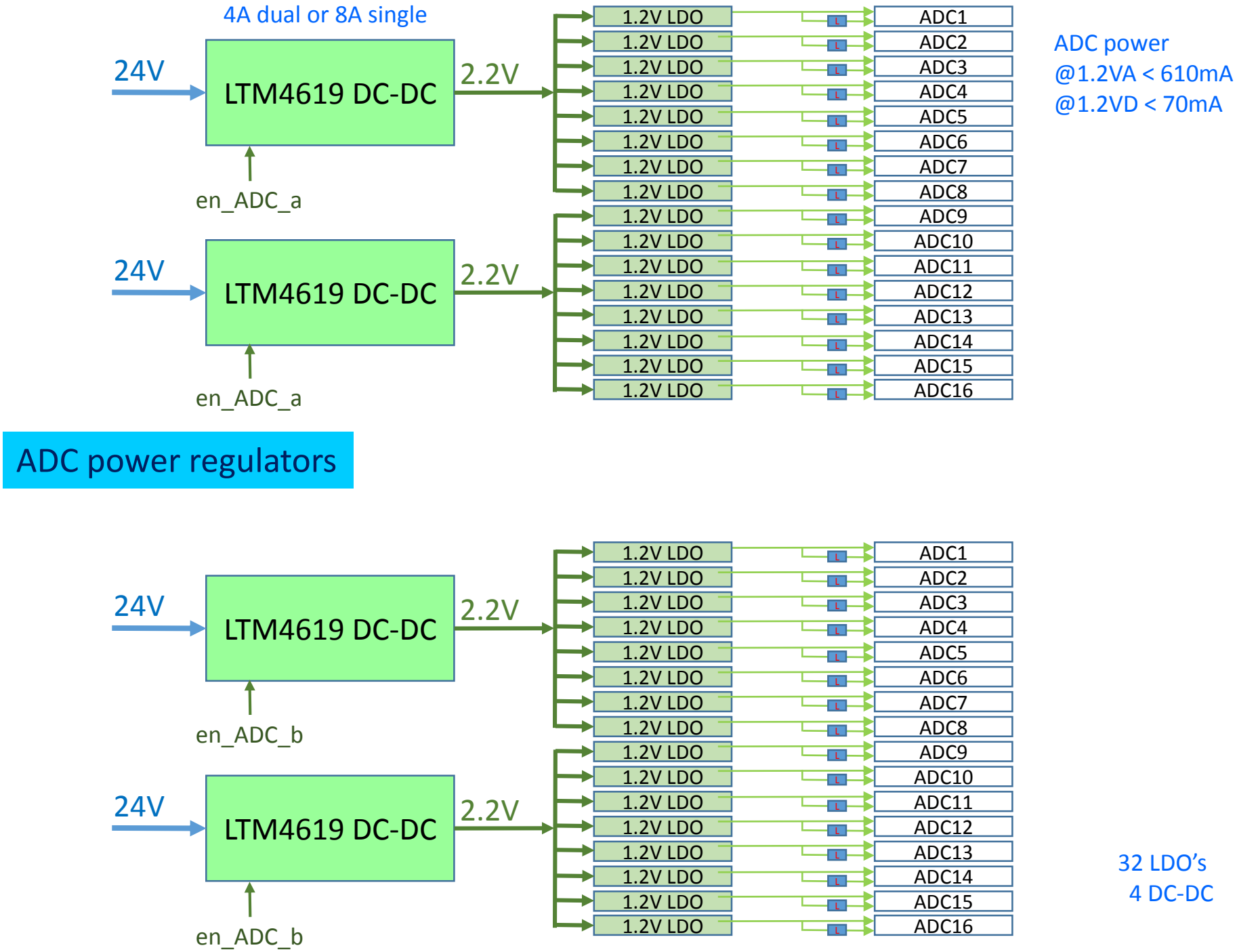


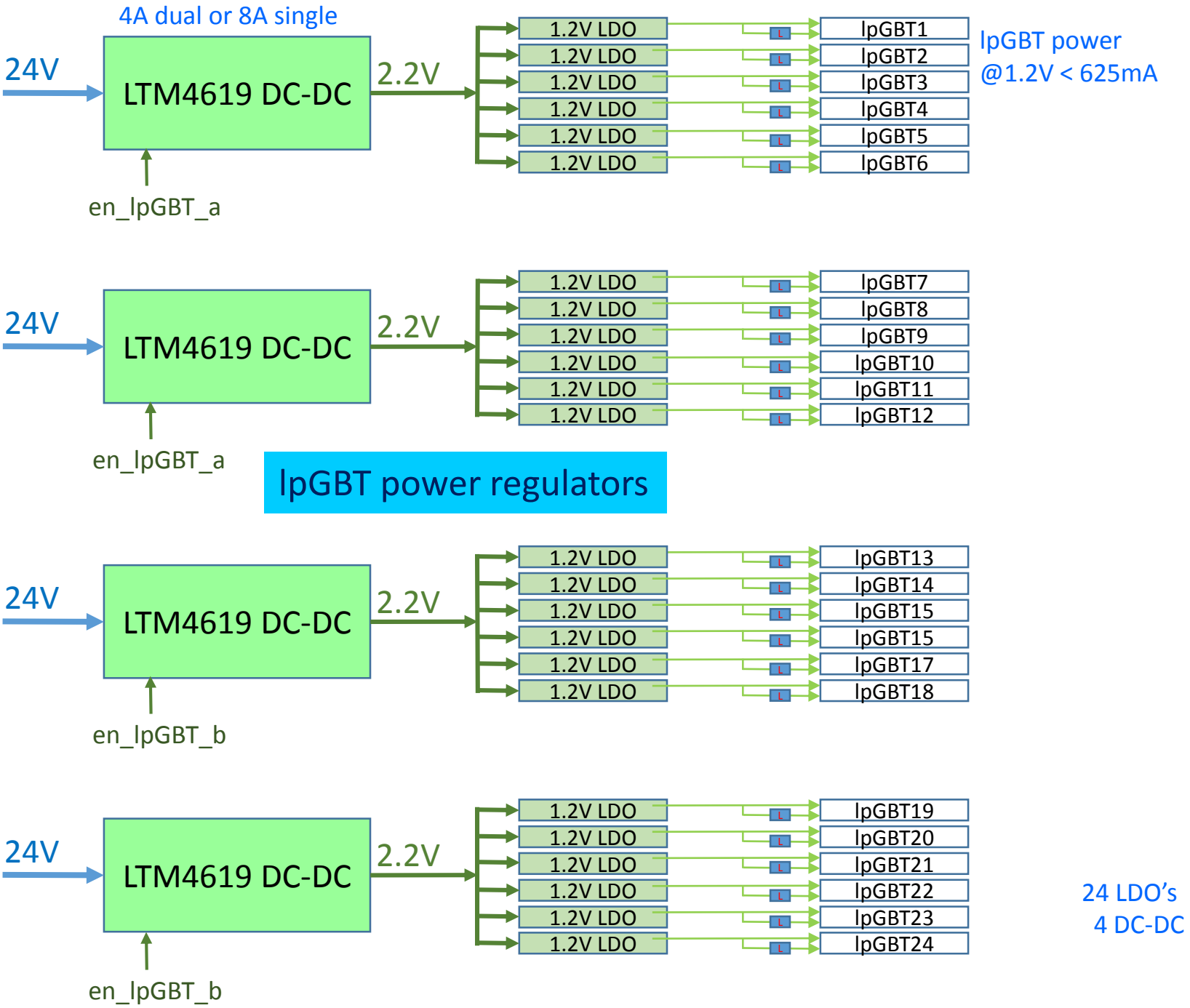
PA power
@2.5V < 100mA
@1.2V < 100mA

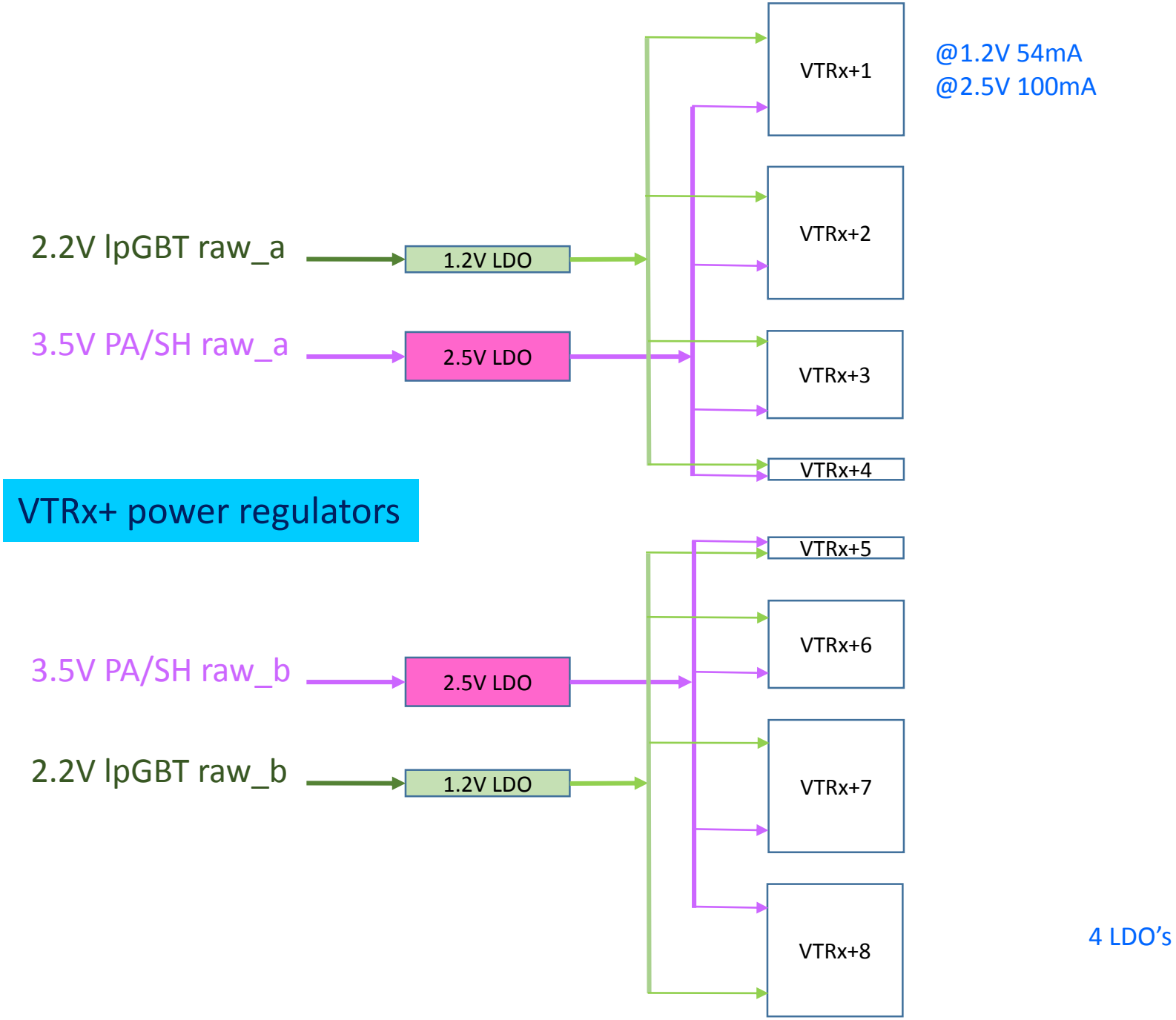
PA/SH power regulators

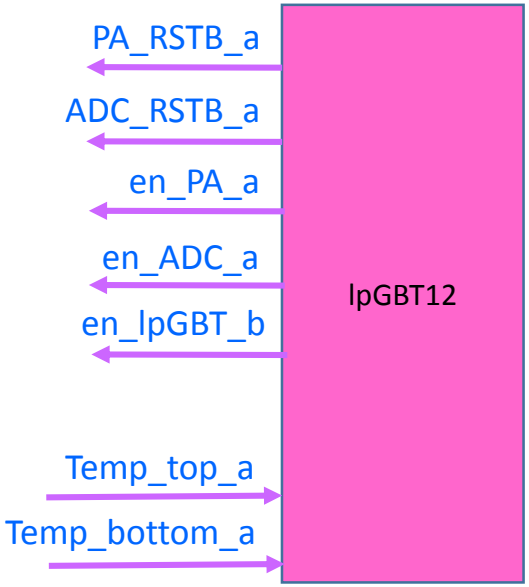


8 LDO's
2 DC-DC


4A dual or 8A single
24V
LTM4619 DC-DC
2.2V
en_ADC_a
24V
LTM4619 DC-DC
2.2V
en_ADC_a
1.2V LDO
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
ADC9
ADC10
ADC11
ADC12
ADC13
ADC14
ADC15
ADC16
ADC power
@1.2VA < 610mA
@1.2VD < 70mA
ADC power regulators
24V
LTM4619 DC-DC
2.2V
en_ADC_b
24V
LTM4619 DC-DC
2.2V
en_ADC_b
32 LDO's
4 DC-DC


4A dual or 8A single
24V
LTM4619 DC-DC
2.2V
en_lpGBT_a
1.2V LDO
lpGBT1
lpGBT2
lpGBT3
lpGBT4
lpGBT5
lpGBT6
lpGBT power
@1.2V < 625mA
24V
LTM4619 DC-DC
2.2V
en_lpGBT_a
1.2V LDO
lpGBT7
lpGBT8
lpGBT9
lpGBT10
lpGBT11
lpGBT12
lpGBT power regulators
24V
LTM4619 DC-DC
2.2V
en_lpGBT_b
1.2V LDO
lpGBT13
lpGBT14
lpGBT15
lpGBT15
lpGBT17
lpGBT18
24V
LTM4619 DC-DC
2.2V
en_lpGBT_b
1.2V LDO
lpGBT19
lpGBT20
lpGBT21
lpGBT22
lpGBT23
lpGBT24
24 LDO's
4 DC-DC

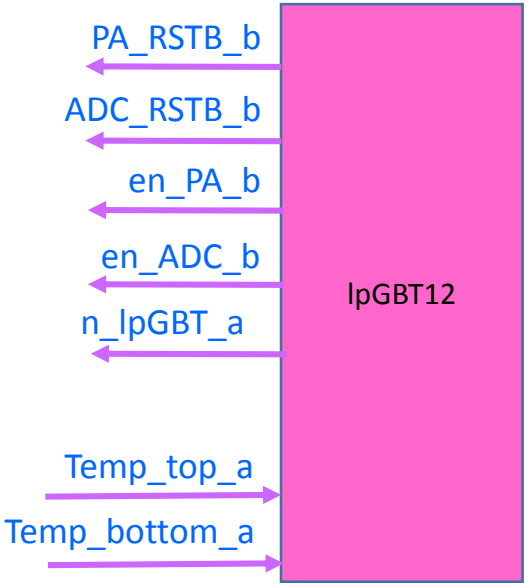

VTRx+ power regulators
2.2V lpGBT raw_a
1.2V LDO
3.5V PA/SH raw_a
2.5V LDO
3.5V PA/SH raw_b
2.5V LDO
2.2V lpGBT raw_b
1.2V LDO
VTRx+1
VTRx+2
VTRx+3
VTRx+4
VTRx+5
VTRx+6
VTRx+7
VTRx+8
@1.2V 54mA
@2.5V 100mA
4 LDO's



To generate resets and enable DC-DC conveters,
PIO pins are used.
Each lpGBT has 16 such an outputs.

To measure the board temperatures,
Internal ADC is used.
Each lpGBT has 7way MUX to ADC.

Slow control & monitoring (1)



Slow control & monitoring (2)

To measure the regulator voltages,
an internal lpGBT ADC is used.
Each lpGBT has 7way MUX to ADC.

Typical PS output measurement scheme.
All PA and ADC power supply
voltages are going to measured.