

# FEB2 Slice Testboard Startup for Board E160398

11-Jan-2021 (v1.0)

Permanent documentation for slice testboard at:

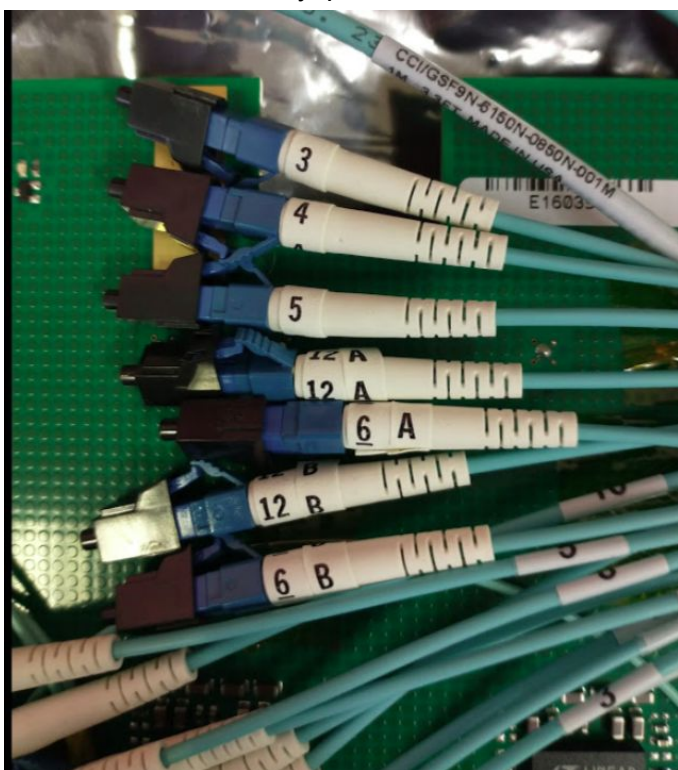
<https://twiki.nevis.columbia.edu/twiki/bin/view/ATLAS/SliceTestboard>

Git Repository for GUI software:

<https://gitlab.cern.ch/dawillia/slice-testboard>

Fiber Mapping for Board E160398

Fibers connected to key IpGBTs were labeled as shown below:



3 = IpGBT11 (COLUTA16 ) uplink

4 = IpGBT16 (COLUTA20) uplink

5 = IpGBT14 (COLUTA17) uplink

12A = IpGBT13 uplink

6A = IpGBT13 downlink

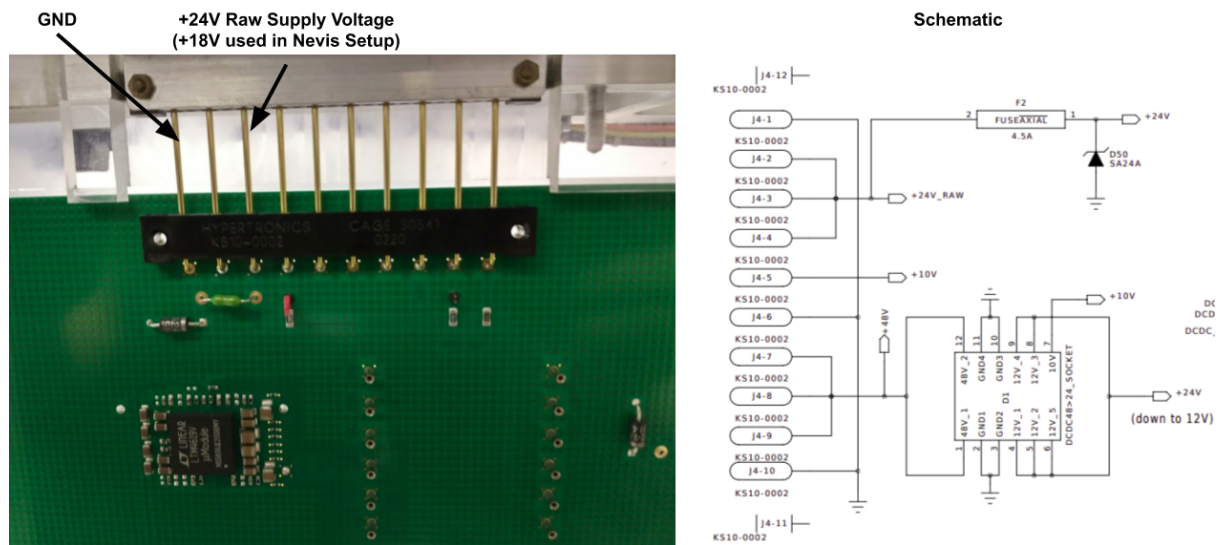
12B = IpGBT12 uplink

6B = IpGBT12 downlink

Note that here COLUTA ADC and IpGBT numbers start from “1”, matching the labels in the board layout and block diagrams (see slide 2):

[https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2\\_block\\_diagrams.pdf](https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2_block_diagrams.pdf)

## Power Connector



For reference the voltage supply connection to the slice testboard as used in the Nevis test setup is shown here.

## GUI Software and Board Configuration

The most up-to-date instructions for using the GUI are posted in the git repository page. A few notes for using this software with board E160398 specifically are provided here.

IpGBTs 12 and 13 on this board have had a minimal set of e-fuses burned to allow configuration over IC on powerup. The LED beside either of these IpGBTs should immediately turn on when their corresponding fiber (listed above) is connected to gigabit link. When this is the case the GUI software should be able to fully configure these IpGBTs, after which it can configure other chips on their respective I2C buses.

There is a set of switches on the side of the board used to enable an external USB device to communicate with IpGBTs 12 and 13 directly without using the FELIX interface. The switches should be down to enable the FELIX interface, which was the state in which the board was sent.

## Basic Startup Procedure

(from slice-testboard repo README)

1. If starting completely from scratch, begin by downloading FLX software from here: <https://gitlab.cern.ch/atlas-tdaq-felix/software>. (If needed, change flx\_setup1.sh to point to the proper paths)
2. Configure the FLX with the proper firmware (it is currently located on flx-srv-atlas and you want the newest version), then reboot (soft reboot - a hard reboot will wipeout the firmware configuration you just did!).

*If the computer is already setup but you just (soft) rebooted, start here!*

3. cd to the ~/FLX/slice-testboard/ directory on flx-srv-atlas and run `source flx_setup1.sh`. This will start the driver, start the FLX, and set up the FLX to send the clock and start to be ready to take data.

*If the computer is already on and configured, start here!*

4. Activate the environment with `conda activate coluta`

5. Run the GUI with `python sliceBoard.py`

6. If you want to take data, run `python takeTriggerData.py` or use the **Take Trigger Data** button in the Data tab of the GUI.

## Configuring the board

1. To configure all chips on the board with their default configuration, press **Configure All** in the Control tab. This takes 4-5 minutes.

2. To configure only specific chips, choose the chip from the drop down menu on the Control tab, and press the corresponding **Configure** button.

*Note:* lpgbt12 must be configured before any other chips on the lpgbt12 side of the board, and likewise for lpgbt13.

3. To write and read specific lpgbt registers, use the drop down menu on the Control tab to select an lpgbt. Enter the register to write/read in hex. If writing, also enter the value to write in hex. If you want to write the same value to more than one consecutive register, or read from multiple consecutive registers, enter the number of consecutive registers as a decimal. Press **Write to LpGBT** or **Read From LpGBT**.

*Note:* If you are switching between data lpgbTs, you will need to do a master reset each time you switch. This can be done with the **Reset IpGBT12/13 I2C Control** buttons.

4. To update a configuration, navigate to the chip using the LAUROC/ COLUTA/ lpgbt tabs. Change the configuration settings, then return to the Control tab and press **Send Updated Configurations**.

### *Configurations for taking Data*

5. By default, COLUTA channels 1-6 come up in Serializer Test Mode, and channels 7-8 come up in normal mode. This can be changed in the COLUTA/Channel/DDPU tab. Additionally, in Channel 1 for each COLUTA there are **Turn On Serialier Mode** and **Turn Off Serializer Mode** buttons, which change serializer mode for all channels.

6. For now, if you want to change between trigger mode and single ADC mode, you'll need to edit takeTriggerData.py directly. Comments in the file indicate which settings are needed for each mode.

## Voltage and Temperature Monitoring

1. To start, configure at least IpGBT12 and Ipgbt13 (you may also configure the whole board, but this will alter the power consumption).

2. Navigate to the Power/Voltage tab. Select the voltages you want to measure (or use **Select All Voltages** to choose all voltages) and press **Read Voltages**. Reading all voltages takes 3-4 minutes.

*Note:* Pending improvement to calibration constants in software - voltage reading may not be exact. Use calculateVREF procedure to determine calibration constants

3. To measure temperatures, navigate to the Power/Temperature tab. Select the temperature points you want to measure (or use **Select All Temperatures** to choose all temperature points) and press **Read Temperatures**. Reading all temperatures will take 2-3 minutes. A temperature reading will appear in celsius.

*Note:* Pending improvement to calibration constants in software - temperature reading may not be exact.

Find board schematics with temperature and voltage points here (*maybe?*):

[https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2\\_slice\\_board\\_schematic.pdf](https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2_slice_board_schematic.pdf)

## Current Monitoring

The following table shows the expected current draw and power usage of the board given an 18V source, at various stages of chip configuration.

Chip	test 1(mA)	test 2	test 3	test 4	Avg (mA)	avg power usage (18V) (W)
nothing	285.6	285.6	285.6	285.6	285.6	5.14
lpgbt12	626.3	626.3	626.6	622.7	625.5	11.26
lpgbt13	1017	1017	1012	1015	1015.3	18.27
lpgbt11	1025	1024	1020	1024	1023.3	18.42
lpgbt14	1019	1022	1018	1018	1019.3	18.35
lpgbt9	1027	1030	1027	1026	1027.5	18.50
lpgbt10	1036	1039	1036	1035	1036.5	18.66
lpgbt15	1047	1049	1046	1046	1047.0	18.85
lpgbt16	1066	1068	1066	1065	1066.3	19.19
coluta16	1136	1139	1135	1137	1136.8	20.46
coluta17	1207	1205	1202	1208	1205.5	21.70
coluta20	1284	1284	1279	1283	1282.5	23.09
lauroc16	1284	1284	1279	1283	1282.5	23.09
lauroc20	1284	1284	1279	1283	1282.5	23.09