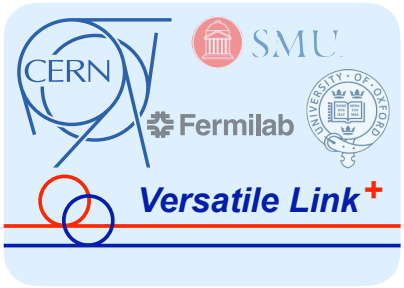

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The Versatile Link+ Application Note

Abstract

This application note describes how to implement a Versatile Link+ system in a typical High Energy Physics experiment. It summarizes the most relevant Versatile Link+ features and available options, and points to the relevant documentation. It guides the optical system designer in his/her engineering effort, highlighting in particular those system aspects that are not directly or fully covered by the Versatile Link+ specification.

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Document History

Rev. No	Date	Pages	Description of Changes
1.0	14 Jan 2019	*All*	First Version
1.1	27 Aug 2019	*All*	Updates based on comments from VL+ project members
1.2	30 Aug 2019	*5*	Updated Irrad Spec title to remove reference to 1 MeV neutrons
1.3	2 Sep 2019	*8*	Updated Samtec FireFly™ CERN-B part numbering scheme
1.4	8 Oct 2019	*4,5,7,8,9,12,13*	various minor updates
1.5	13 Feb 2020	*10, 11*	updated power connection recommendations
1.6	24 Sep 2021	*11*	Added explicit I2C address

Contents

1 Introduction

The Versatile Link+ (VL+) is a bi-directional digital optical data link with up to four upstream channels operating at up to 10.24 Gb/s and one downstream channel operating at 2.56 Gb/s. It has serial data interfaces and is protocol-agnostic, but is targeted to operate in tandem with the Low-power GigaBit Transceiver (lpGBT) serializer/deserializer chip at the front-end, and with a lpGBT core instantiated in an FPGA at the back-end. A block-diagram of the VL+ system is shown in Figure 1. All optical components of the VL+ are multimode and operate at 850 nm wavelength.

The VL+ system is available in two grades of radiation resistance: *standard* and *extended*. The standard grade provides the same radiation resistance as the predecessor Versatile Link components and the extended grade can be used in locations where higher radiation resistance is required. The implementation difference is in the choice of back-end component to provide the required performance to close the optical power budget (see Section 2.2).

This application note is written for teams intending to use the Versatile Link in their experiment, but who were not involved in the project from the beginning. It intends to explain the principles underlying the design of a Versatile Link+ based system and to help them take the relevant engineering decisions.

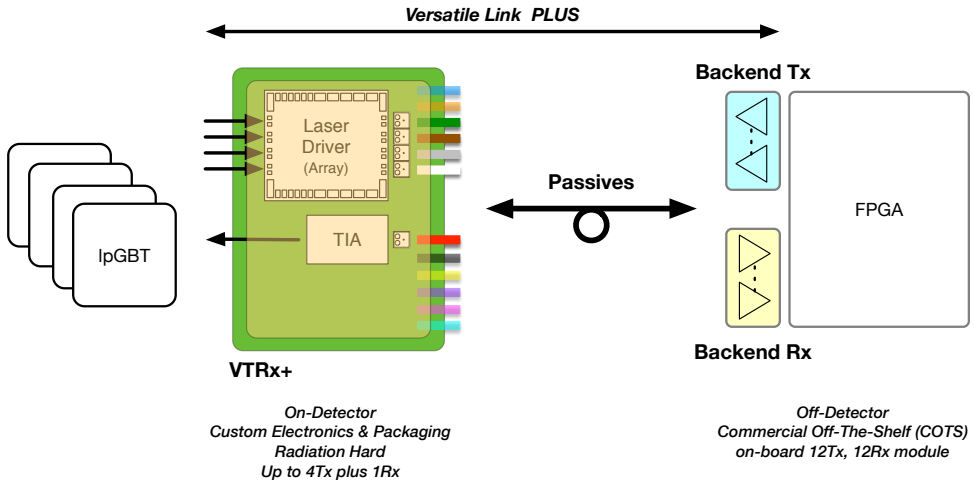

Figure 1: Overview of the Versatile Link+ system showing the components of the Versatile Link+: VTRx+ transceiver, passives, and commercial backend optical transmitters (Tx) and receivers (Rx).

2 Versatile Link Plus Specifications

The VL+ specifications are available to users as a full set of electronic documents from the CERN EDMS server [2]. All components selected to be used as part of the VL+ system must comply fully with these specifications to guarantee that the system will meet its requirements over its entire operating range, over component performance spread, and during the lifetime of the experiment. Users wishing to deviate from the listed specifications are encouraged to contact the VL+ team to discuss the possible impact of non-compliances on operation margins.

2.1 Operational and environmental specifications

The system-level operational and environmental specifications are shown in Table 1, Table 2, and Table 3 below for quick reference. The full specification set must however be used whenever system details need to be investigated.

Table 1: VL+ general specification

#	Parameter	Min.	Typ.	Max.	Unit
3.1.1	Bit Rate (uplink)			10.24[c]	Gb/s
3.1.2	Bit Rate (downlink)			2.56[c]	Gb/s
3.1.3	BER[a]			10^{-12}	
3.1.4	Link length[b]		50	150	m

[a] Test patterns for the BER measurement should be reasonably stressful. Thus PRBS23-1 patterns or longer record lengths are preferred.
[b] Power budget margin for 150 m uplink may be marginal, depending on radiation environment and link speed (see section 2.2).
[c] Test values for validation.

Table 2: VL+ radiation tolerance specifications

#	Tolerance Level	Dose and fluence
4.1.1.1	Standard Grade	1 MGy 1.7×10^{14} neutrons/cm^2 1.7×10^{14} hadrons/cm^2
4.1.1.2	Extended Grade	1 MGy 1×10^{15} neutrons/cm^2 1×10^{15} hadrons/cm^2

Table 3: VL+ temperature specifications(ambient unless otherwise noted)

#	Parameter	Min.	Typ.	Max.	Unit
4.2.1.1	VL+ front-end	-35		60	℃
4.2.1.2	Passives in-detector	-35		60	℃
4.2.1.3	Passives off-detector	0		70	℃
4.2.1.4	Back-end(heatsink)	0		70	℃

2.2 Power budget

The VL+ power budget is calculated in Table 4 for the Standard Grade system and in Table 5 for the Extended Grade system.

Table 4: VL+ power budget: Standard Grade

Standard Grade	**Upstream VTx+→Rx (10 Gb/s)**	**Downstream Tx→VRx+ (2.5 Gb/s)**
Tx OMA (min)	–5.2 dBm	–5.6 dBm
Rx sensitivity (max)	–11.5 dBm	–13.1 dBm
Power budget (min)	**6.3 dB**	**7.5 dB**
Fiber attenuation (max)[a]	0.125/0.25/0.375 dB	0.375 dB
Insertion loss (max)	1.75 dB	1.75 dB
Link penalties (max)[a,b]	1.7/1.9/2.3 dB	0.5 dB
Tx radiation penalty (max)	1.0 dB	NA
Rx radiation penalty (max)	NA	1.4 dB
Fiber radiation penalty (max)	0.5 dB	0.5 dB
Margin (min)[a]	**1.225/0.9/0.375 dB**	**2.975 dB**
Coding gain (min)[c]	1 dB	1 dB

[a] Specified for link lengths of 50/100/150 m.
[b] The link lengths documented here represent the actual link length where the first 7 m consists of radiation hard OM2 fiber. For example, the length of 100 m is an overall link length of 100 m, which includes 7 m of OM2 fiber followed by 100 – 7 = 93 m of OM3 fiber.
[c] Error coding scheme, for example, the lpGBT FEC coding will result in an additional gain in margin.

Table 5: VL+ power budget: Extended Grade

	Upstream VTx+→Rx (10 Gb/s)	**Downstream Tx→VRx+ (2.5 Gb/s)**
Tx OMA (min)	–5.2 dBm	–1.6 dBm
Rx sensitivity (max)	–12.5 dBm	–13.1 dBm
Power budget (min)	**7.3 dB**	**11.5 dB**
Fiber attenuation (max)[a]	0.125/0.25/0.375 dB	0.375 dB
Insertion loss (max)	1.75 dB	1.75 dB
Link penalties (max)[a,b]	1.7/1.9/2.3 dB	0.5 dB
Tx radiation penalty (max)	1.0 dB	NA
Rx radiation penalty (max)	NA	5.4 dB
Fiber radiation penalty (max)	1.5 dB	1.5 dB
Margin (min)[a]	**1.225/0.9/0.375 dB**	**1.975 dB**
Coding gain (min)[c]	1 dB	1 dB

[a] Specified for link lengths of 50/100/150 m.
[b] The link lengths documented here represent the actual link length where the first 7 m consists of radiation hard OM2 fiber. For example, the length of 100 m is an overall link length of 100 m, which includes 7 m of OM2 fiber followed by 100 – 7 = 93 m of OM3 fiber.
[c] Error coding scheme, for example, the lpGBT FEC coding will result in an additional gain in margin.

2.2.1 Saturation of VTRx+ Receivers

The receiver of the VTRx+ will saturate if supplied with an optical signal that exceeds the specified value of 2.0 dBm. This will result in a dramatically increased BER and link failure.

3 Versatile Link+ features and options

The VL+ generic architecture and its implementation options are presented schematically in Figure 1. In its basic configuration, the link is driven by VTRx+ optical transceivers at the on-detector front-end and customised commercial transmitters and receivers at the back-end. Passive components including optical fibers, connectors, fan-out patch-cords, and trunk cables take care of the signal transmission and mapping between the front- and back-ends.

3.1 Front-end components

Whereas the transceivers located at the Versatile Link back-end sit in a standard crate environment, the front-end VTRx+ must withstand radiation, operate in a magnetic field and in many cases be as small and lightweight as possible(see Figure 2). The VTRx+ module developed for the VL+ front-end is thus a full-custom device integrating a radiation hardened transceiver chipset along with a radiation-qualified laser diode array and photodiode. The module was designed to have as small foot-print and thickness as possible while maintaining good optical coupling and electrical connectivity.

Most experiments have asymmetric bandwidth needs in the up- and downstream directions. This typically results in applications requiring many more front-end transmitters than receivers. To cover this need, the VTRx+ uses four up-stream channels at 10.24 Gb/s and one down-stream channel at 2.56 Gb/s, Figure 2. The VTRx+ module can be used in different configurations, depending on user requirements. In case of smaller up-stream bandwidth requirement unused transmitting channels can be disabled by programming the laser driver via I2C and the transceiver then operates in a single Tx/Rx mode. If there is no need for a down-stream connection, the receiver side of the VTRx+ need not be powered and in this case the module operates as a quad-transmitter.

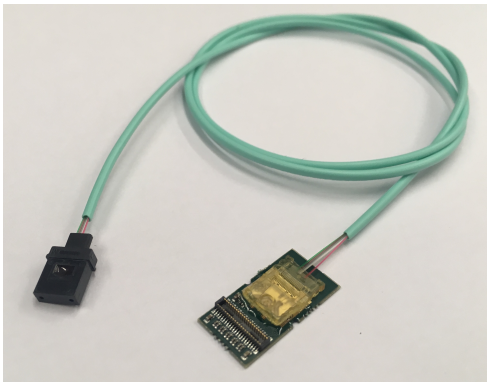

Figure 2: Photograph of a VTRx+ module showing pigtail and MT connector

The VTRx+ module has an optical fibre pigtail as shown in Figure 2. The five individual fibres shown are bundled into a single sheath with outer diameter 1.5 to 2.0 mm (TBD). The minimum bend radius for the pigtail is 10 mm for a single quarter turn (i.e. one 90° bend) and 25 mm for three complete turns. The pigtail length can be chosen from a pre-determined range (TBD) of values when ordering. Each pigtail is terminated with a female MT connector. The female MT does not have guide pins because for an MT-MT connection the guide pins must be added before making the connection since they are retained only by the MT spring clip that unites the two MT connectors. For test systems it is recommended to use an MT-MPO adapter with a male MPO connector for connection to the test system.

3.2 Passive components

The overall cabling scheme of the VL+ is show in Figure 3. The figure contains a number of optional parts that users may implement or not, depending on their needs. A full catalogue of variants for the different elements is in preparation and will be referenced here once it becomes available.

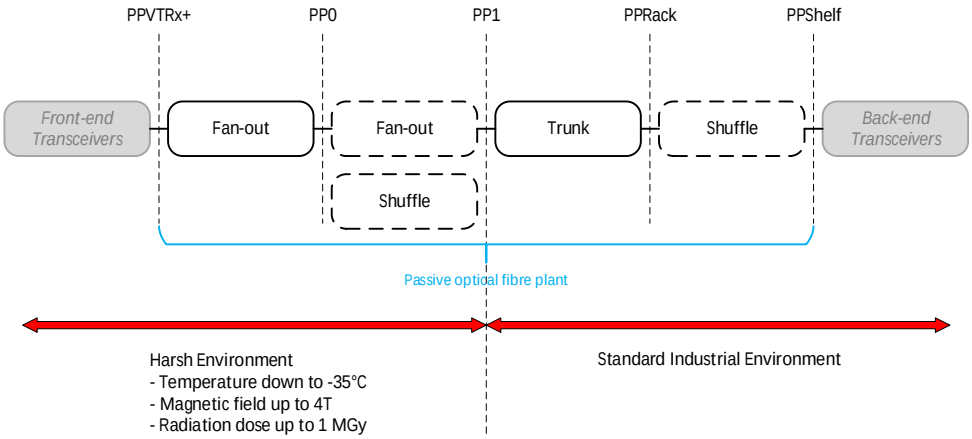

Figure 3: Overview of the different cable elements in the VL+ system.

3.3 Back-end components

Samtec Inc. is the exclusive supplier of Back-end components compatible with the VTRx+ modules, the FireFly™ CERN-B. Three different assembly types are available: 12- or 24-channel transmitter module with pigtail (T12/T24); 12- or 24-channel receiver module with pigtail (R12/R24); and an assembly where the pigtails of one T12 and one R12 module terminate in a single multi-fibre connector (Y12). Furthermore, each assembly type is available in standard (-1) or extended (-2) grade. The part numbers to be used are given in Table 6. Further information regarding the FireFly™ CERN-B module can be found in the product brief[3] and in the datasheet available under NDA by contacting firefly@samtec.com. For information regarding purchasing please contact the Electronics Coordinator of your HL-LHC experiment.

Table 6: Samtec FireFly™ CERN-B Module part numbers for use in VL+ back-end

Assembly type	Standard Grade	Extended Grade
12-channel Tx module	CERN-B-T12-XXX-H-1-F-C	CERN-B-T12-XXX-H-2-F-C
12-channel Rx module	CERN-B-R12-XXX-H-1-F-C	CERN-B-R12-XXX-H-2-F-C
12-channel TRx module	CERN-B-Y12-XXX-H-1-F-C	CERN-B-Y12-XXX-H-2-F-C
24-channel Tx module	CERN-B-T24-XXX-H-1-F-C	CERN-B-T24-XXX-H-2-F-C
24-channel Rx module	CERN-B-R24-XXX-H-1-F-C	CERN-B-R24-XXX-H-2-F-C

(XXX) Assembly length in cm.
(H) Heatsink type: -1 Flat; -2 Pin-Fin; -3 Flat with 3-Ribbon passthrough; -4 High Performance Pin-Fin.
(F) Fibre type: -1 Bare with singulation; -2 Jacketed ribbon; -3 round PVC jacket with strain relief.
(C) Connector type: -M MTP Short Boot Male; -F MTP Short Boot Female (not recommended, since VL+ trunk cable will be terminated with female MTP).

4 VTRx+ mechanical dimensions and electrical connectivity

4.1 Mechanical dimensions

The mechanical outline of the VTRx+ module is shown in Figure 4 and the equivalent 3D rendered version in Figure 5. A representation of the VTRx+ plugged onto its host board is shown in Figure 6.

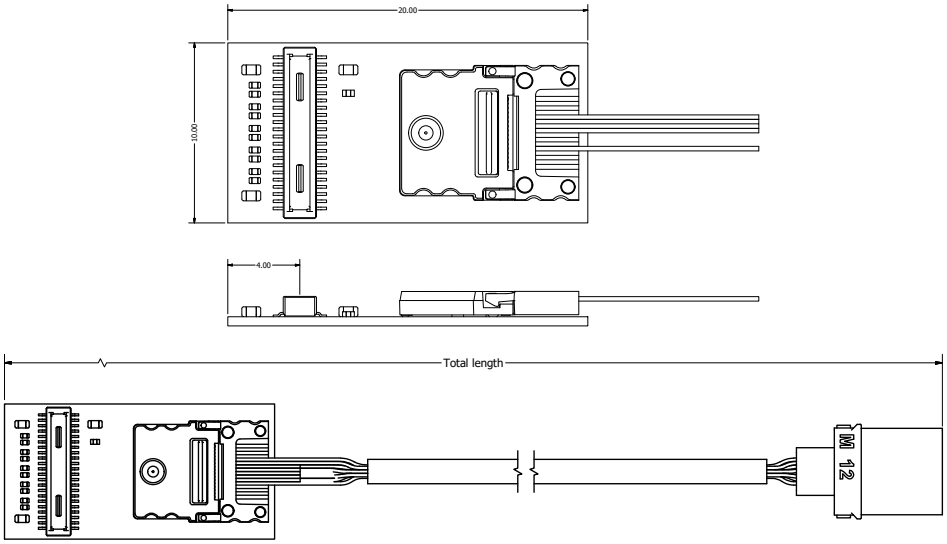

Figure 4: Mechanical dimensions of the VTRx+ module.

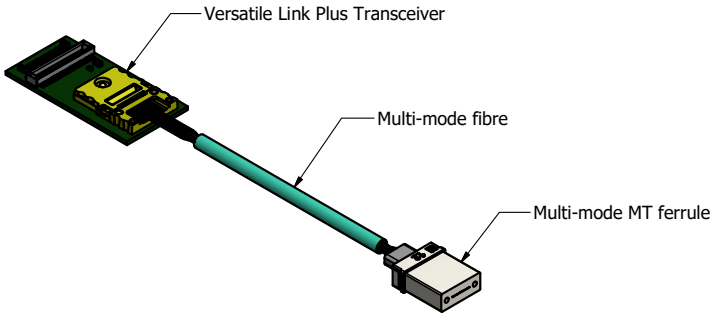

Figure 5: 3D rendering of the VTRx+ module with MT connector.

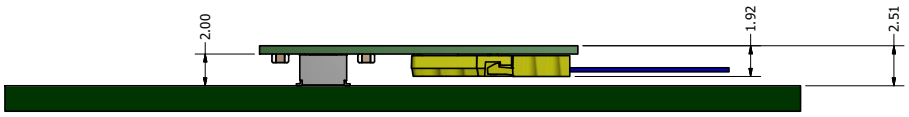

Figure 6: VTRx+ module plugged onto its host board.

4.2 Electrical connectivity

The pin descriptions of the VTRx+ modules are given in Table 7, while Figure 7 shows the pin numbering on the connector. The pinout is arranged so that direct straight connections can be made on the host board

to the lpGBT package. However, there will be an inversion in the Rx path that can be handled either in the configuration of the lpGBT or the Backend FPGA transceiver. When used as a 1Tx + 1Rx transceiver, TX1 should be used to ensure that the optical fibre connections are optimised in the fibre cabling plant.

The electrical connector on the host board is Hirose DF40C-2.0-40DS-0.4V. This connector is rated for 15 mating cycles. Careful handling is required when mating and de-mating the connector to ensure that the male and female parts engage and disengage only perpendicular to the PCB. Twisting and bending will potentially result in damage to the connector itself and its soldering to the boards.

Table 7: VTRx+ module pin numbering and description.

Pin #	Name	Description	Pin #	Name	Description
1	VCCR2V5	2.5V Power supply for TIA	2	n/c	
3	VCCR2V5	2.5V Power supply for TIA	4	RSSI	RSSI current output from TIA, to be pulled up via a resistor to VCCR2V5
5	GND	Ground	6	GND	Ground
7	RXN	Rx $\overline{\text{output}}$	8	SDA	I2C data (to be pulled-up to VCCT1V2)
9	RXP	Rx output	10	SCL	I2C clock (to be terminated to VCCT1V2)
11	GND	Ground	12	GND	Ground
13	TX1N	Tx Ch.1 $\overline{\text{input}}$	14	RSTN	Laser Driver Reset
15	TX1P	Tx Ch.1 input	16	DIS	Laser Driver Disable
17	GND	Ground	18	GND	Ground
19	TX2N	Tx Ch.2 $\overline{\text{input}}$	20	n/c	
21	TX2P	Tx Ch.2 input	22	n/c	
23	GND	Ground	24	GND	Ground
25	TX3N	Tx Ch.3 $\overline{\text{input}}$	26	n/c	
27	TX3P	Tx Ch.3 input	28	n/c	
29	GND	Ground	30	GND	Ground
31	TX4N	Tx Ch.4 $\overline{\text{input}}$	32	TH1	10k Thermistor Terminal 1
33	TX4P	Tx Ch.4 input	34	TH2	10k Thermistor Terminal 2
35	GND	Ground	36	GND	Ground
37	VCCT2V5	2.5V Power supply for Laser Driver	38	VCCT1V2	1.2V Power supply for Laser Driver
39	VCCT2V5	2.5V Power supply for Laser Driver	40	VCCT1V2	1.2V Power supply for Laser Driver

4.2.1 Powering

The module supply voltages (VCCT2V5, VCCT1V2 and VCCR2V5) must be properly decoupled on the host board using an LC filter network as shown in Figure 8. The recommended value of L is between 1uH and 4.7uH. Note that ferrite bead inductors must be avoided if the module is used inside a strong magnetic field. Air-core inductors can be used provided their DC resistance does not exceed 0.6 ohm. In systems powered by radiation tolerant DC-DC converters which typically have output filters containing inductors it may not be necessary to include the additional inductors shown in Figure 8. In such cases any additional inductance

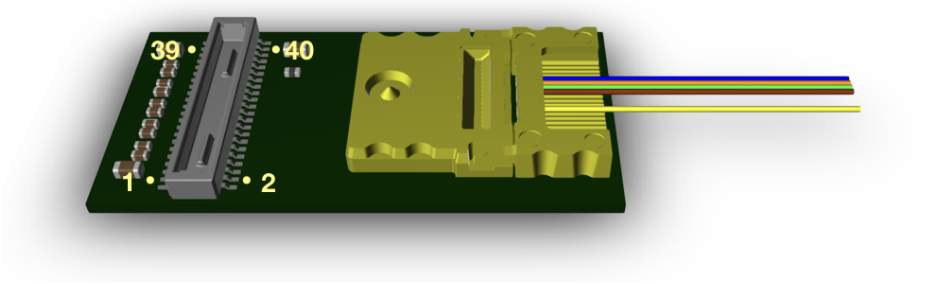

Figure 7: 3D rendering of the VTRx+ module showing pin numbering.

may in fact cause instabilities in the Power Distribution Network (PDN), rather than providing any filtering. It is thus recommended to carry out PDN simulations and/or laboratory evaluations in order to assess the impact of power supply noise on the VTRx+ performance.

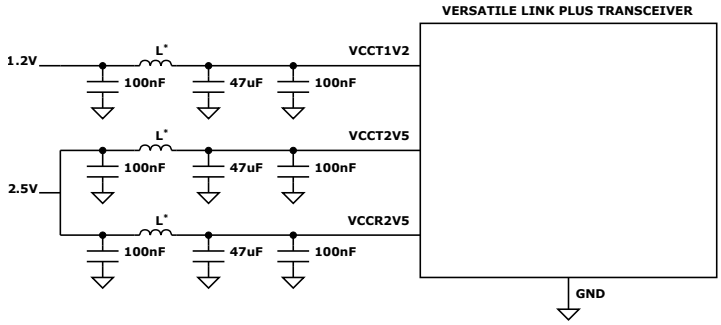

Figure 8: Recommended power connections of the VTRx+ module. See text for recommended values of L

4.2.2 High-Speed Signal connections

The high-speed connections between the SERDES (e.g. lpGBT) and the VTRx+ are implemented using AC coupled differential lines. The DC blocking capacitors are installed on the VTRx+ module. See Figure 9

4.2.3 Control connections

The control interfaces of the VTRx+ module are shown in Figure 10.

The VTRx+ has an I2C interface with fixed address of 0x50 (7-bit address 0b1010000) for the laser driver. This requires a separate I2C bus per module, with pull-ups to VCCT1V2. For normal operation, the laser driver is pre-configured with default laser bias and modulation settings on channel 1. The other channels (2,3, & 4) require programming using the I2C control interface to access the laser driver control registers.

The reset (RSTN) and disable (DIS) pins of the VTRx+ module are internally pulled-up/down so that they can be left unconnected if desired.

The VTRx+ module can provide information about the average optical power of the received light. The RSSI output is a current sink that draws a current equivalent to the average photo current. To use this feature the user must connect the RSSI output of the module to VCCR2V5 using an appropriately sized resistor, R1 (e.g. R1 = 1 kΩ) (see Figure 10 Option A). The resulting voltage on the RSSI pin is VRSSI=VCCR2V5-Iavg*R1, where Iavg is the average photo current. For correct operation the voltage on the resistor should not exceed 2.5V. In case of a voltage sensor with a limited measuring range a voltage divider can be created by connecting RSSI output also to ground with two additional resistors, R2 & R3 (see Figure 10 Option B). For example, with a measurement range of 0 – 1.0 V and VCCR2V5 = 2.5V suitable resistor values are R1 = 4.8 kΩ, R2 = 1 MΩ, and R3 = 470 kΩ.

There is a 10k thermistor on the VTRx+ that can be used to sense the temperature of the substrate using an external current source and ADC (like those present in the lpGBT chip for example). The two terminals of

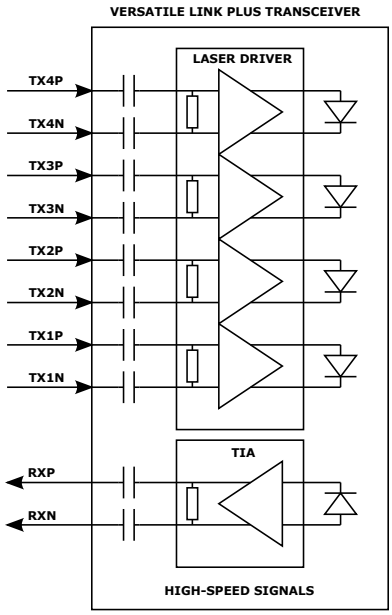

Figure 9: High-Speed connections of the VTRx+ module.

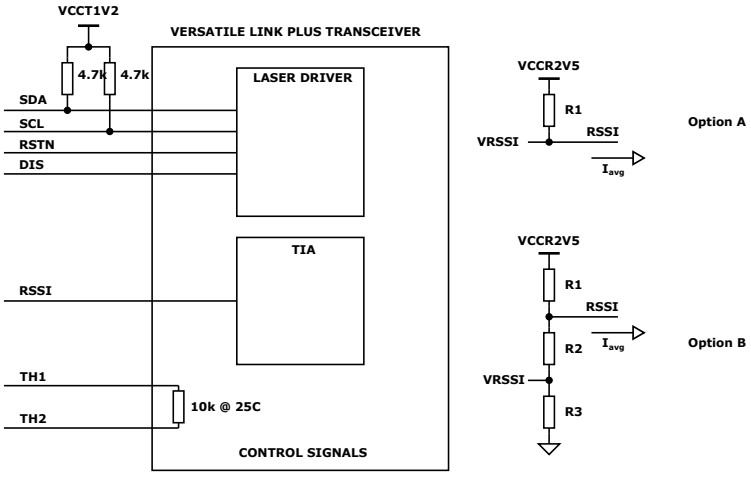

Figure 10: Control connections of the VTRx+ module, showing RSSI connection options.

the thermistor are pins TH1 and TH2. The thermistor part number is TDK NTCG063UH103HTBX which has a resistance of 10 kΩ at 25 ℃ with a maximum operating current of 310 µA.

4.3 Optical connections

The optical pigtail of the VTRx+ is terminated with an MT connector (for pinout see Table 8). When used as a 1Tx + 1Rx transceiver, TX1 should be used to ensure that the optical fibre connections are optimised in the fibre cabling plant. For test systems designed to interface directly to the VTRx+ it is recommenced to use an MT-MPO adaptor with a male MPO connector facing the VTRx+ pigtail. In the final installation the VL+ connection scheme calls for an MT-MT connection, where the two MT connectors are held together using a special spring clip. It is necessary to add guide pins by hand to the MT connectors prior to making this connection. The guide pins are available in metal or ceramic, depending on the application's need for non-magnetic components.

Example instructions for the mating procedure for MT ferrules are available[1].

Table 8: VTRx+ module optical interface pinout.

VTRx+ Function	Fibre Number
RX	7
TX1	6
TX2	5
TX3	4
TX4	3

4.4 Mechanical aspects

It may be desirable to mechanically fix the VTRx+ to the host board in the final application. Different solutions are possible, depending on the space constraints of the application. An example is fixing with a plastic clamp that engages the edges of the VTRx+ PCB (see the example from the CMS Outer Tracker in Figure 11. The VL+ team is available to discuss options.

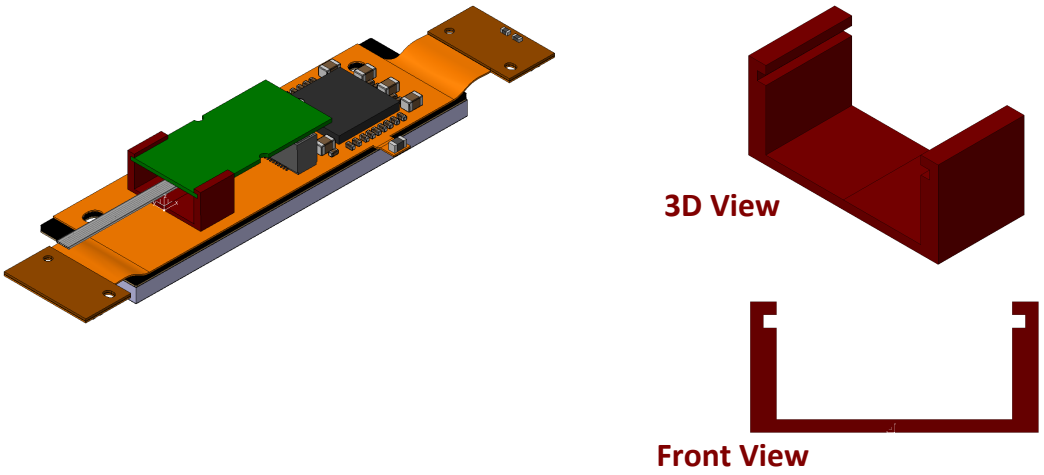

Figure 11: Example implementation of the VTRx+ module in the CMS Outer Tracker showing 3D-printed (or moulded) plastic retention clip.

5 Fibre Handling

Optical fibres can be more fragile than other components if not handled correctly. They are very strong when pulled along the fibre axis, but can be subject to cracking and breaking if bent too tightly. In addition, fibre bending causes optical power loss as the radius is reduced, with light leaking out of the fibre and being lost at the bend.

5.1 Bending losses

As a demonstration, we have performed a small experiment with the fibre pigtail of the VTRx+. Photographs were taken with ever tighter bend radii, with a camera that is sensitive to 850 nm light

6 Documentation

The Versatile Link project documentation can be downloaded from the public page of the collaboration workspace:

`https://espace.cern.ch/project-Versatile-Link-Plus/SitePages/Home.aspx`

The public documents page contains:

- The project proposal and its amendments
- A selected set of project overview presentations
- All material published in peer reviewed journals (and referenced below)
- A link to the project specification repository (including the latest version of this document)

References

[1] USConec AEN-1910. Instructions for mating MT ferrules when using a spring clamp device. `http://www.usconec.com/resources/AEN/AEN-1910.pdf`.

[2] Versatile Link Plus Project Team. Versatile Link Plus EDMS repository. `https://edms.cern.ch/project/CERN-0000149832`.

[3] Versatile Link Plus Project Team. Versatile link plus technical specification, part 2.2: Back-end transceiver.