FEB2 "Slice" Testboard Update

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on behalf of Columbia (Nevis Laboratories)

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NEVIS LABORATORIES
COLUMBIA UNIVERSITY

ATLAS
EXPERIMENT

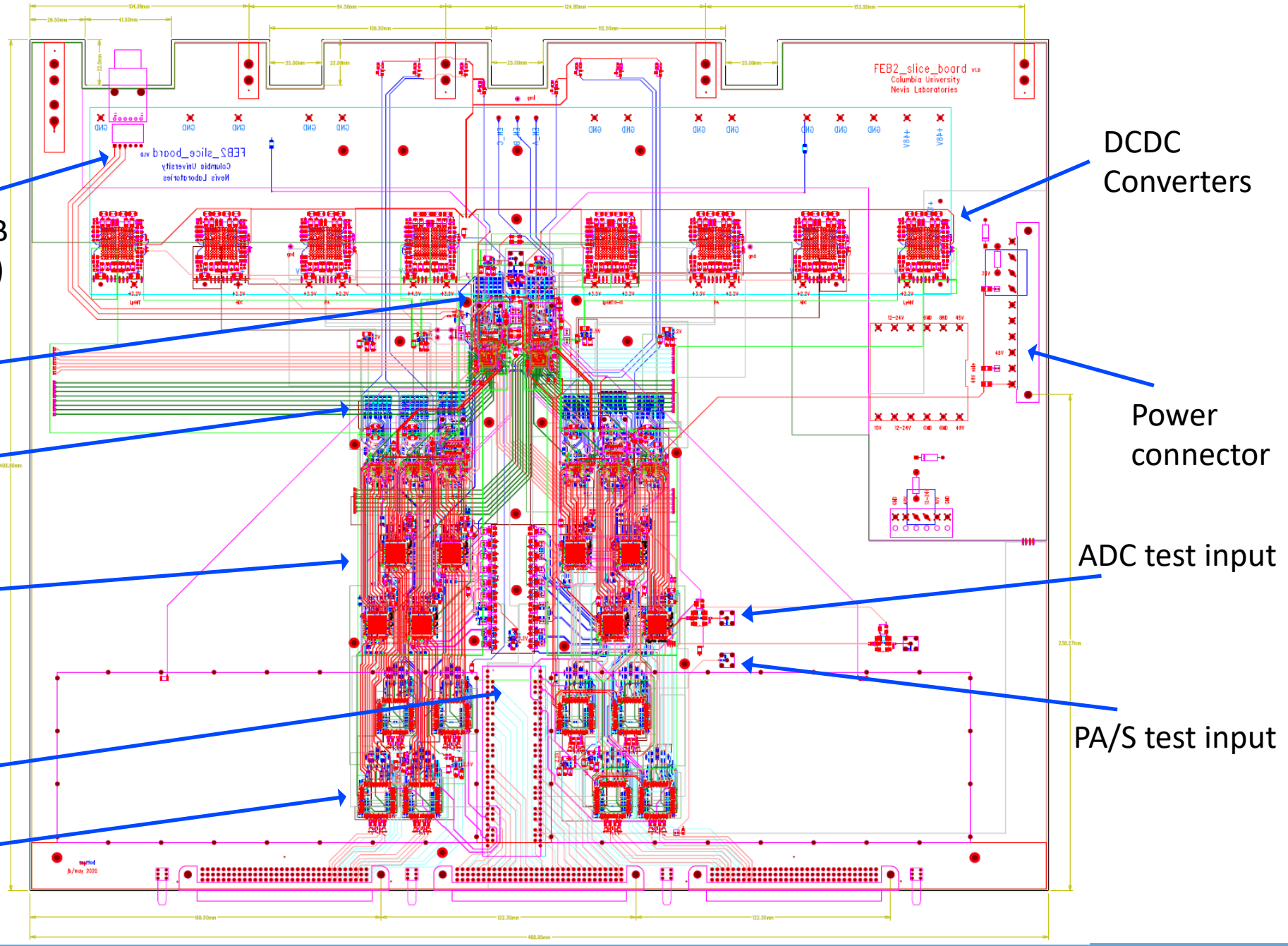
Overview

- Analog Testboard (2019)
  - 2 (LAUROC1 PA/S + COLUTAv2 ADC) + lpGBT
  - Verified full readout chain PA/S + ADC + optical data links
- Slice Testboard (2020)
  - 8 (LAUROC2/ALFE1B PA/S + COLUTAv3 ADC + lpGBT) chips, 32 LAr channels available
  - Aim to demonstrate multichannel performance, bi-directional control links
- Full FEB2 Prototype (2021-2022)
  - All 128 channels

Slice Testboard Design

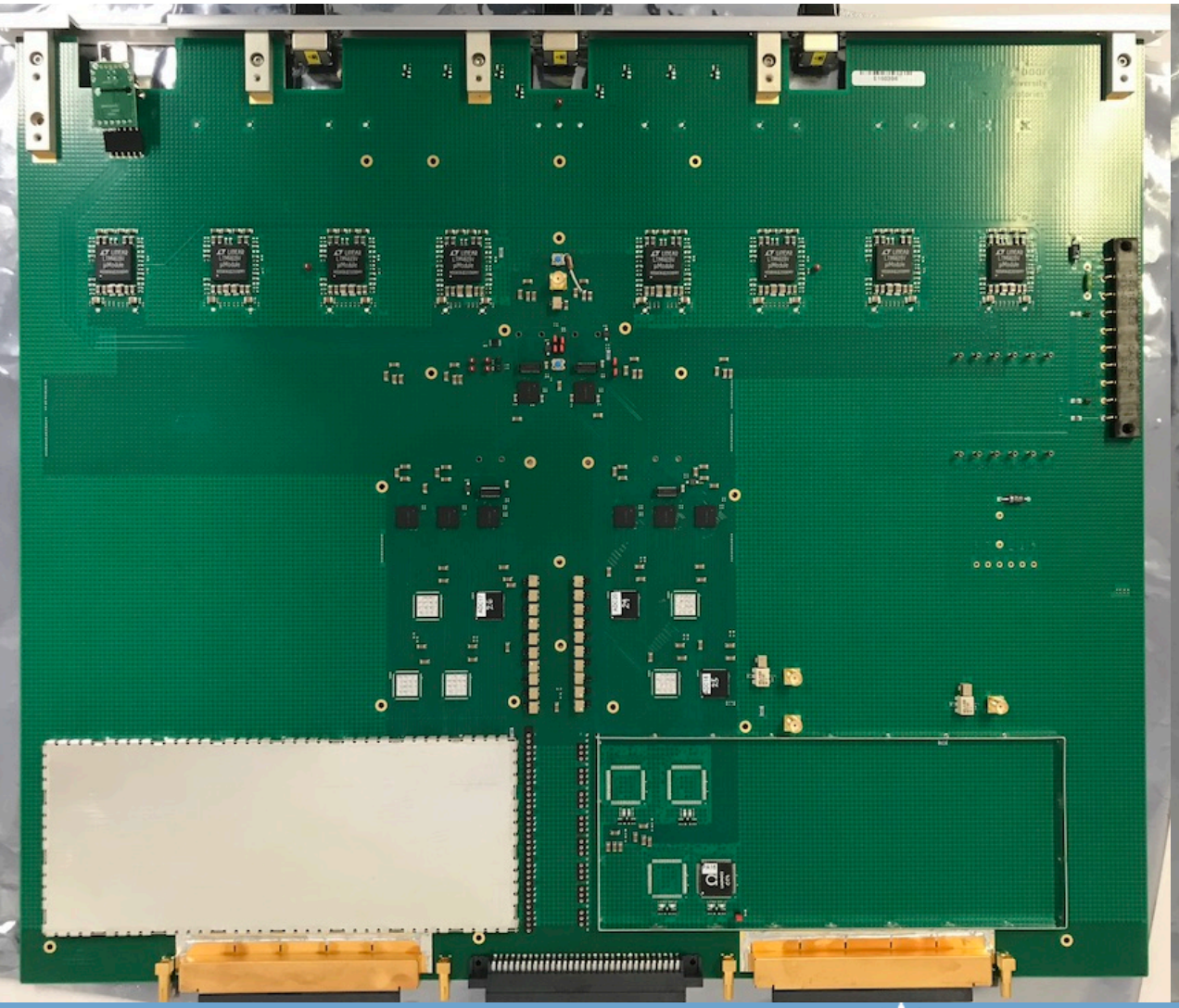
- The Slice Testboard represents a central “slice” of the final FEB2 board (block diagrams on following slides), using the full FEB2 architecture:
  - Integrates latest version of the PA/S (including I2C control, L1 trigger sums) and ADC (including full 8 channel/ chip density and on-chip Vrefs)
  - Scales up to a 32 channel read out (compared to 2 channel read out on analog testboard)
  - Includes redundant bi-directional control/ monitoring using lpGBTs
  - Includes VTRx+ for data and control links
  - Includes 3 variations of rad-tol power scheme
  - Fabricated using halogen free materials (special design requirements)

Slice Testboard Layout

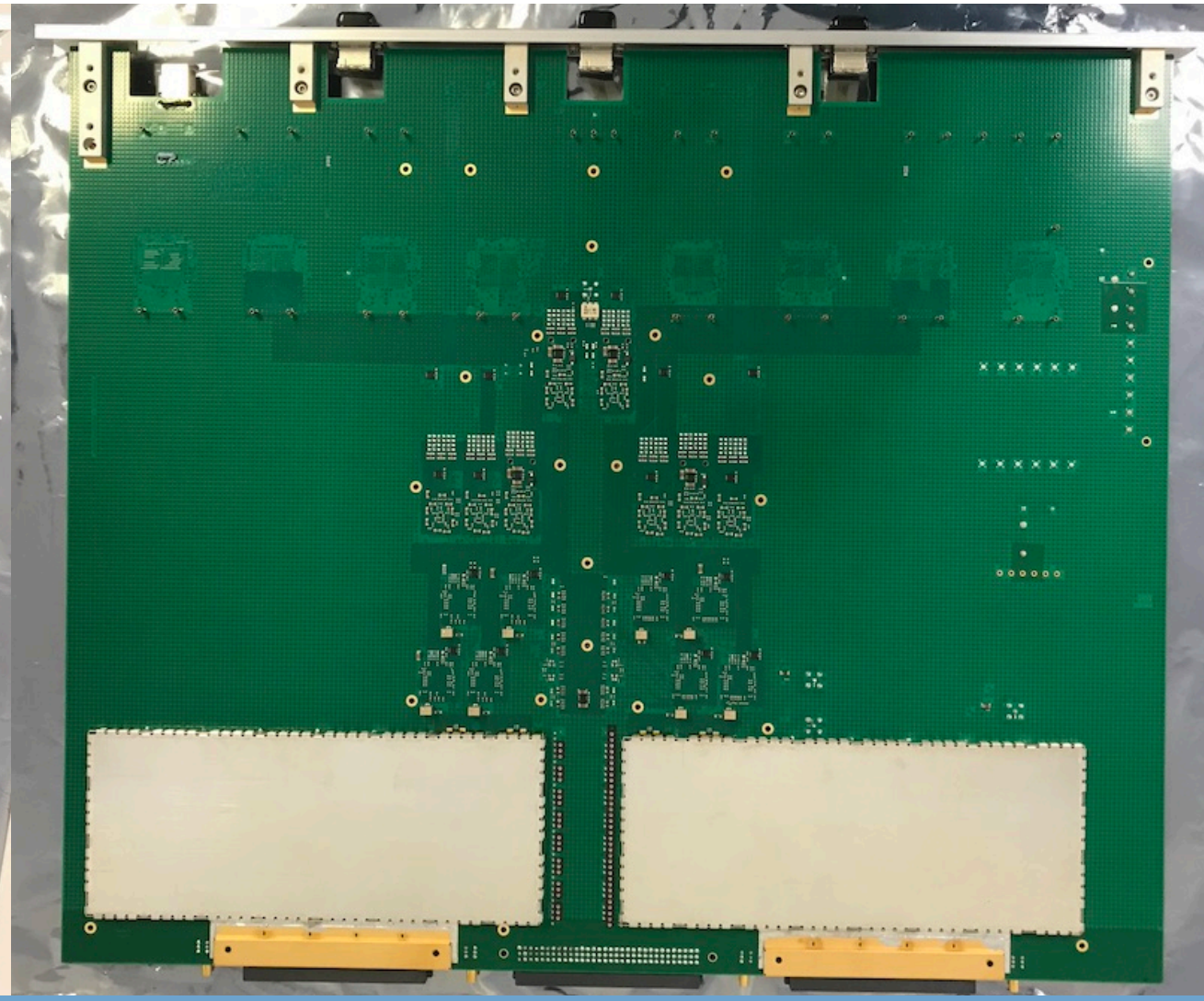


Slice Testboard Layout

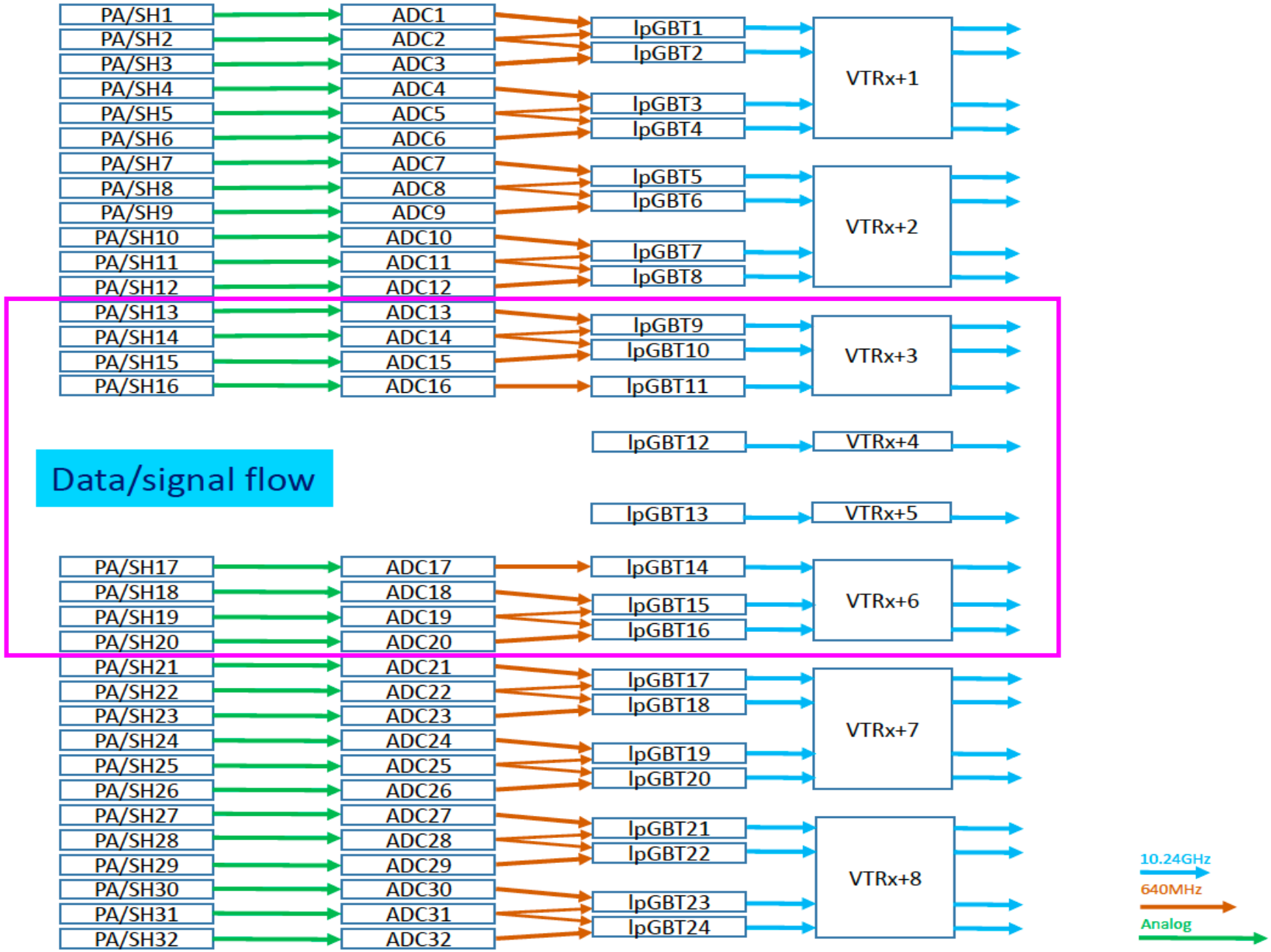
Front



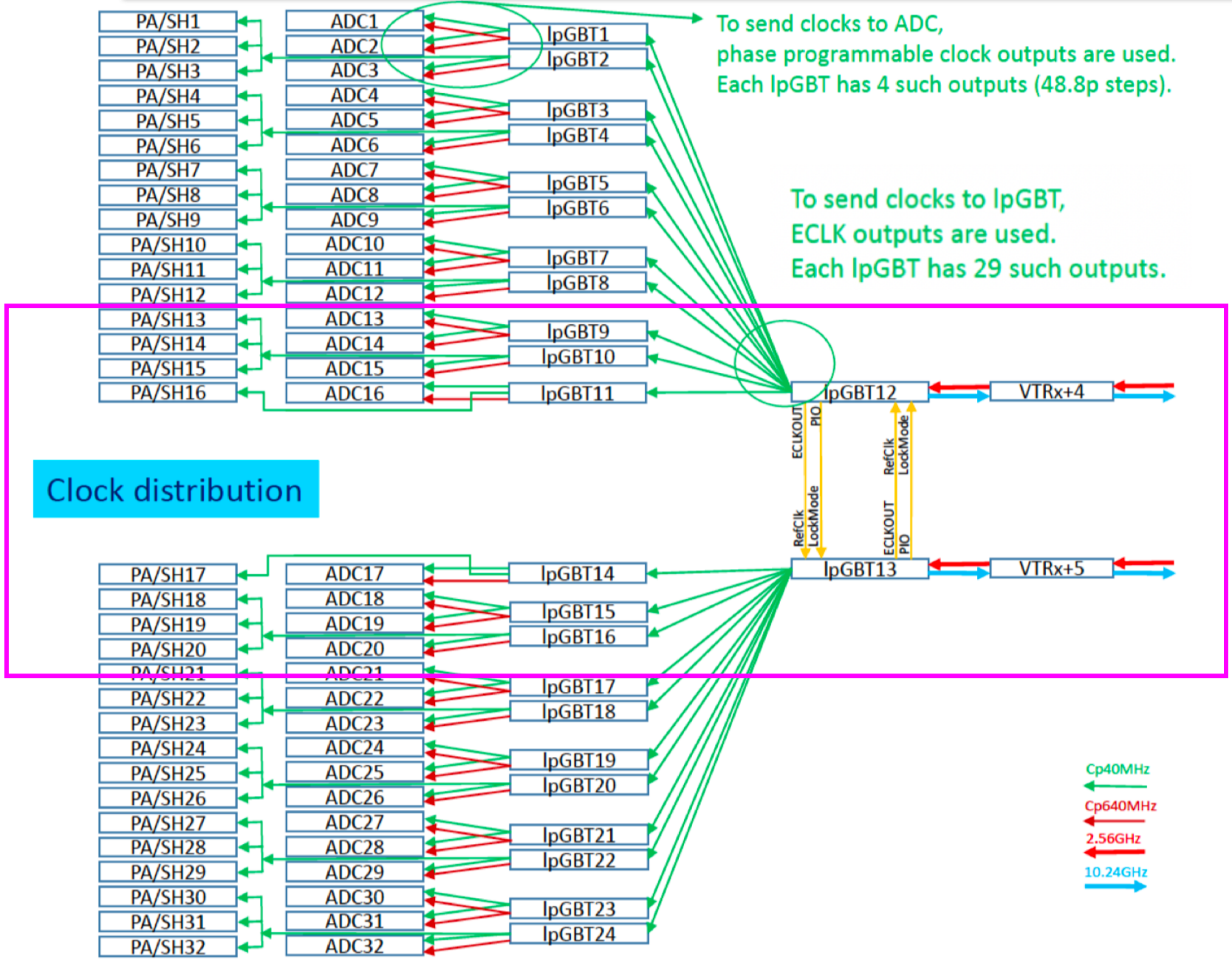
Back



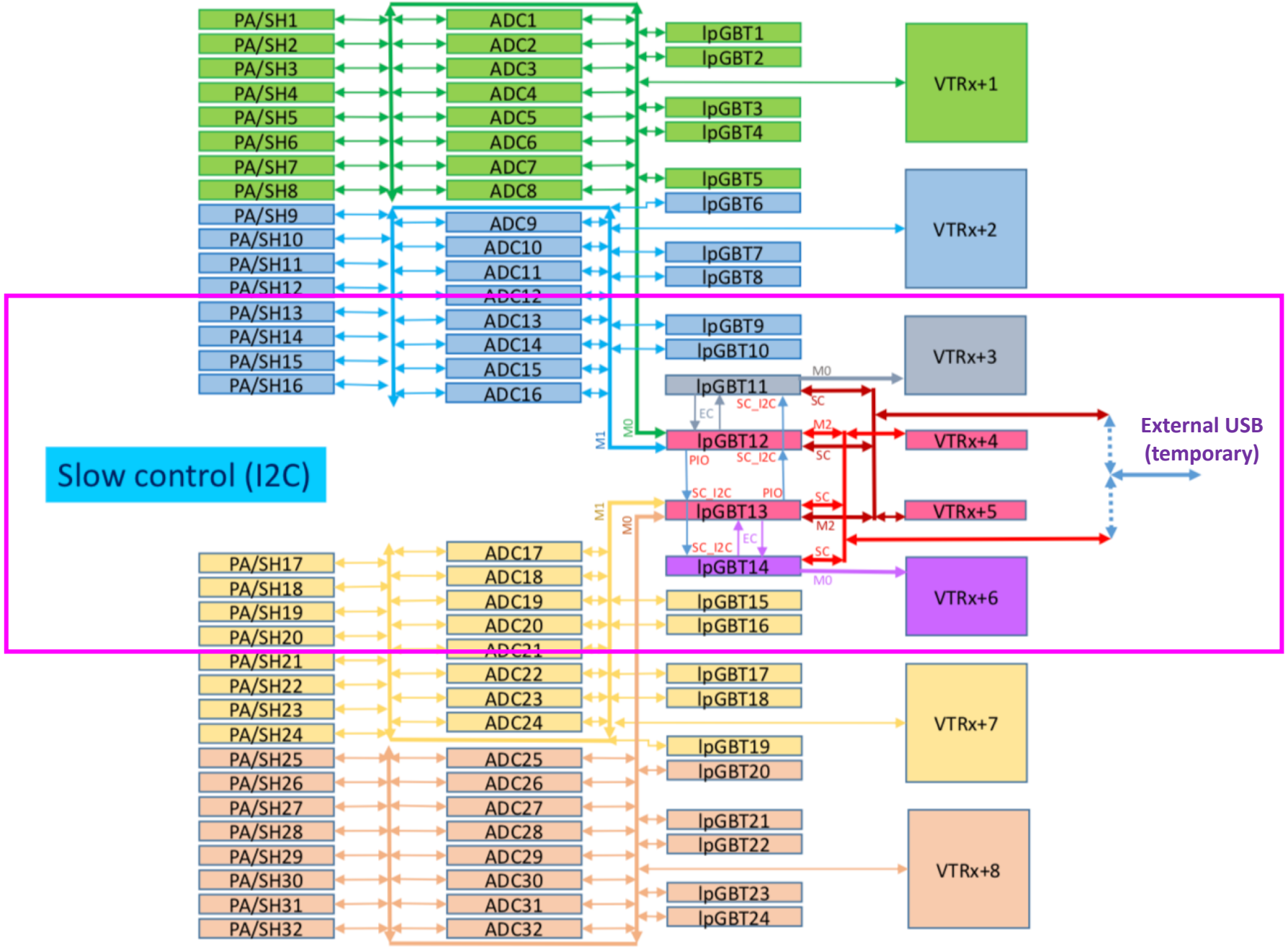
FEB2 Data/Signal Flow



FEB2 Clock Distribution



FEB2 I2C Slow Control



Slice Testboard Production Timeline

Apr 24 — FEB2 Specifications Review

Slice Testboard design was ready at that time. However, due to COVID-related lab shutdown, we took some extra time to revisit/expand the design, including implementing LSBs as well as two mezzanines to enable testing of various rad-tol powering schemes being developed by INFN

Jun 18 — PCB order placed with PCB vendor 1

Jul 2 — PCB order placed with PCB vendor 2 (after having adapted the design due to differences in the stackup)

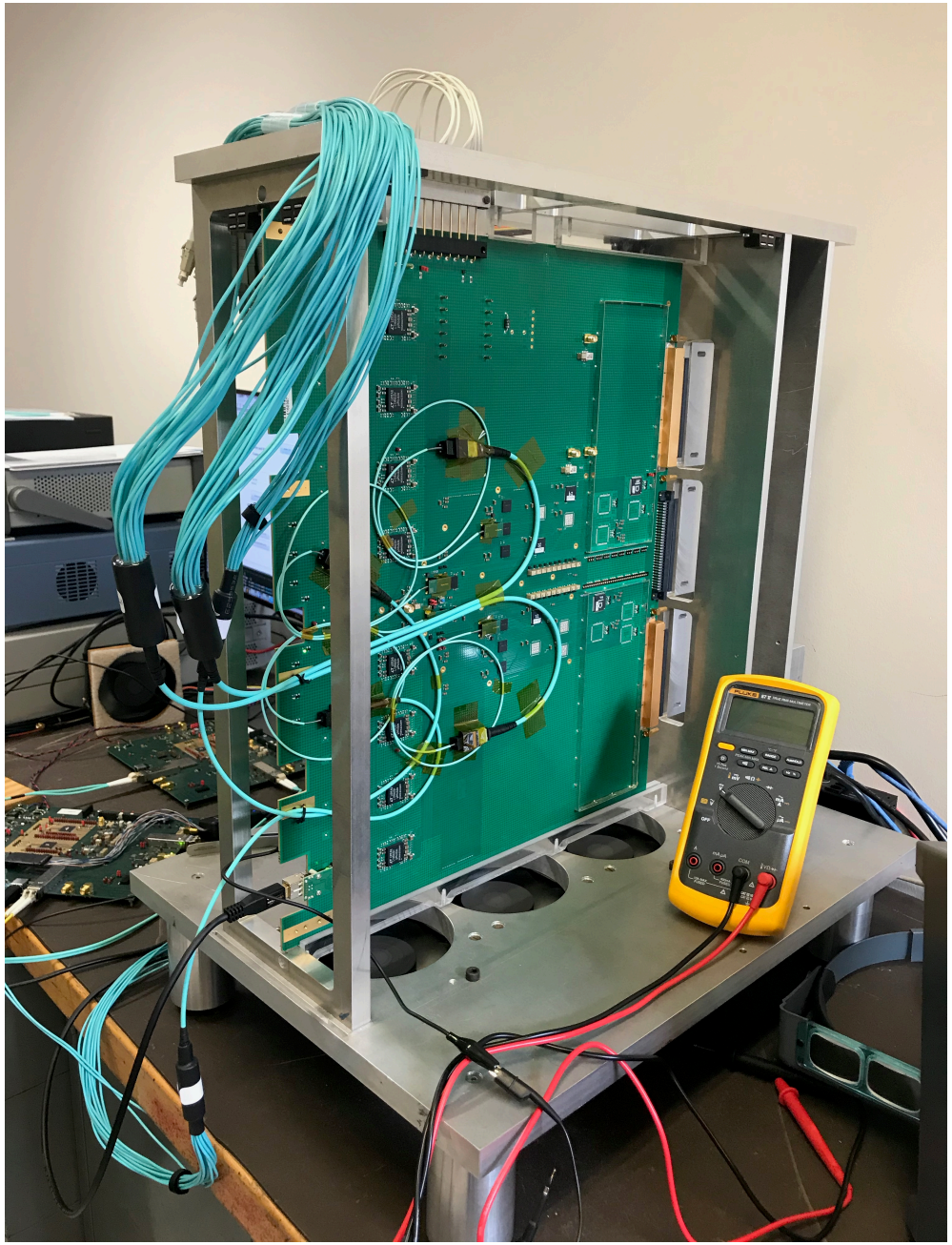
Aug 13 — Bare PCBs received from PCB vendor 1 (about 1 month of the delay was due to vendor awaiting reception of halogen-free material)

Sep 2 — First two (partially assembled) boards received, and testing gets underway (temporarily using Analog Testboards for control and readout of Slice Testboard)

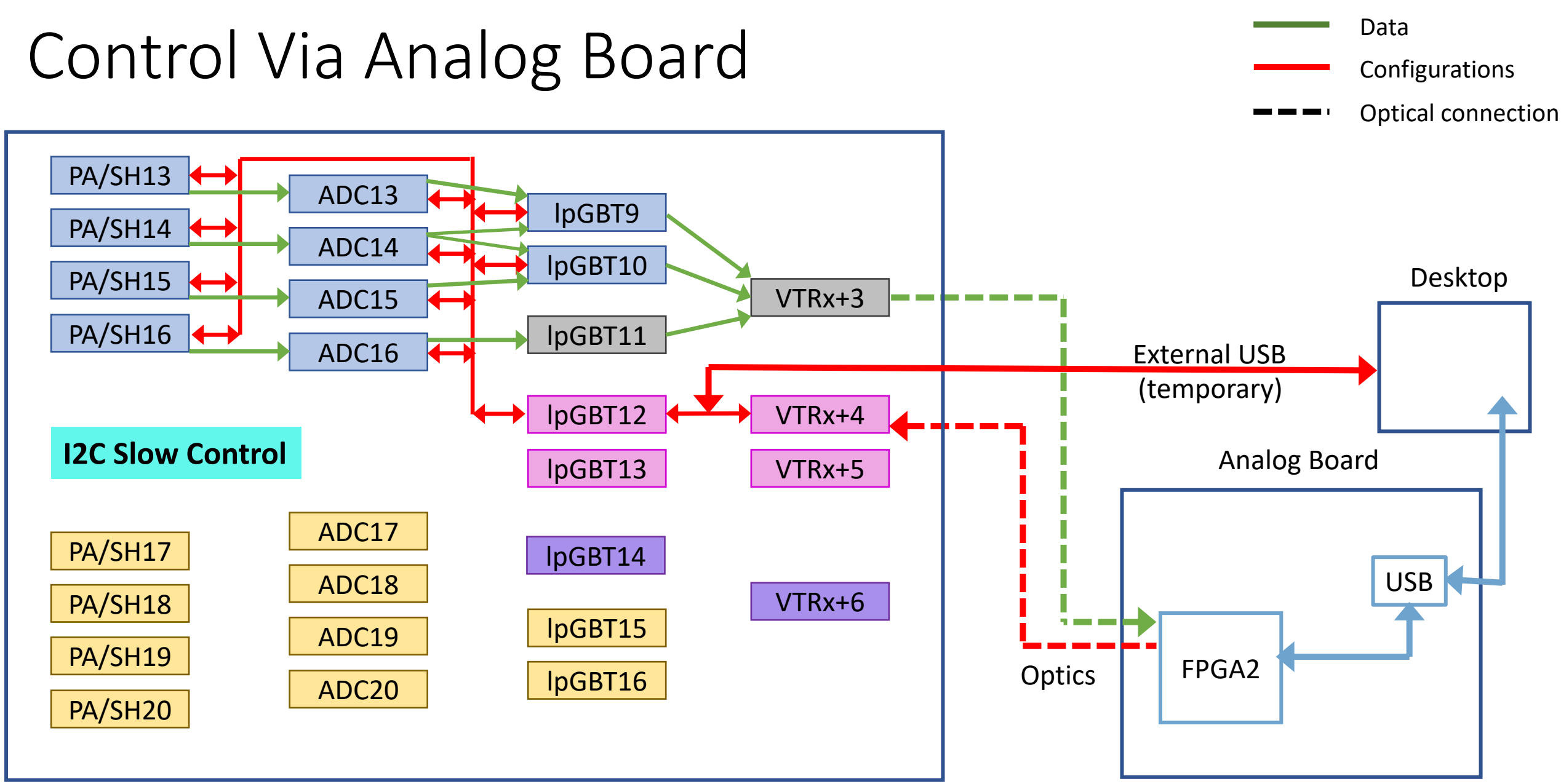
Sep 9 — PCB vendor 2 receives halogen-free material and is ready to proceed. We ask them to wait, so we can make any revisions indicated by the ongoing testing of the first 2 boards

Board Testing At Nevis

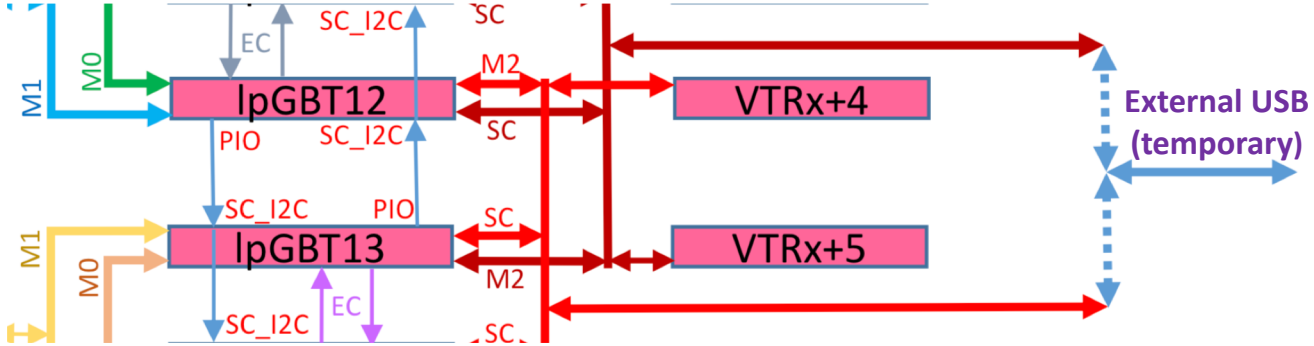
- Optics attached for IC control and data readback
- We are currently using the FPGA on the analog test board to write/read via the optics
  - This allows us to take advantage of software tools developed for the Analog Testboard by using it to control and readback the Slice Testboard
  - However, we can only control half of the Slice Testboard at once, and only read out one data channel at a time



Control Via Analog Board

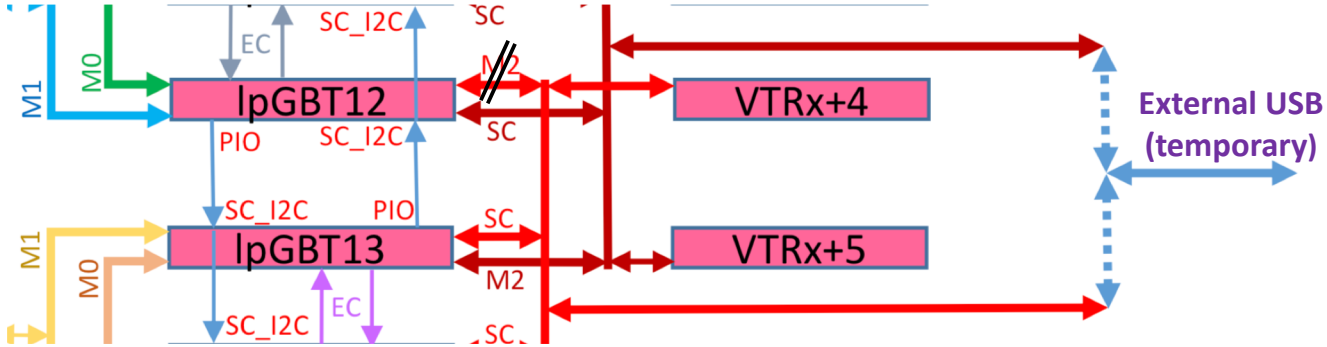


Early Issues with lpGBT I2C Buses



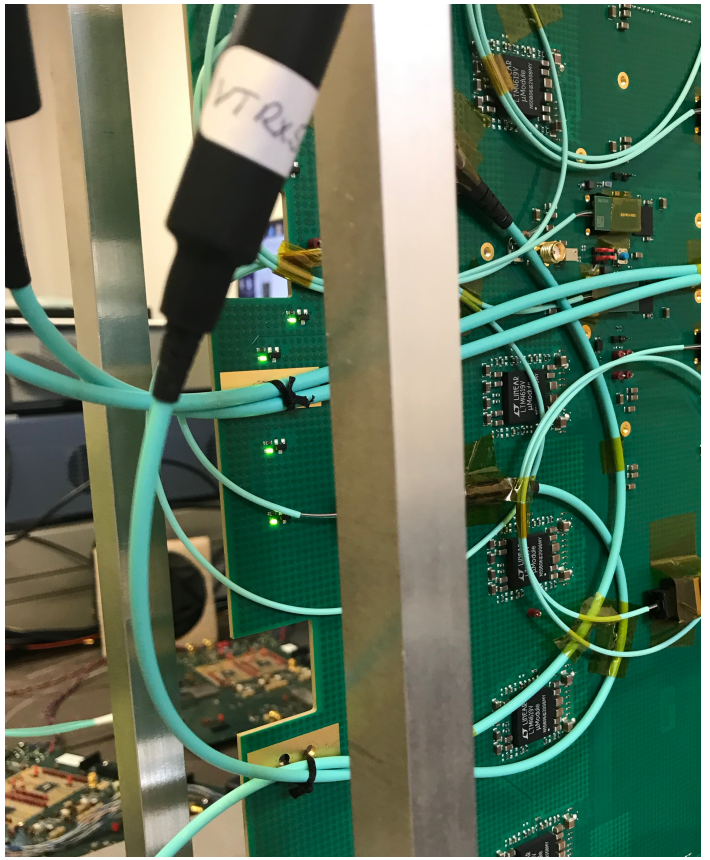
- The redundant control design has lpGBT12 and lpGBT13 sharing their M2 I2C bus
  - The external USB is connected to this shared bus, to be used to burn the e-fuses on lpGBT12/13 so that thereafter they power on in transceiver mode and can be addressed via their optical links
- We discovered that on powerup, lpGBTS do not properly reset
  - Instead, lpGBTS hold their I2C buses at fixed voltages
  - This originally prevented us from talking to lpGBT12/13 via the external USB

Early Issues with lpGBT I2C Buses



- Solution – we temporarily cut the M2 lines to lpGBT12
  - Once we cut M2 lines to the master lpGBT, we can freely control the M2 bus via the USB
  - Using the USB I2C, we burned the e-fuses on lpGBT13, which allows us to use IC communication via the optics
  - Then we can use IC control to reset the M2 buses
  - Repeat the process with lpGBT13
- Same problem with M1 from control lpGBTs
  - Simple fix → generate master reset sequence, resets M1 buses
- Note that this issue is separate from the known issue that M0 does not work on a subset of lpGBT chips

Control links demonstrated (so far)



PA/SH13
PA/SH14
PA/SH15
PA/SH16

ADC13
ADC14
ADC15
ADC16

lpGBT9
lpGBT10
lpGBT11
lpGBT12
lpGBT13
lpGBT14
lpGBT15
lpGBT16

VTRx+3
VTRx+4
VTRx+5
VTRx+6

External USB
(temporary)

I2C Slow Control

PA/SH17
PA/SH18
PA/SH19
PA/SH20

ADC17
ADC18
ADC19
ADC20

Optics (IC)

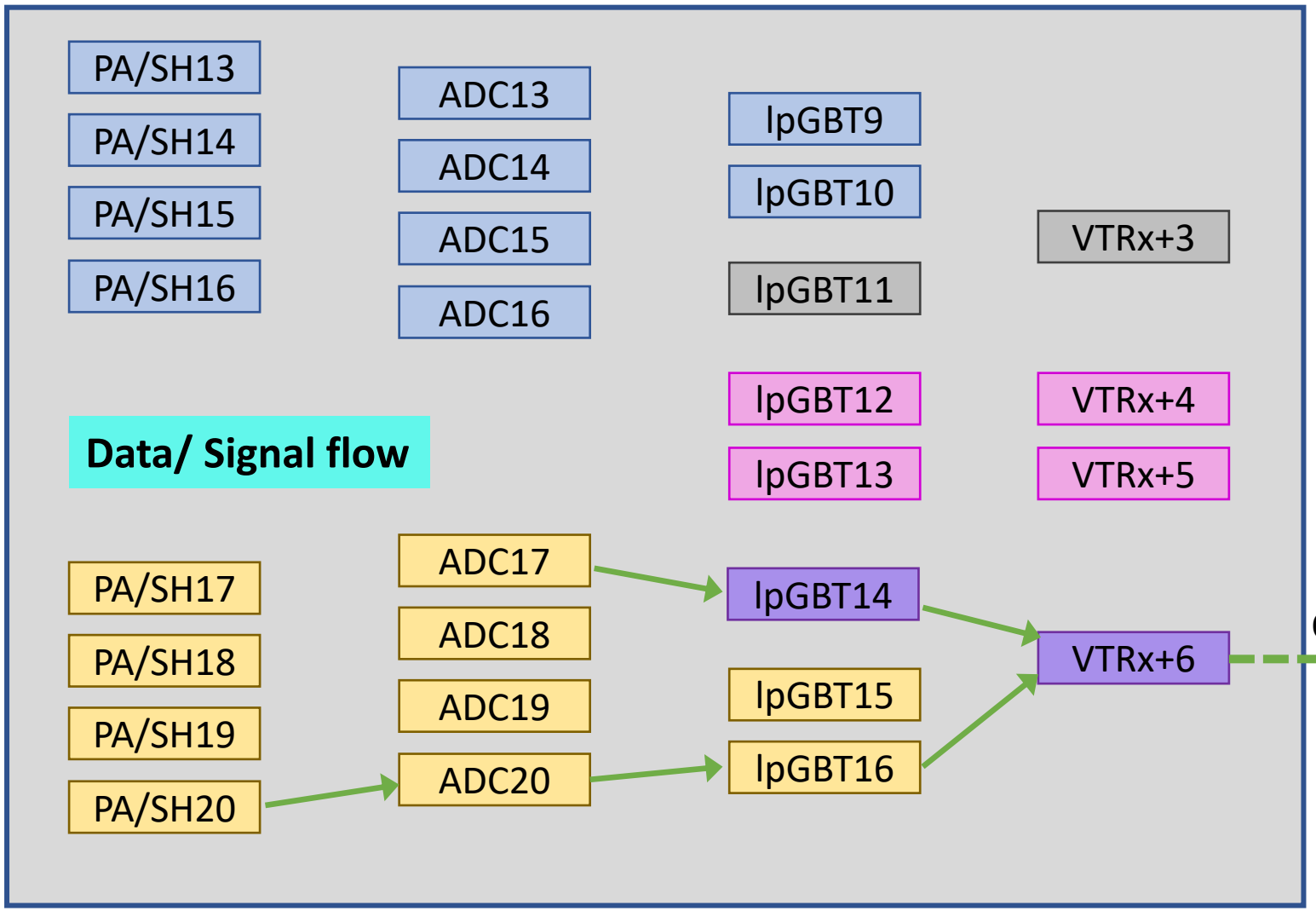
FPGA2

Desktop

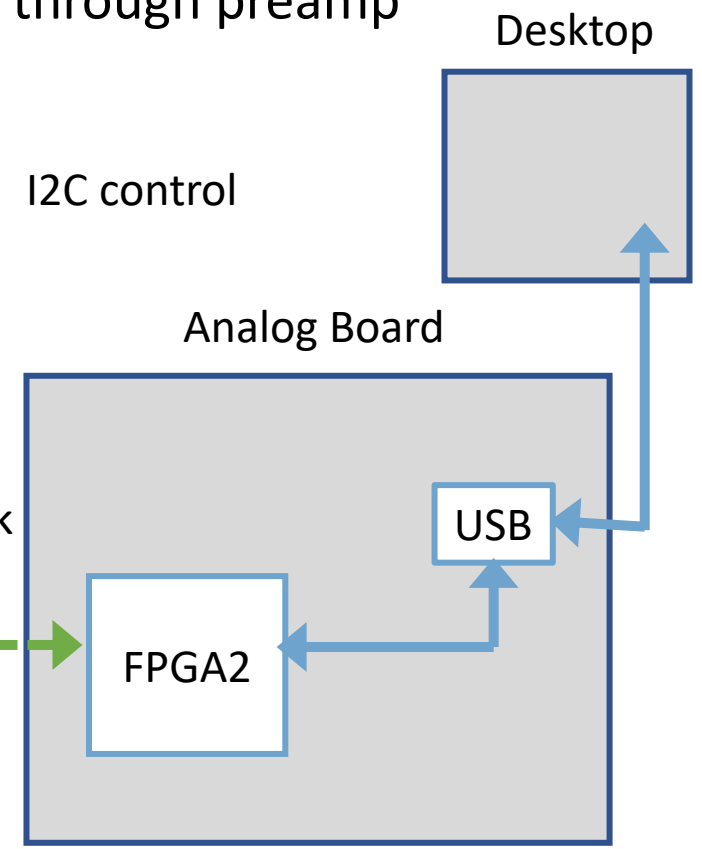
USB

Analog
Board

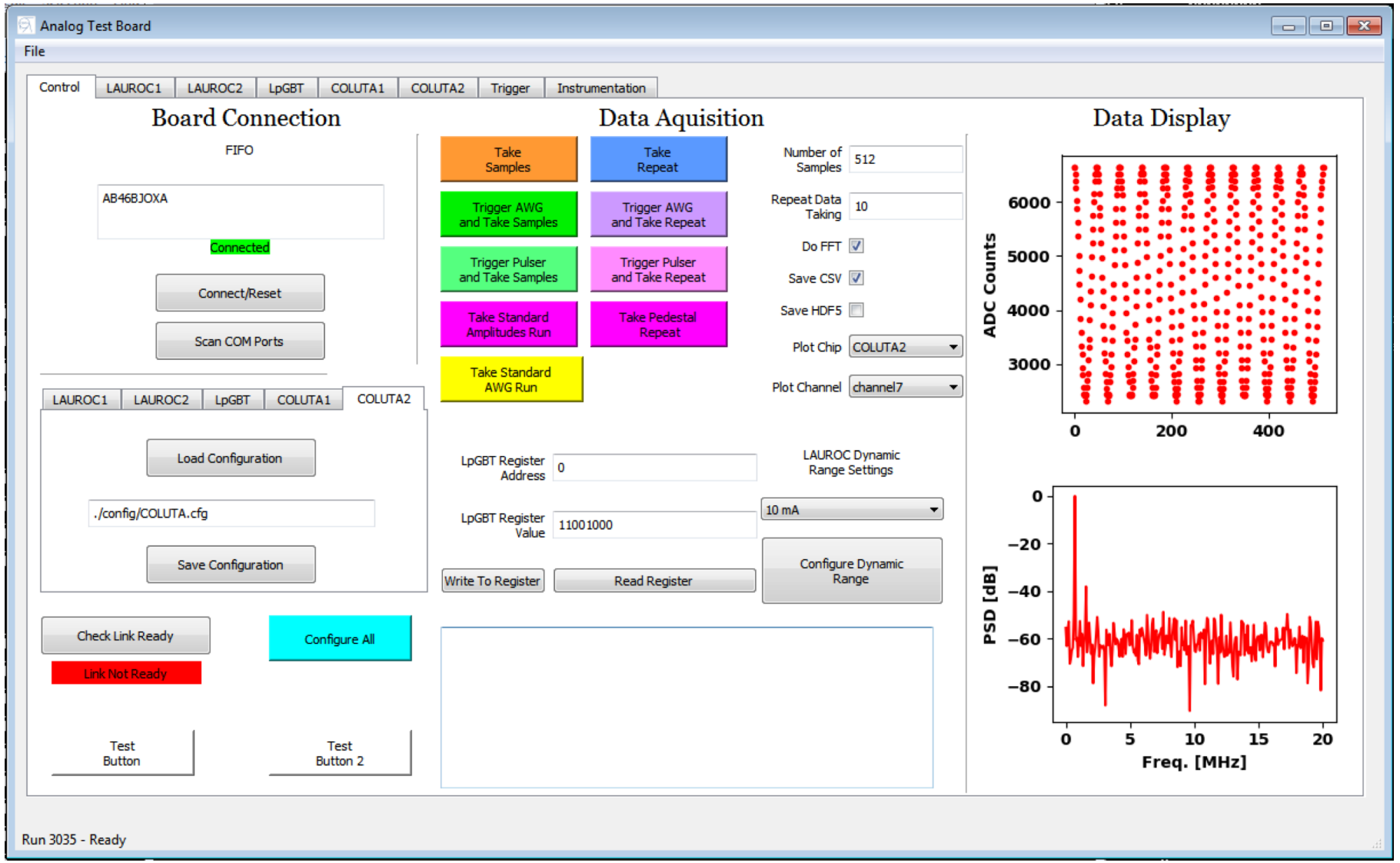
Data links demonstrated (so far)



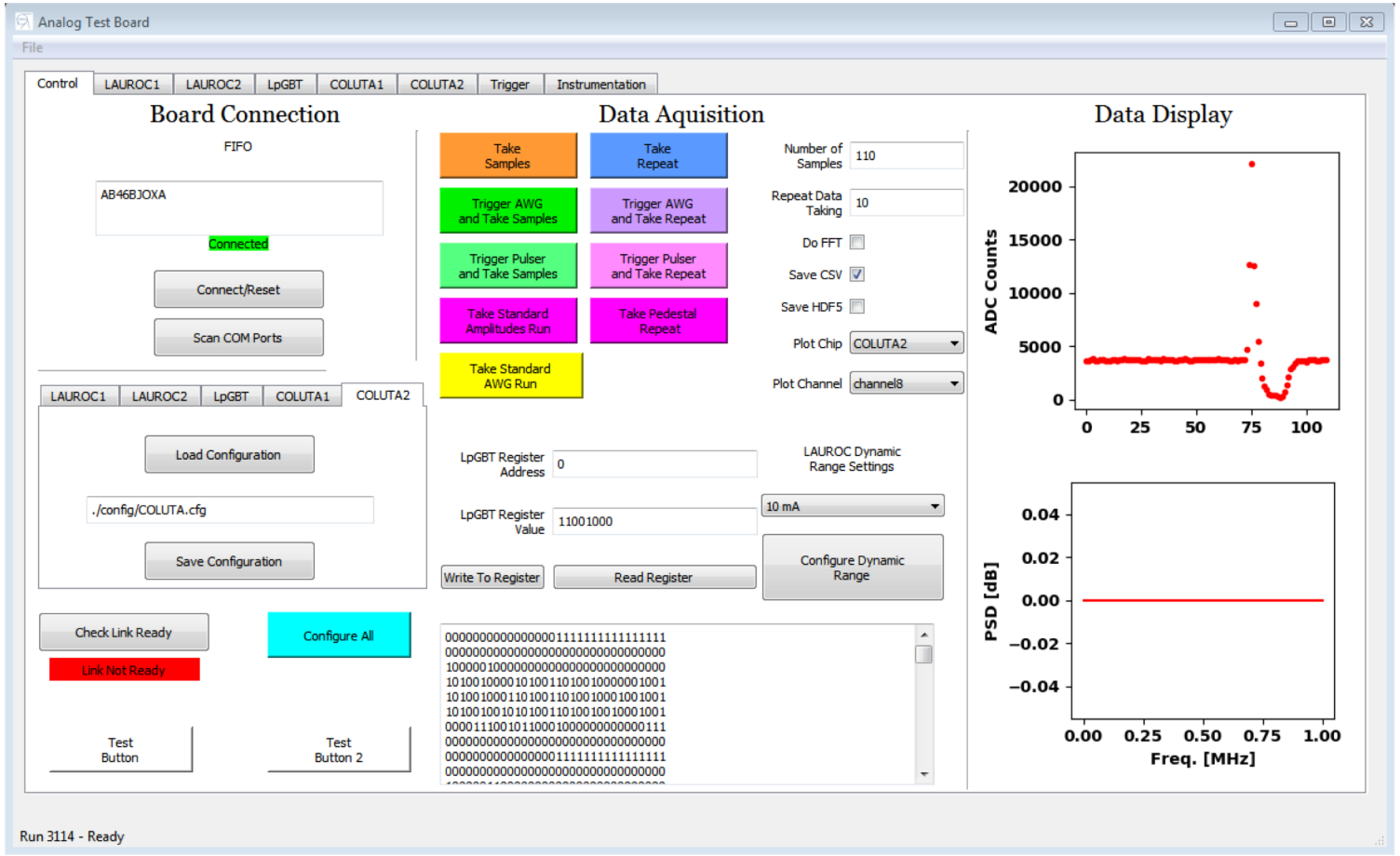
- ✓ Test pattern data from data lpGBTs
- ✓ Test pattern data from ADC
- ✓ Sine wave data through ADC
- ✓ Pulse through preamp

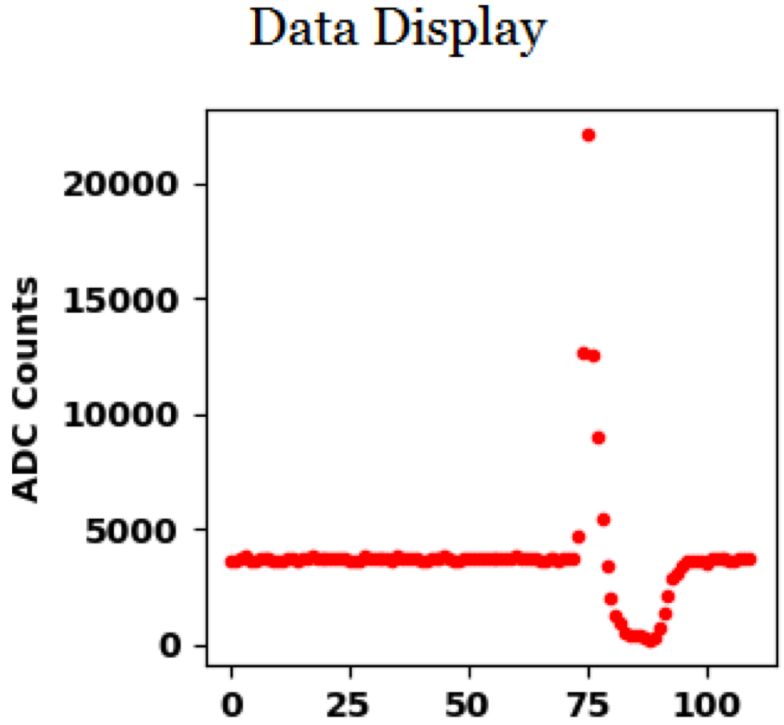


Sine Wave through ADC



Pulsing the PA/S





- We are currently working to adjust the ADC configurations to improve the performance

Summary of Progress

- ✓Resolve M2 bus issues and burn e-fuses on both control lpGBTs
- ✓Write to control lpGBTS via the optical link
- ✓Configure and read back both control lpGBTs
- ✓Configure and read back all data lpGBTs
- ✓Configure and read back ADCs
- ✓Configure and read back PA/Ss
- ✓Read correct test pattern data from data lpGBTs and ADCs via the optical uplink
- ✓Send sine wave through ADC
- ✓Pulse PA/S and read back via the optical uplink

Transition to FLX card

- To allow full control of the board and readout of all channels, we will use a FLX card going forward
  - The FLX card arrived at Nevis on Monday Oct 5th, and is currently being setup
  - FLX card has 48 channels

Next Steps - Timeline

Oct 5 — FLX card received at Nevis

Preparations made to be ready to migrate to FLX for both control and readout functions

Oct 12 — Start to use FLX to control and read out entire Slice Testboard

Nov 16 — Complete validation of Slice Testboard design, and proceed with fabrication of (slightly modified) PCBs with PCB vendor 2

Dec 7 — Receive new PCBs and submit for assembly

Jan 4 — Begin testing of new fully assembled boards

Feb 15 — Ready to deliver first board to collaborators

Conclusions

- Testing of the Slice Testboards is proceeding despite some delays due to COVID19 and the challenges presented by using halogen free materials
- We have verified the functionality every type of ASIC on the board (lpGBTs, VTRXs, ADCs and PA/Ss) as well as the bi-directional control links between these ASICs
- We have verified the data uplink path by sending a sine wave through the ADC and a pulse through the PA/S
- In the coming weeks we will complete our validation of the Slice Testboard design, aided by transitioning to the FLX card
- We are on track to send boards to our collaborators in early 2021