FEB2 "Slice" Testboard Update

Elena Busch
on behalf of Columbia (Nevis Laboratories)

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NEVIS LABORATORIES
COLUMBIA UNIVERSITY

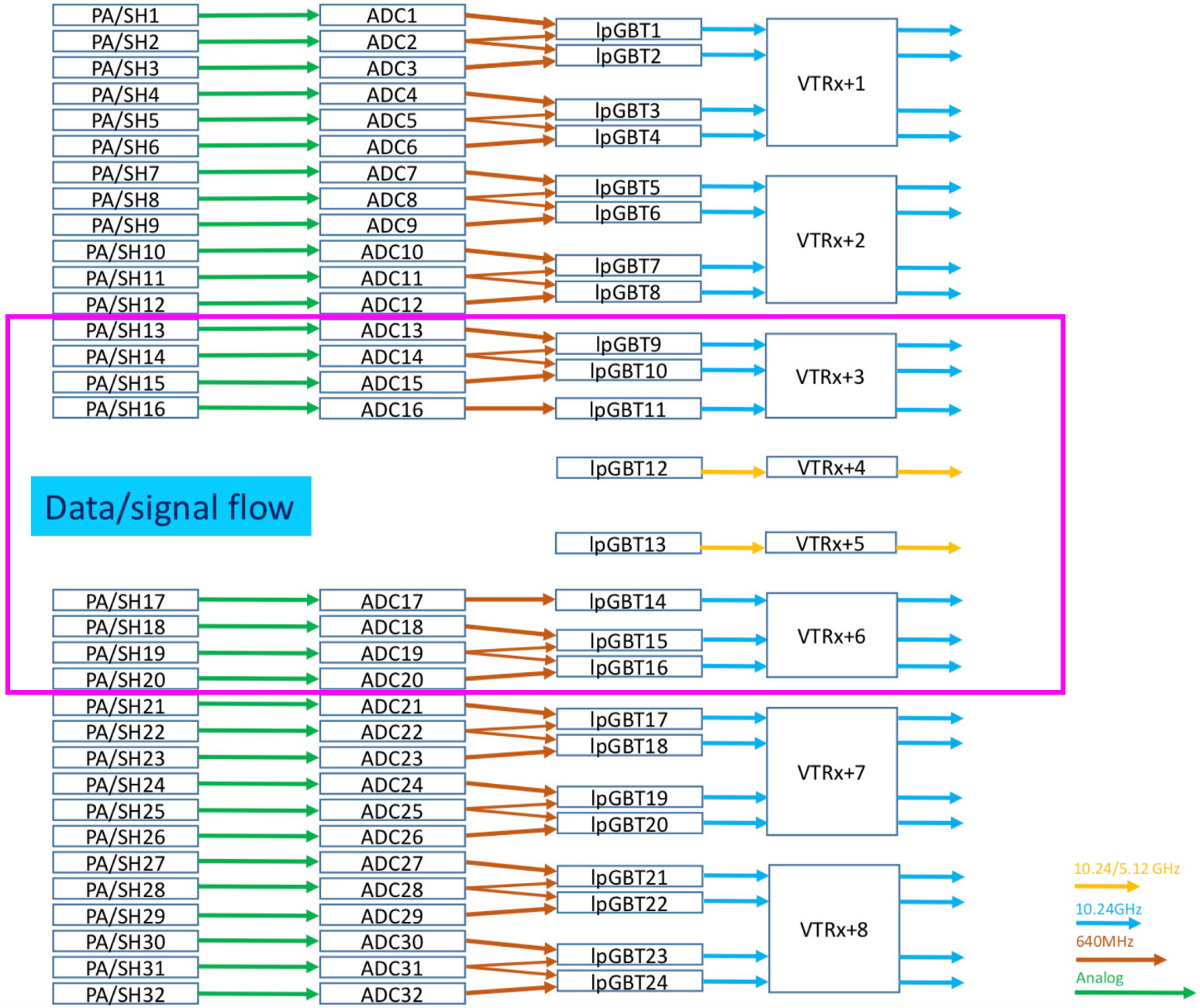
ATLAS EXPERIMENT

Overview

- Analog Testboard (2019)
  - 2 (LAUROC1 PA/S + COLUTAv2 ADC) + lpGBT
  - Verified full readout chain PA/S + ADC + optical data links
- Slice Testboard (2020-2021)
  - 8 (LAUROC2 PA/S + COLUTAv3 ADC + lpGBT) chips, 32 LAr channels available
  - Aim to demonstrate multichannel performance, bi-directional control links
  - v1.1 of the board is being tested at Nevis now – first fully assembled version after debugging done on partially assembled v1.0 board
- Full FEB2 Prototype (2021-2022)
  - All 128 channels

Review: FEB2 Data/Signal Flow

- V1.1 board assembled with full set of 8 PA/S, 8 ADCs, 8 lpGBTs
  - up from only 2 PA/S & 3 ADC on v1.0
- 32 channels of readout
  - Each channel represents a HI/LO gain pair
- Results will be shown only for the 16 MDAC channels



Features of v1.1

- New optical connections, designed by SMU
  - Front panel mounted connectors
- Fix for the lpGBT 12 & lpGBT13 master problem
  - The first time the board is brought up, we need to communicate with lpGBT12&13 to burn e-fuses
    - On v1.0, we had to cut the M2 lines to allow this communication
  - On v1.1, we can now isolate undefined lpGBT12&13 masters by changing the headers on the board
    - As soon as I2C buses are free we burn e-fuses on lpGBT12&13, and lpGBT11&14
  - This is a one time operation – once done the board can be fully operated via FELIX

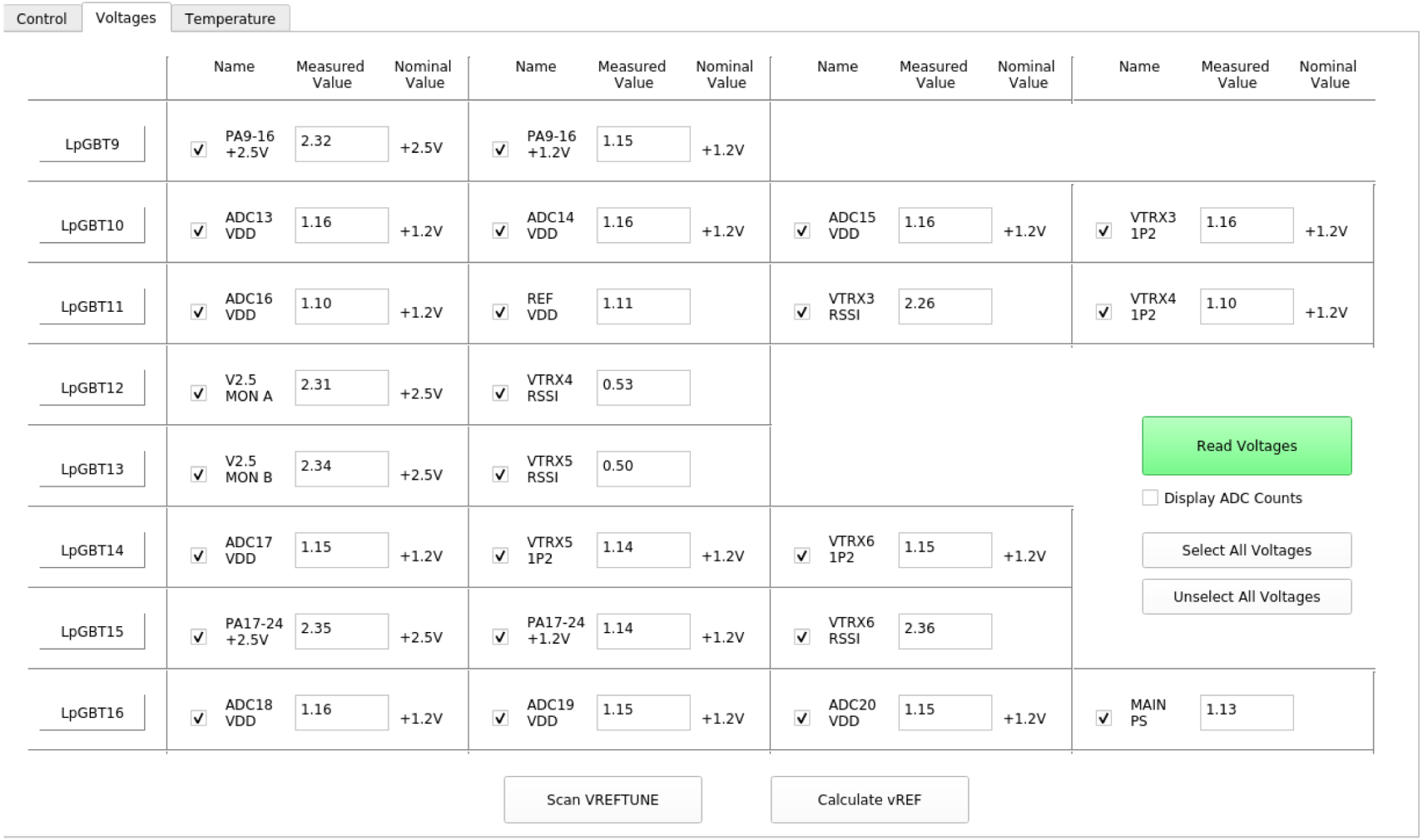
Status of the v1.1 boards

Both boards are fully operational!

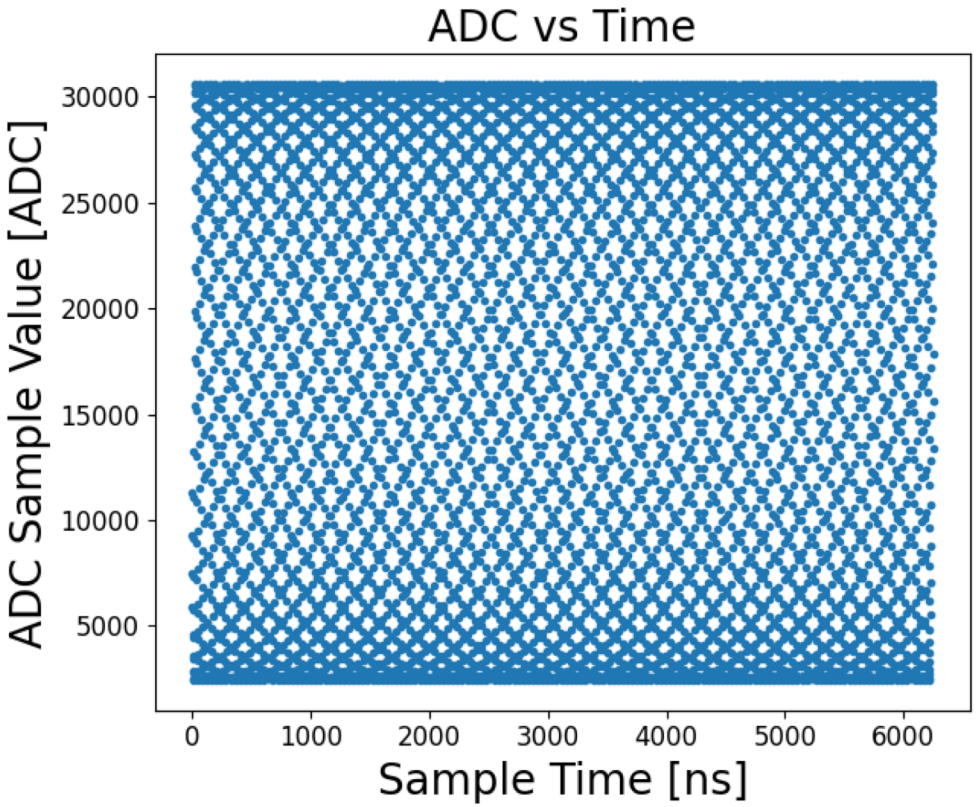
- ✓Bi-directional I2C control established between each master lpGBT (12/13) and all secondary chips (4 PA/S, 4 ADCs, 3 data lpGBTs for each master lpGBT)
- ✓Correct clock parameters have been determined for each ADC/lpGBT pair
  - Clock synchronization parameters must be tuned for each ADC/lpGBT pair independently on every board
- ✓We have seen correct test pattern data + noise data on all 32 channels
- ✓We have measured a sine wave signal through ADC20, which has a test input for this purpose

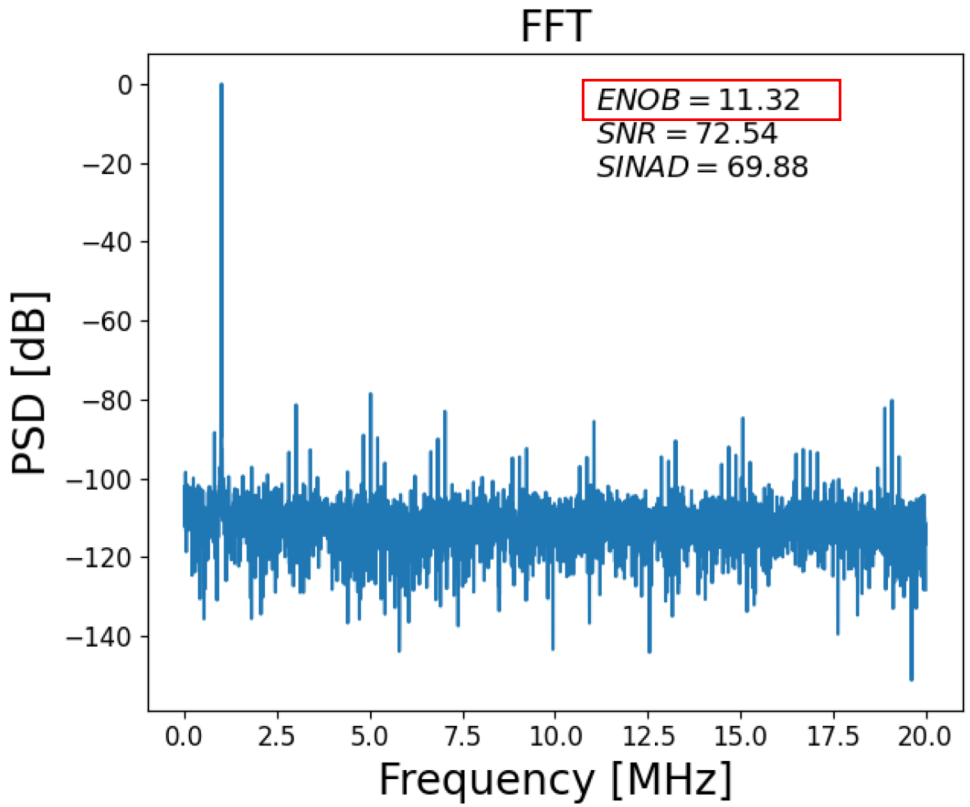
Voltage and Temperature Monitoring

- We have implemented in our DAQ GUI a fully software-based system for monitoring the voltage of all test points
- We have a similar system for monitoring the temperature



Sine Wave Results

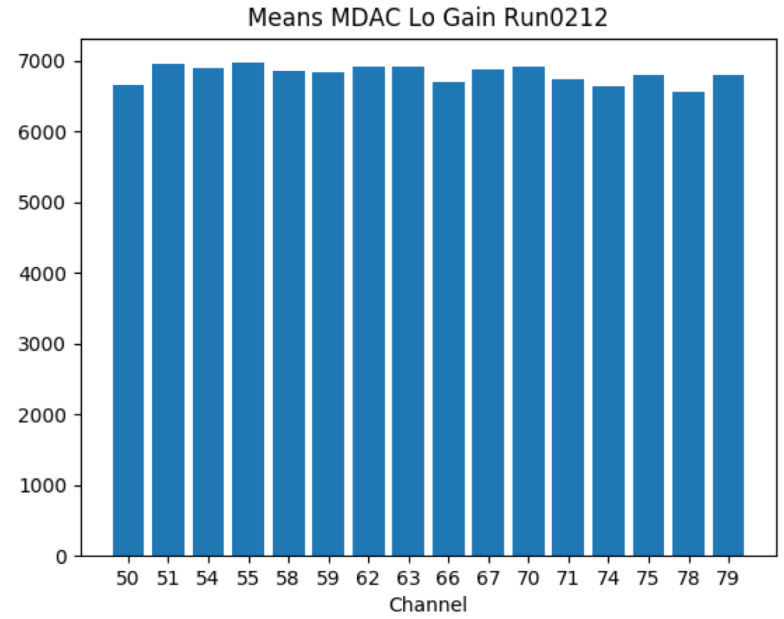


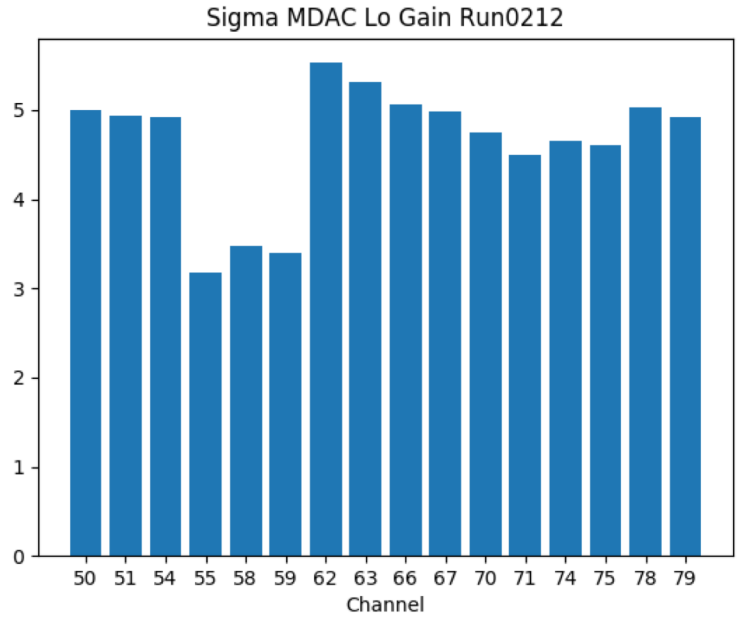


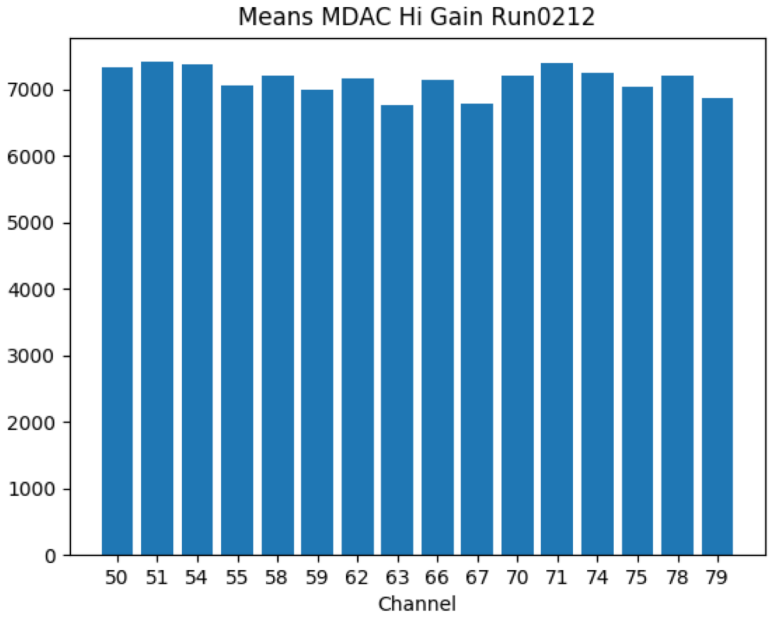
* Spikes in the FFT are most likely due to the MDAC transition sample offset which is an understood problem – there is a solution planned for CV4

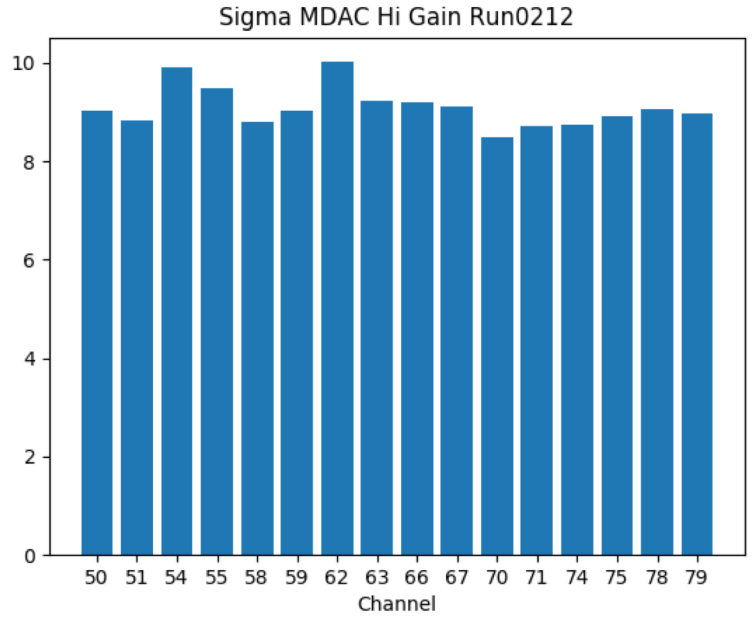
Noise Results

- Summary of noise results with the default PA/S parameters
  - The baselines have been adjusted so that all channels have a baseline close to 7000 counts
- On average we see ~9 counts of noise in the HG, and ~5 counts of noise in the LG
- These noise levels are higher than expected



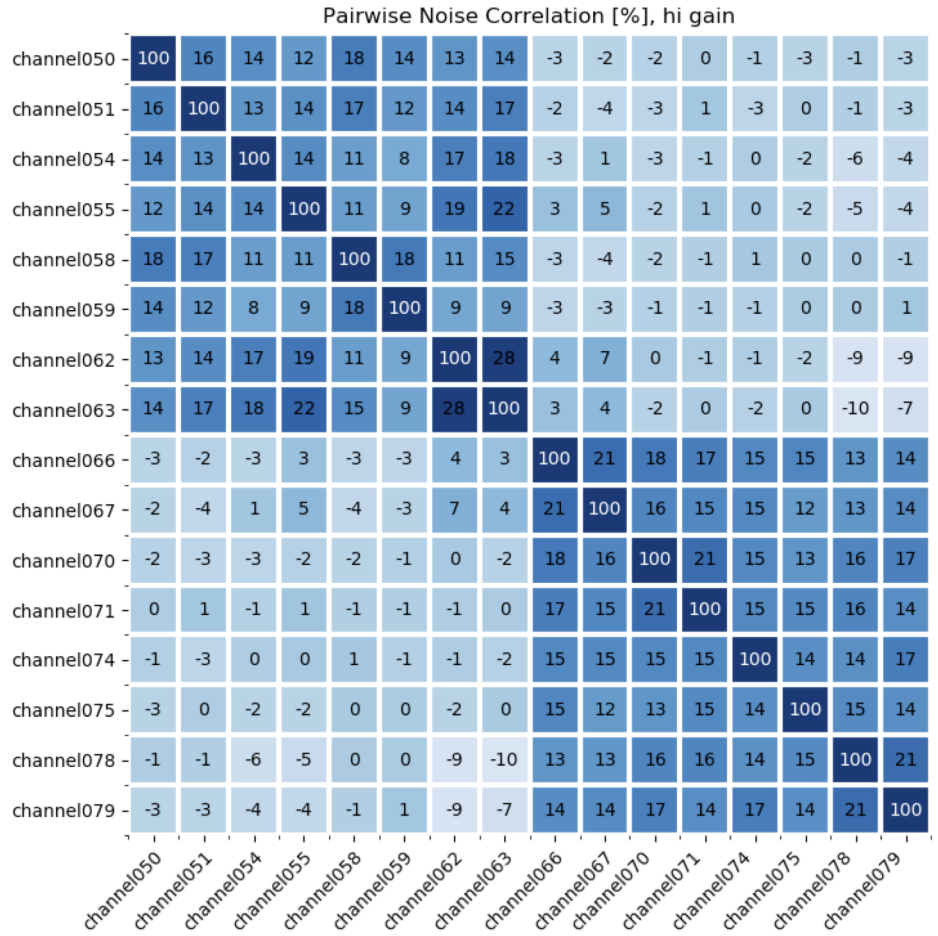


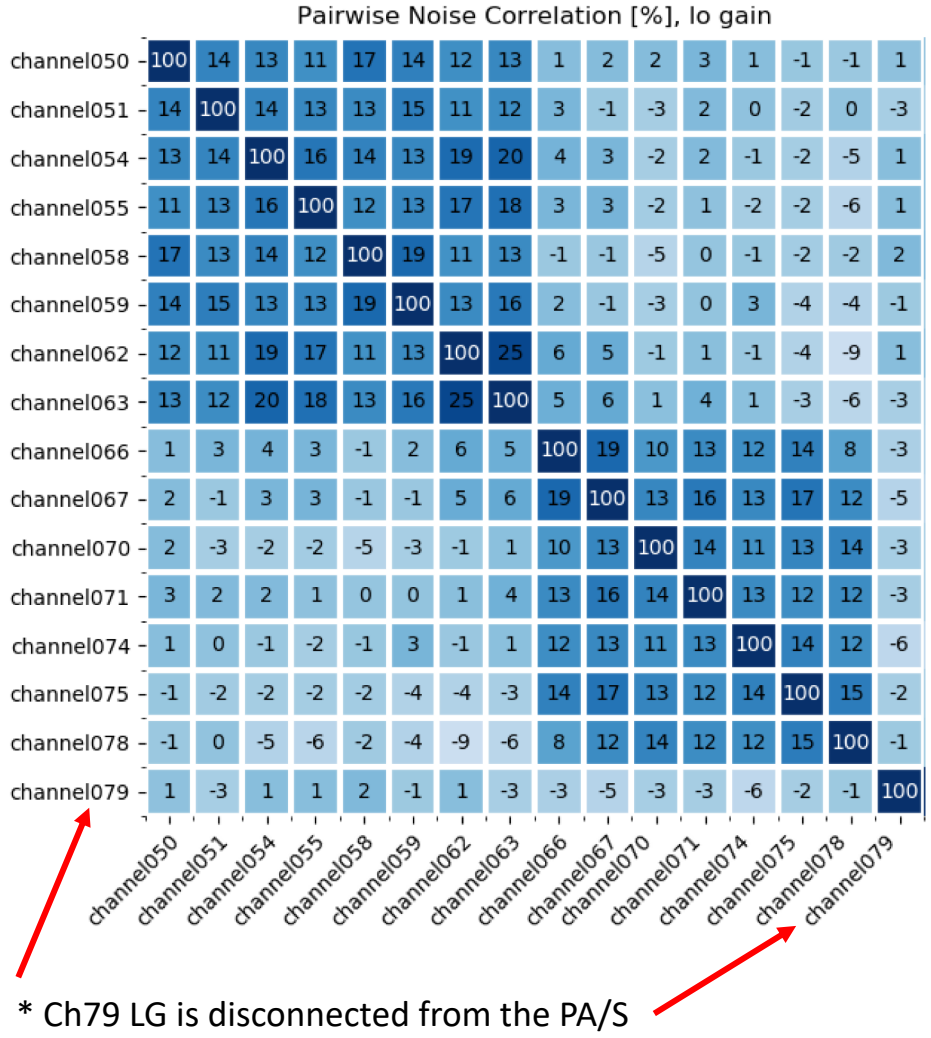




Noise Correlation

- Noise is correlated within each half of the board
- Within a half of the board, the noise correlation is mostly flat, and large (~10-20%)
- Opposite sides of the board are slightly negatively correlated

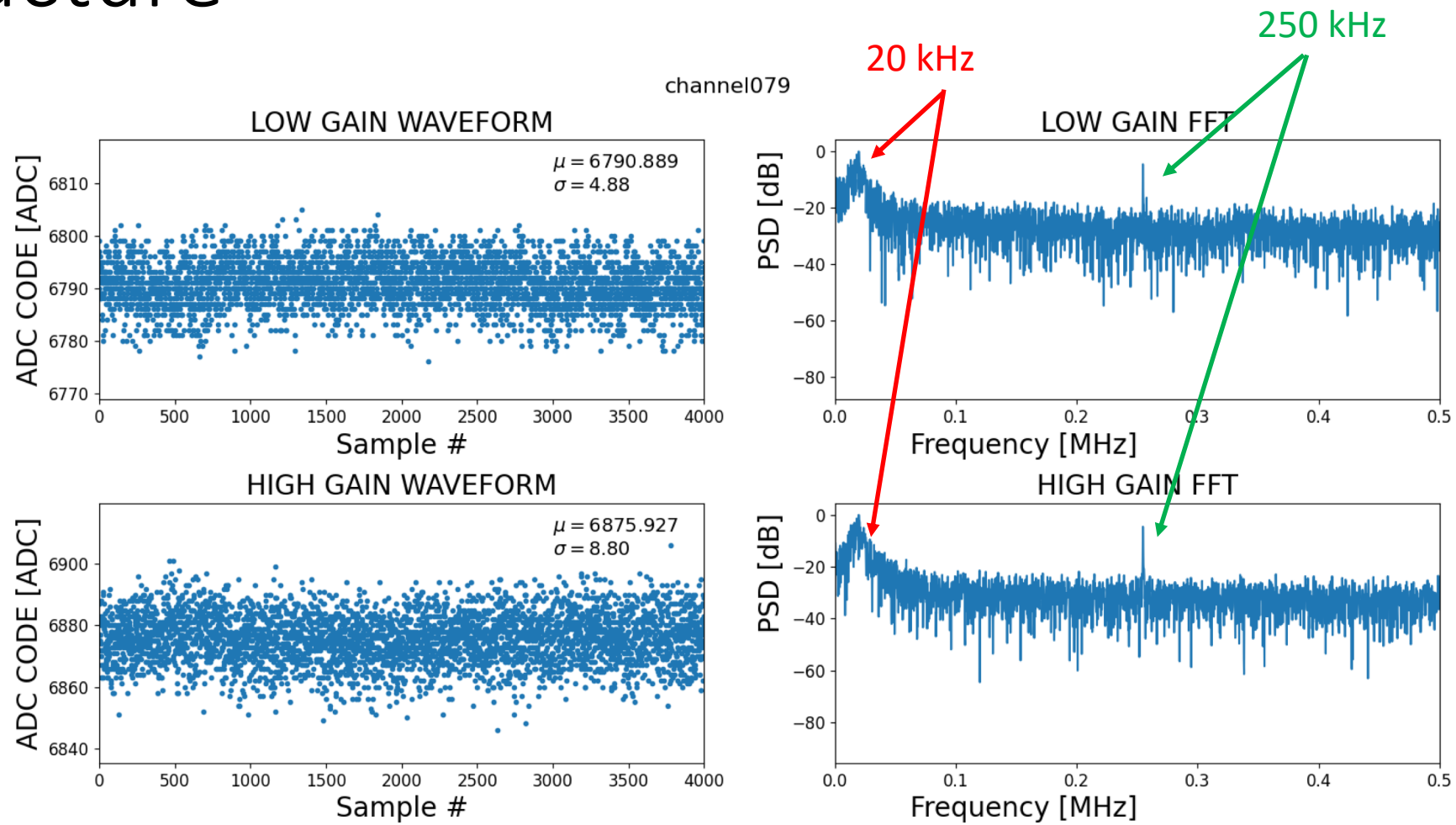




* Ch79 LG is disconnected from the PA/S

Noise Structure

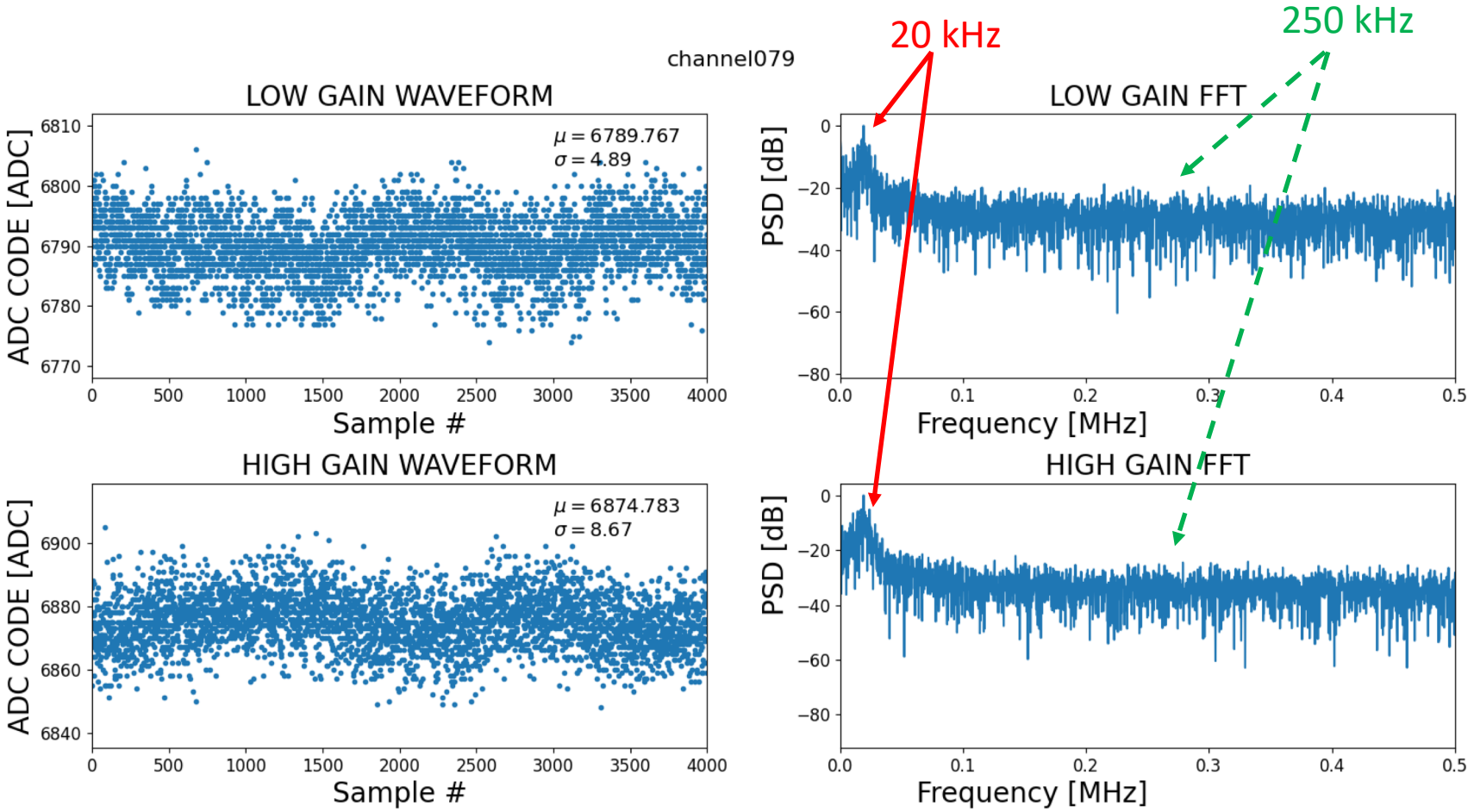
- There is a prominent 250 kHz spike in the FFT of the pedestal data
- We also observe a broad peak around 20 kHz
- The DCDC converters operate at 250 kHz – we wanted to isolate them as the source of the 250 kHz spike



Noise with External Linear Power Supply

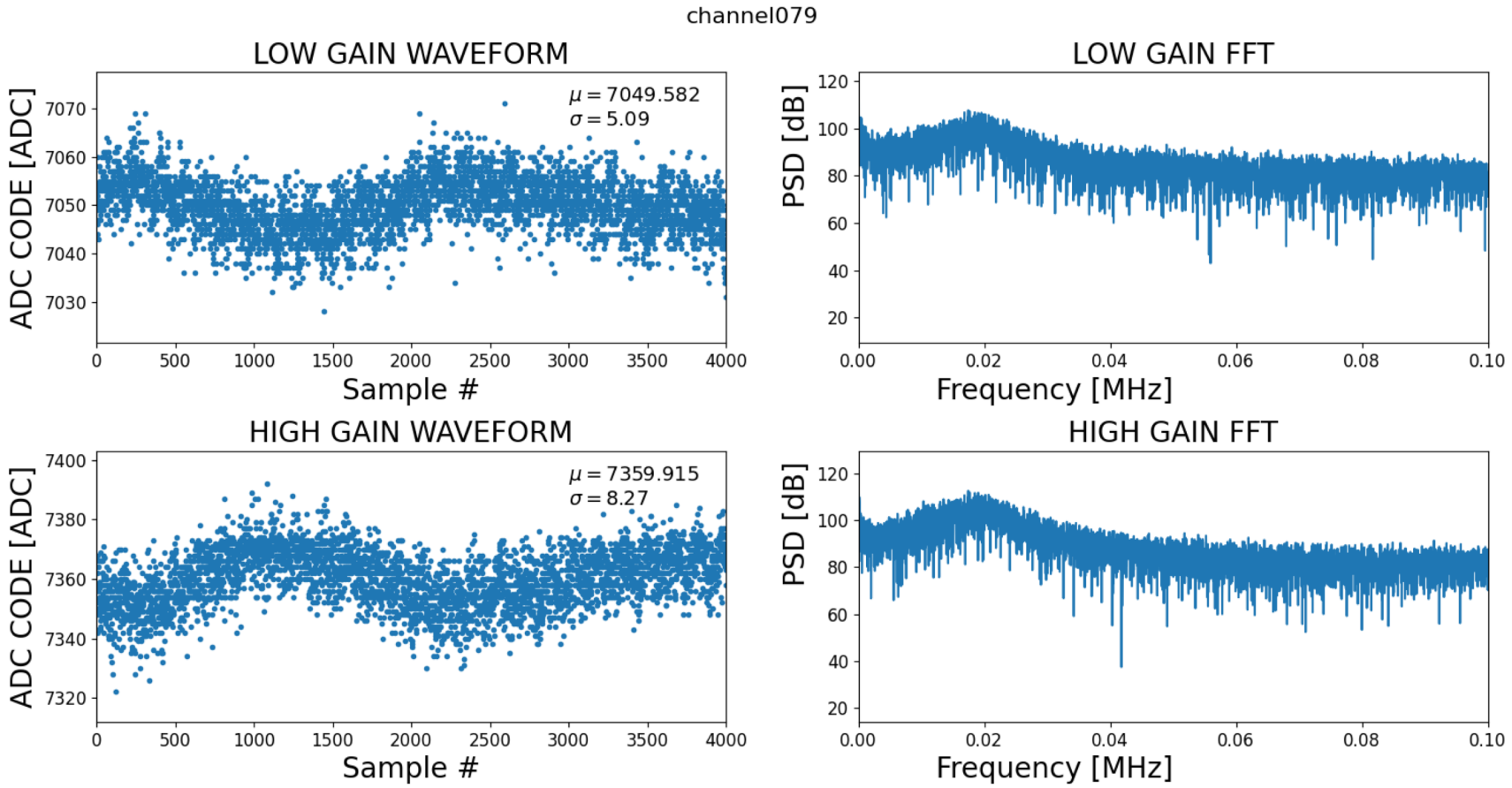
- For this measurement we bypass the DCDC converters with linear external power supplies

➢ We see the 250 kHz spike disappears, but the large peak around 20 kHz remains



20 kHz Noise

- We see the 20kHz noise is very dominant in the noise distribution
- We would like to understand where the noise comes from, and how it couples to our measurements



Investigating 20 kHz Noise

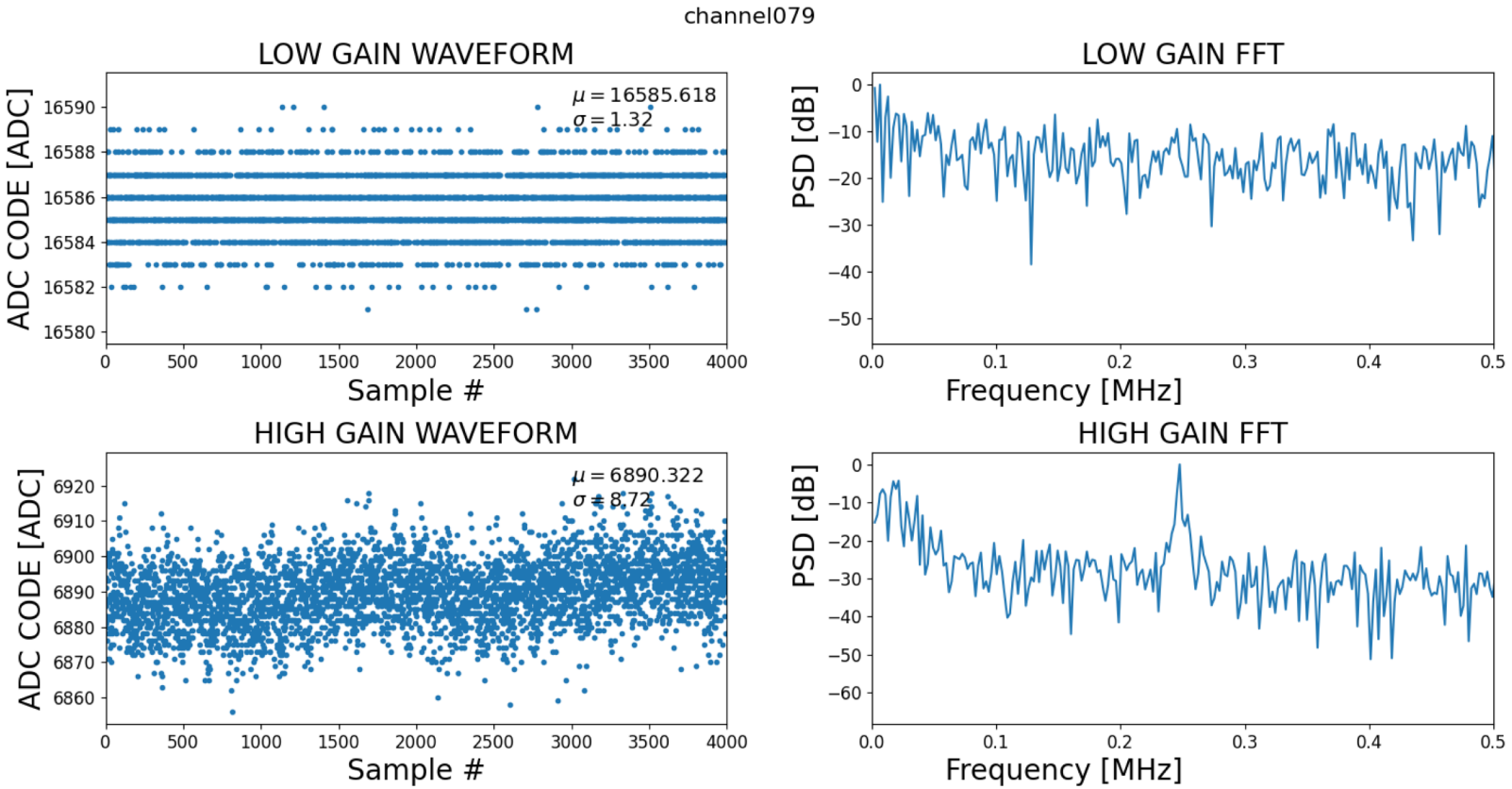
We have so far tried a number of modifications to the board to see if we could isolate the source of the 20 kHz noise:

- Adding a Faraday cage over the input connectors
- Adding a Faraday cage over the preamps
- Shorting the signal input pins
- Disabling the PA/S 40 MHz clock
- Removing the AC-coupling capacitor in the input protection networks, in order to disconnect the PA/S input
- Partially disabling the preamp
  - ON_pa=0, ON_g20=1, ON_lg_s1=1, ON_hg_S1=1, ON_lg_s2=1, ON_hg_s2=1
  - ON_pa=0, ON_g20=0, ON_lg_s1=1, ON_hg_s1=1, ON_lg_s2=1, ON_hg_s2=1
  - ON_pa=0, ON_g20=0, ON_lg_s1=0, ON_hg_s1=0, ON_lg_s2=1, ON_hg_s2=1

The 20kHz noise remained roughly consistent through all these tests

Ch79 LG - Disconnected from PA/S

- Ch79 LG can be disconnected from the PA/S
  - This was done we so we can send an external pulse to the chip
- We see the 20 kHz noise is gone in this measurement, and the noise is greatly reduced (1.3 counts, down from 4.9 counts)
- This, coupled with our other tests, implies 20 kHz noise is coming through the PA/S



Timeline (updates since Dec LAr Week Presentation)

- ✓ Dec 28 - Received new PCBs and submitted for assembly
- ✓ ~~Jan 25~~ Feb 15 - Began testing of 2 new fully assembled boards
- ? Mar 5 – New PA/S chips sent from Omega for packaging

Next Steps

- ➢ We are working to uncover the reason for the high noise levels and come up with a solution
- ➢ We can submit 3 more boards to the assembler once we have the new PA/S chips

Conclusions

- We have demonstrated control and readout of all 32 channels on both fully assembled v1.1 Slice Testboards
- Up to 3 more boards can be produced once more PA/S chips are available
- We have begun performance evaluation of the board and will continue in the coming weeks
  - Investigations of the noise performance continue

Backup

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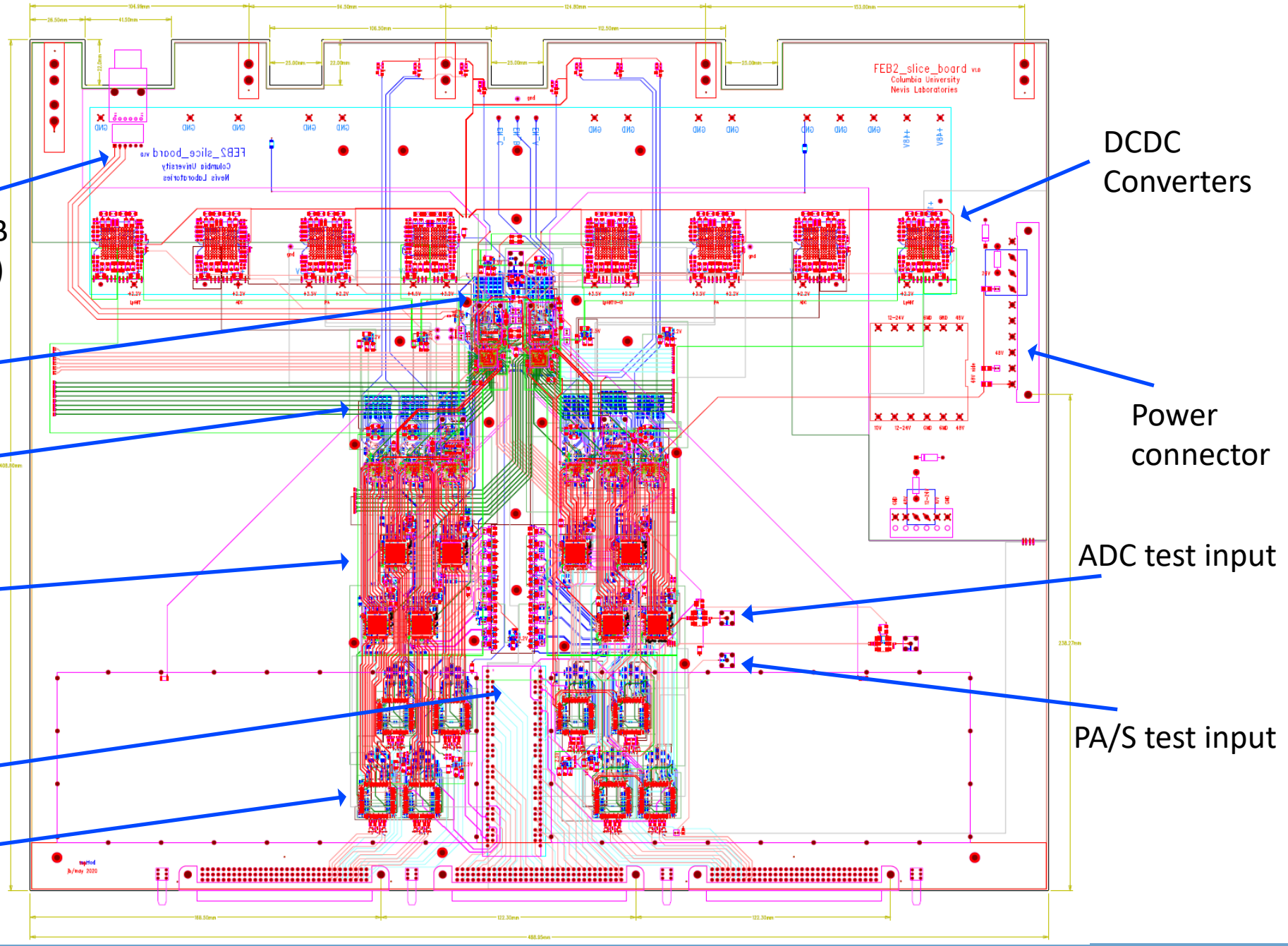
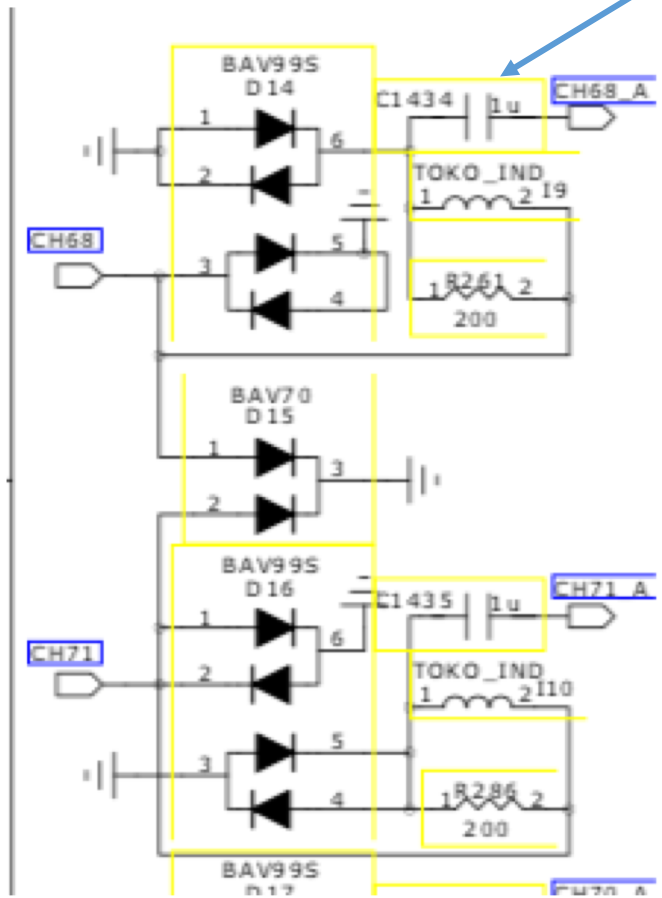
Slice Testboard Layout



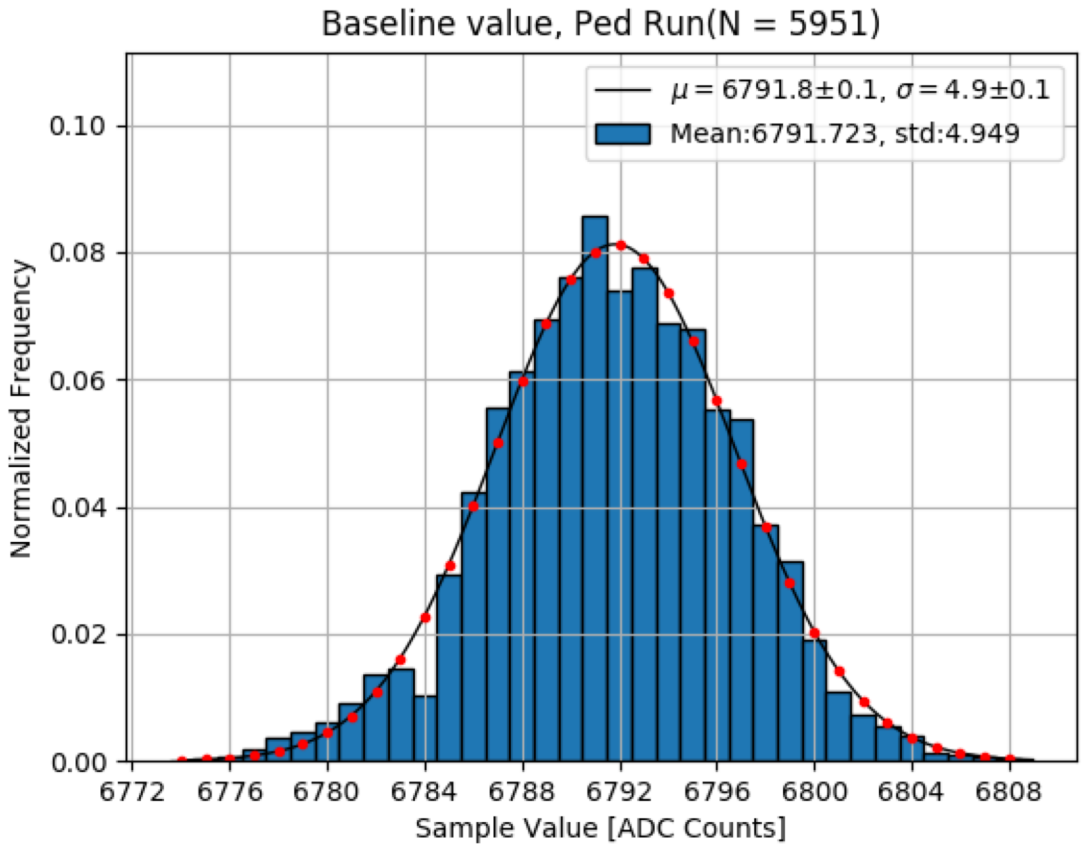
PA/S Schematic

AC Coupling capacitor

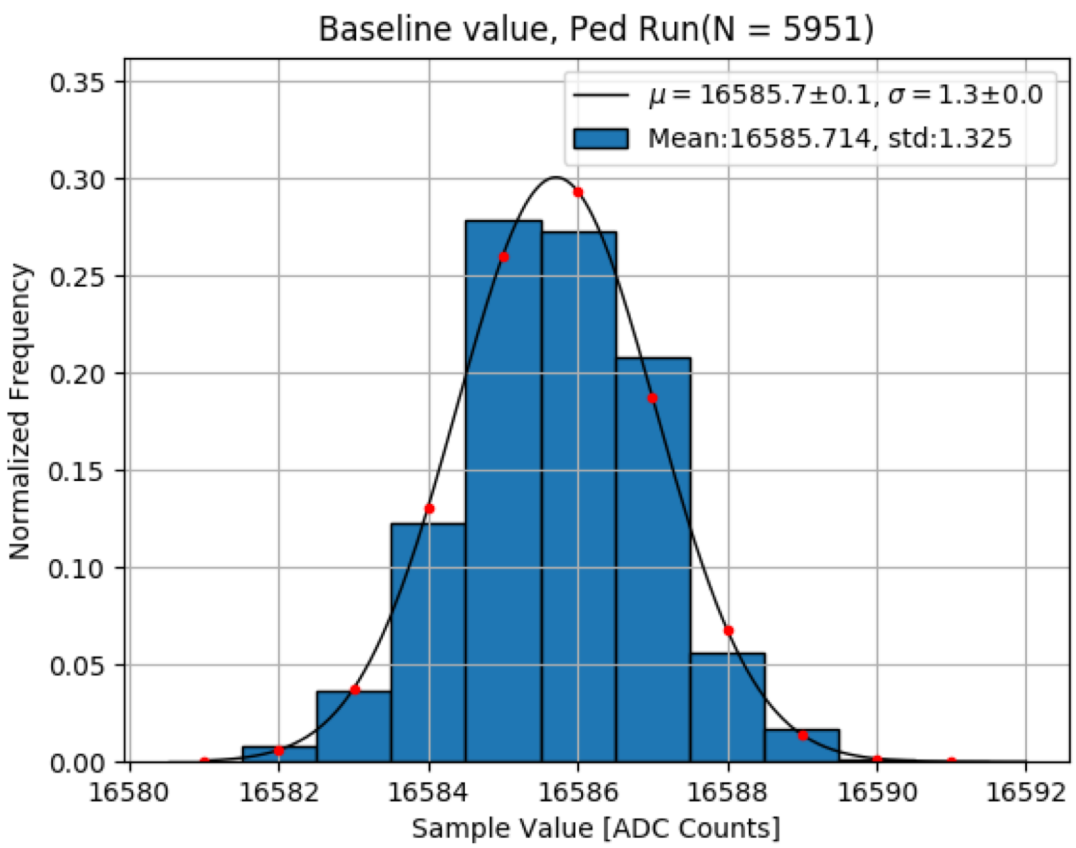


Ch79 LG Noise Histograms

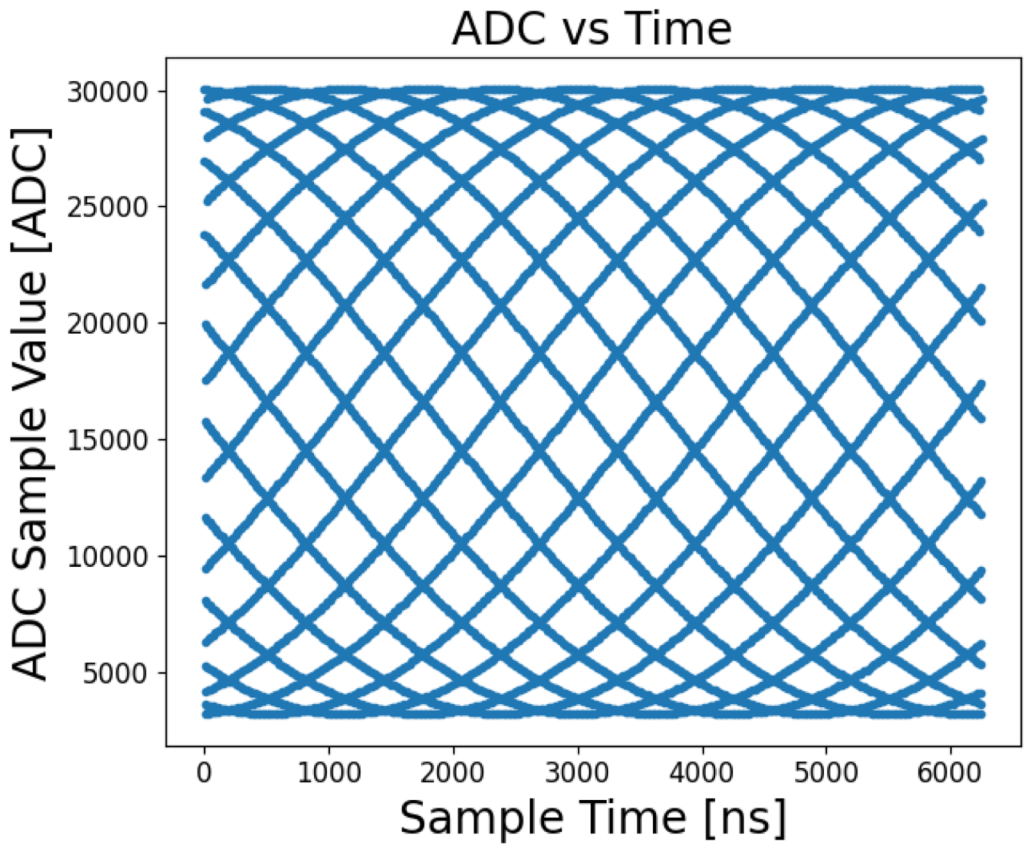
Connected to PA/S

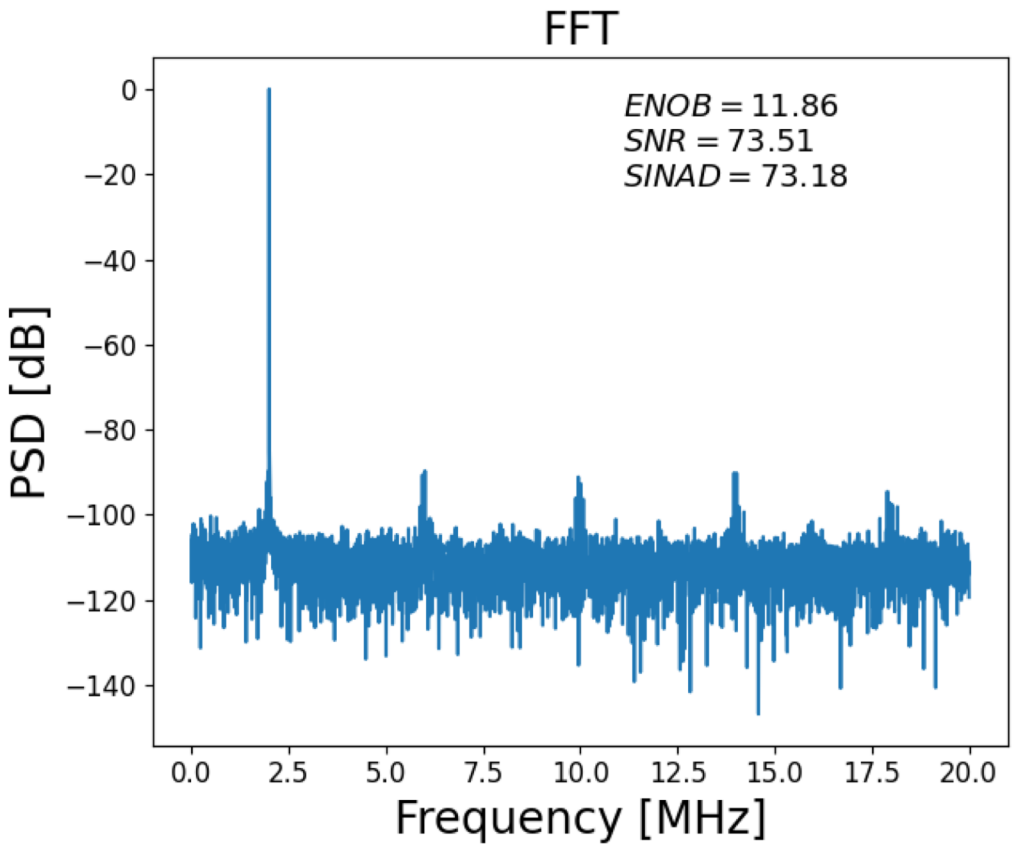


Disconnected from PA/S



Sine Wave Results from v1.0





Noise Results from v1.0

Channels 66 & 67 are not connected to a LAUROC (no LAUROC17 on board)