LAUROC2 working document

Last update: 18/06/2021

General description

LAUROC2 (Liquid Argon Upgrade ReadOut Chip) is designed in CMOS 130 nm technology for the phase II of the high luminosity Large Hadron Collider at CERN. It integrates four analog front end channels and one sum channel.

Each front-end channel consists of a preamplifier followed by a High-Gain (HG) and Low-Gain (LG) CRR2 differential shaper. The two gains shaper accommodate the large dynamic range of the LAr signals with detector currents reaching up to 10 mA and detector capacitances ranging from 300 pF to 1.5 nF. The sum channel provides an analog sum of the 4 channels and so differential trigger outputs that are first sent to « Layer Sum Boards (LSB) » located on the FEB board, and then sent to the « Lar trigger system (LTD: LAr Trigger Digitizer Boards) ».

The ASIC general architecture is shown in Figure 1 and Figure 2. It integrates 4 front-end channels (Ch<1:4>). An additional channel (Ch <5>) has been integrated only for specific tests.

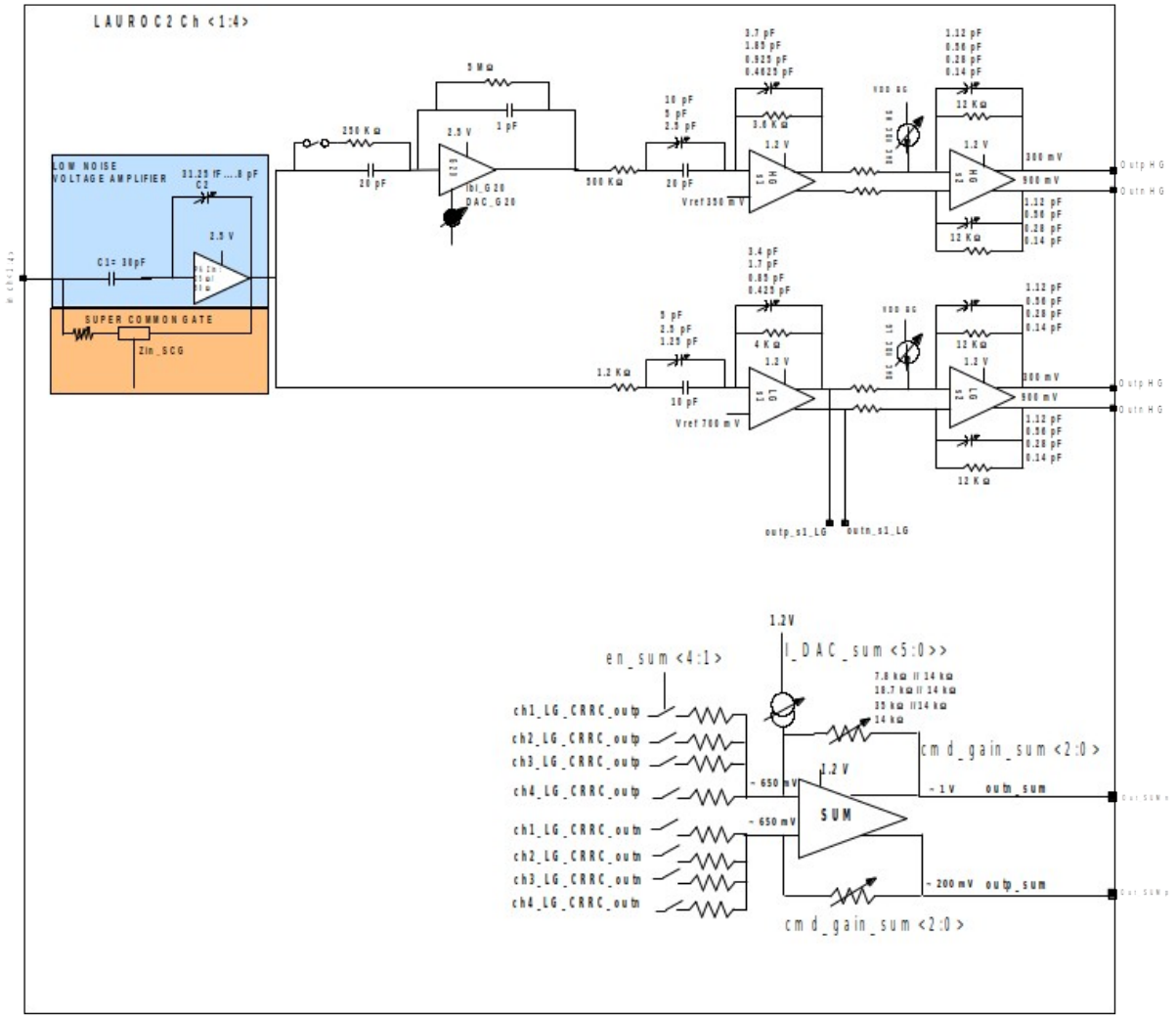


Figure 1 LAUROC2 schematic channels <1 :4>

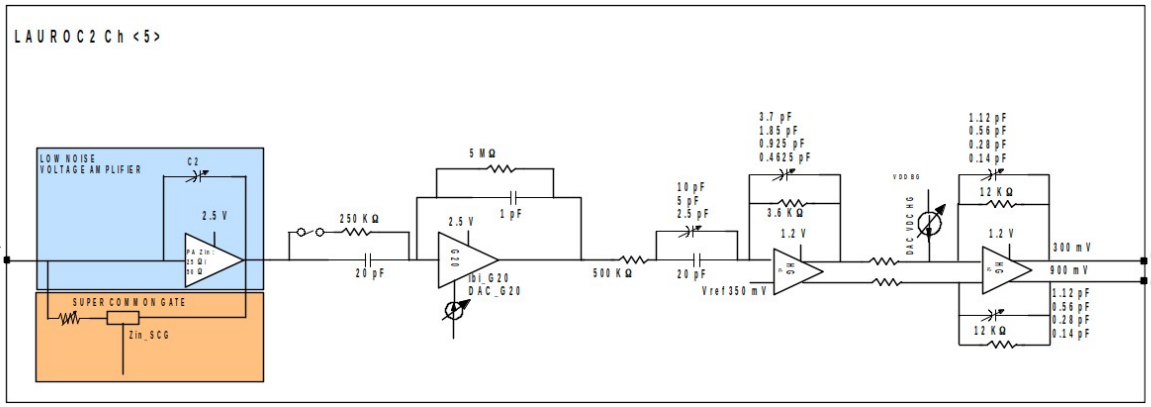


Figure 2 LAUROC2 schematic channel <5>

The front end channel is built around a preamplifier (Figure 3) with a tuneable input impedance (25 or 50 Ohm). The 4 channels (channel <1:4>) are identical. The preamp is followed by a HG and a LG differential CRRC2 shaper (shaper amplifier designed by BNL). The first stage of the LG shaper that corresponds to the CRRC output of the four channels are

summed in the SUM block. An extra RC shaping will be included in the LTDB board to slow down the signal if needed.

Channel 5 is an extra channel used for “academic” tests. It integrates a similar preamplifier as the one integrated in the 4 other front-end channels but without the input capacitance C1. This capacitor will be soldered externally to study the preamplifier noise. The preamplifier is followed by a HG CRRC2 shaper.

The preamplifier

The input preamplifier, which is current sensitive due to the long signal duration (600 ns) of the liquid argon pulse, is built around a classical cascode configuration with a large input transistor.

The input impedance (Zin) has to be precisely matched to the cable impedance bringing the signals out of the cryostat (25 and 50 Ohm). This line termination of the preamplifier is done using a resistor (R0) in series with a Super Common Gate amplifier (SCG) in the feedback of a low noise voltage amplifier. The input impedance is then given by the following formula:

$$Z \in PA = \frac{R0 + Zin(SCG)}{1 + |G|}$$

Where G=C1/C2 and with C2 tuneable on 9 bits (C2<8:0>) (LSB= 31.25 fF) . The input impedance Zin is therefore tuneable on 9 bits using SC parameters.

The two main advantages of this architecture are that the voltage gain is made using capacitors that have a much lower noise contribution than resistors and the equivalent noise of R0 is divided by the square of the gain $4kTR0/(1+|G|)^2$, while the input impedance is only given by R0 divided by the gain. The feedback also ensures that the input impedance does not vary with the signal amplitude.

The preamp used for channel <5> is identical to the one used for channel <1:4> except to the input capacitance C1. The C1 will be soldered on the board to study the origin of 1/f noise observed in the LAUROC1 version.

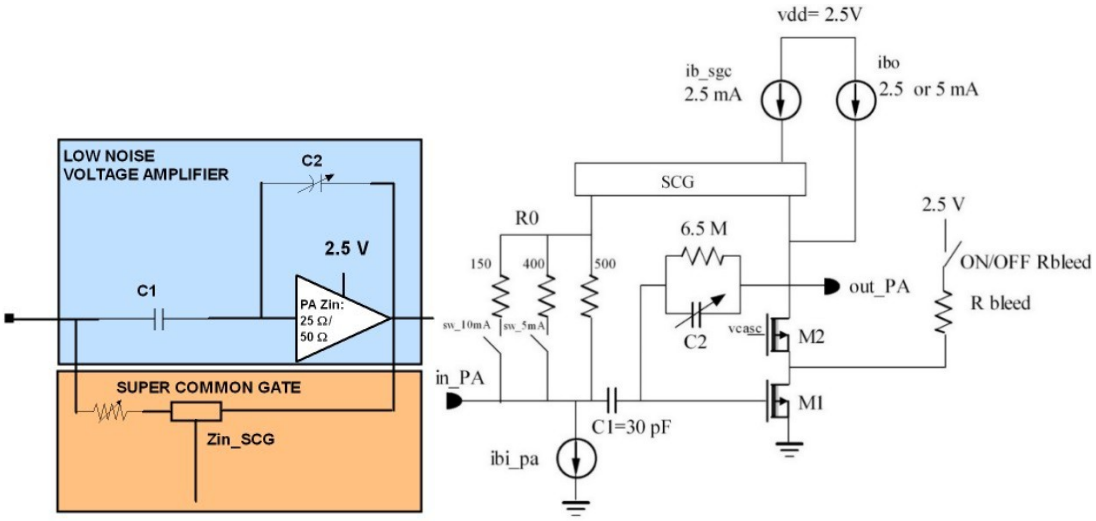


Figure 3 Preamplifier schematic

	SW_R0_10m	SW_R0_5m	R0 equivalent	Gain (formula)	C2 (formula)	C2 (decimal)
50 □ □□ mA	0	0	500 □	9	3.3 pF	107
25 □ □□ □mA	1	0	150//500= 115 □	3.6	8.3 pF	266

Table 1 : 25 Ohm/50 Ohm configuration bits

HG and LG channels

The preamplifier (of channel <1:4>) is followed by a HG and a LG CRRC2 differential shaper. The two-gain shaper accommodates the large dynamic range of the LAr signals to the external 14-bit ADC. Their bipolar waveform optimizes the signal to noise ratio in the presence of the anticipated pileup and acts as anti-aliasing for the following 40 MHz ADC. The HG path is made of an amplifier with a gain of ~17 (named “G20 amplifier”) followed by the HG CRRC2 shaper (Figure 4).

The amplifier can be coupled to the preamplifier using AC or DC mode: this choice is done using a SC parameter (sw_DC_g20, Table 6). The DC coupling mode is important to avoid baseline shift with saturated events. A 6-bit DAC (dac_g20<5:0>, Table 6) allows to tune the current (named ibi_G20) that flows in the G20 amplifier and so to adjust the DC level of the G20 amplifier output.
The DC tuning of the G20 amplifier is given by the following formula:

$$VDC_{out\_G20} = 5\ M\Omega \times (ibi\_G20 + (DC_{PA} - DC_{G20})/250\ K\Omega$$

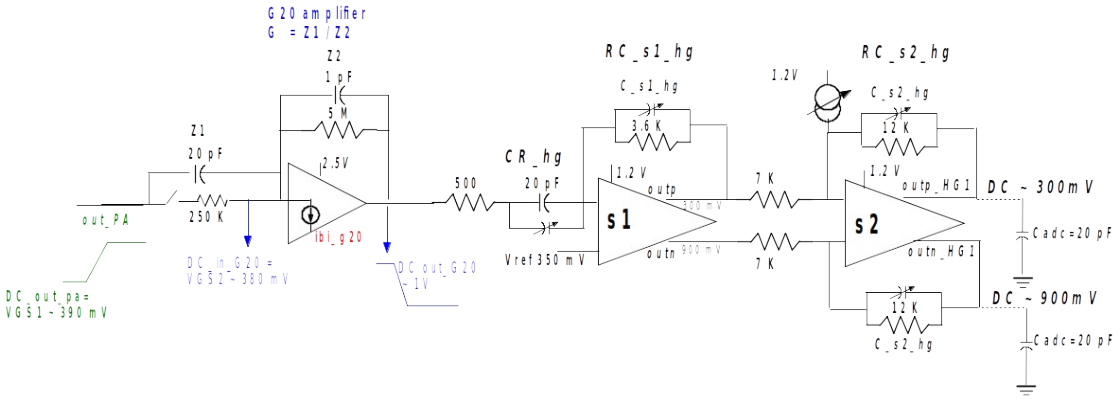


Figure 4: High Gain path: G20 amplifier + CRRC2

The LG path is made of a CRRC2 shaper. Both CRRC2 shapers have a variable Ƭ: 4 bits (LSB= 1.7 ns). CR tuning independent of RC tuning. See SC parameters in Table 6: cr_hg_s1<0 :2>, rc_hg_s1<0 :3>, rc_hg_s2<0 :3>, cr_lg_s1<0 :2>, rc_lg_s1<0 :3>, rc_lg_s2<0 :3>

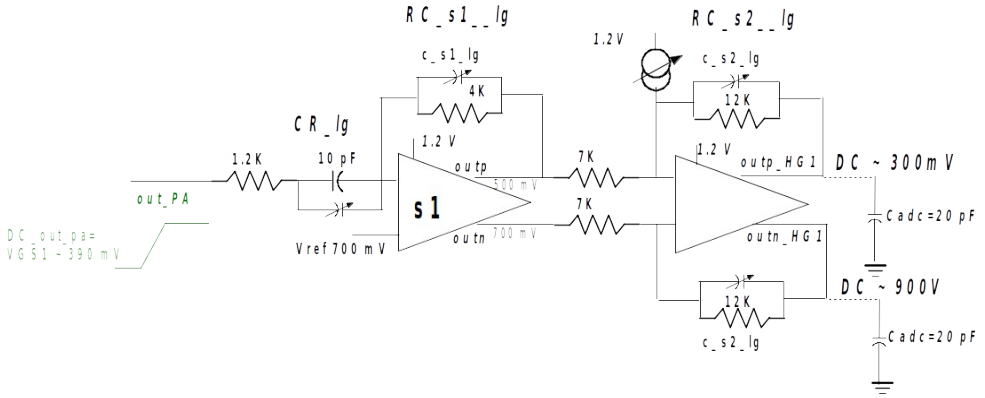


Figure 5: CRRC2 Low Gain path

HG C1R1			
Code	C (pF)	R (Ω)	τ (ns)
0	***20***	***500***	***10***
1	22,5	***500***	11,25
2	*25*	*500*	*12,5*
3	27,5	*500*	13,75
4	30	*500*	15
5	32,5	*500*	16,25
6	35	*500*	17,5
7	37,5	*500*	18,75

HG R1C1			
Code	C (pF)	R (Ω)	τ (ns)
0	0	3600	0,0
1	0,462	3600	1,7
2	0,924	3600	3,3
3	1,386	3600	5,0
4	1,848	3600	6,7
5	2,31	3600	8,3
6	2,772	3600	10,0
7	3,234	3600	11,6
8	3,696	3600	13,3
9	***4,158***	***3600***	***15,0***
10	4,62	3600	16,6
11	5,082	3600	18,3
12	5,544	3600	20,0
13	6,006	3600	21,6
14	6,468	3600	23,3
15	6,93	3600	24,9

HG R2C2			
Code	C (pF)	R (Ω)	τ (ns)
0	0	12000	0
1	0,14	12000	1,68
2	0,28	12000	3,36
3	0,42	12000	5,04
4	0,56	12000	6,72
5	0,7	12000	8,4
6	0,84	12000	10,08
7	0,98	12000	11,76
8	1,12	12000	13,44
9	***1,26***	***12000***	***15,12***
10	1,4	12000	16,8
11	1,54	12000	18,48
12	1,68	12000	20,16
13	1,82	12000	21,84
14	1,96	12000	23,52
15	2,1	12000	25,2

Table 2 : CR RC parameters for the HG channel

LG C1R1			
Code	C (pF)	R (Ω)	τ (ns)
0	10	1200	12
1	11,25	1200	13,5
2	***12,5***	***1200***	***15***
3	13,75	1200	16,5
4	15	1200	18
5	16,25	1200	19,5
6	17,5	1200	21
7	18,75	1200	22,5

LG R1C1			
Code	C (pF)	R (Ω)	τ (ns)
0	0	4000	0,0
1	0,425	4000	1,7
2	0,85	4000	3,4
3	1,275	4000	5,1
4	1,7	4000	6,8
5	2,125	4000	8,5
6	2,55	4000	10,2
7	2,975	4000	11,9
8	3,4	4000	*13,6*
9	***3,825***	***4000***	***15,3***
10	4,25	4000	17,0
11	4,675	4000	18,7
12	5,1	4000	20,4
13	5,525	4000	22,1
14	5,95	4000	23,8
15	6,375	4000	25,5

LG R2C2			
Code	C (pF)	R (Ω)	τ (ns)
0	0	12000	0
1	0,14	12000	1,68
2	0,28	12000	3,36
3	0,42	12000	5,04
4	0,56	12000	6,72
5	0,7	12000	8,4
6	0,84	12000	10,08
7	0,98	12000	11,76
8	1,12	12000	13,44
9	***1,26***	***12000***	***15,12***
10	1,4	12000	16,8
11	1,54	12000	18,48
12	1,68	12000	20,16
13	1,82	12000	21,84
14	1,96	12000	23,52
15	2,1	12000	25,2

Table 3 : CR RC parameters for the LG channel

SUM block

The new LAr L1 trigger system will still be used as a L0 system at the HL-LHC. So the analog signals of four neighboring cells in a given layer should be summed together. Consequently the ASIC will provide the sum of the 4 channels, giving an additional output.

The CRRC LG outputs of the four channels are summed in the SUM block. The SUM block has a variable gain thanks to a system of switchable resistors (Figure 6). The gain is given by the ratio between the feedback resistor, which is variable (R= [5kΩ, 8 kΩ, 10 kΩ, 14 kΩ]) and the input resistor fixed at R= 2 kΩ. A 6-bit input DAC (DAC_VDC_sum) allows to adapt the DC levels of the differential outputs (out_SUMp and out_SUMn).

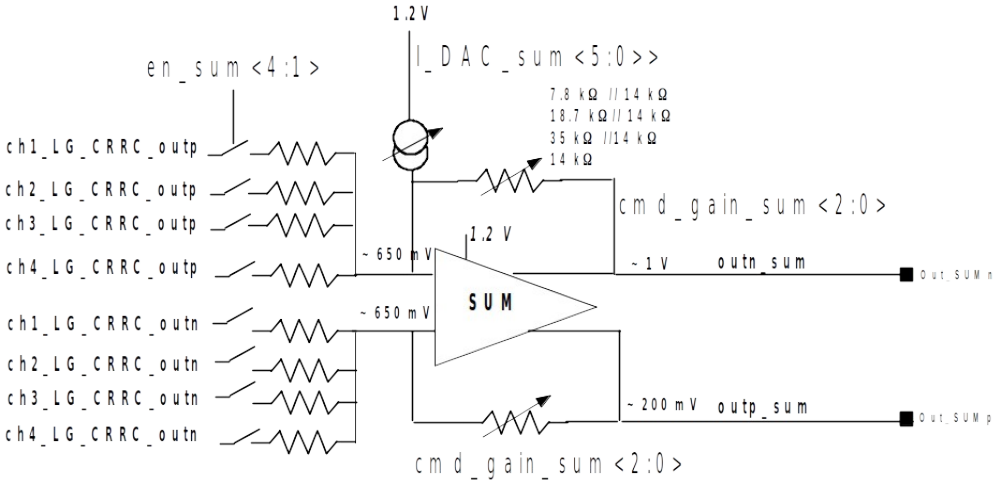


Figure 6 SUM general schematic

The chip dimensions are: 3200µm x 2000µm, 750 µm thick

It is packaged in a LQFP 128 14*14 package.

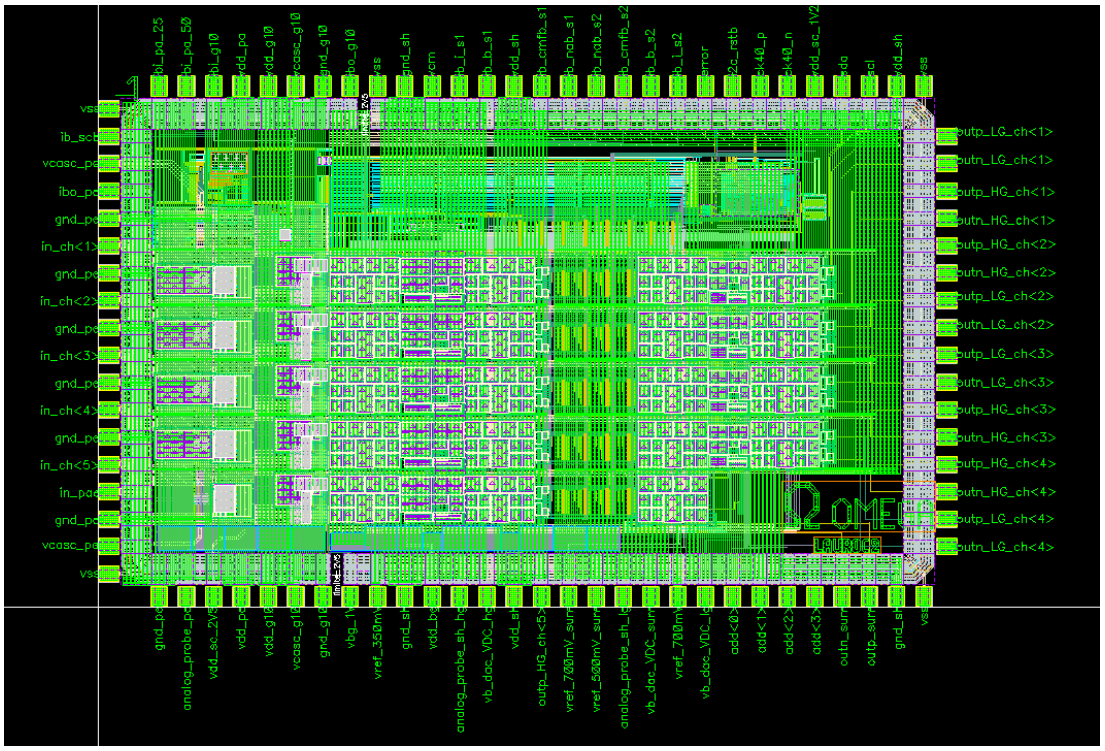


Figure 7: Layout of LAUROC2 (size 3.2 mm x 2 mm)

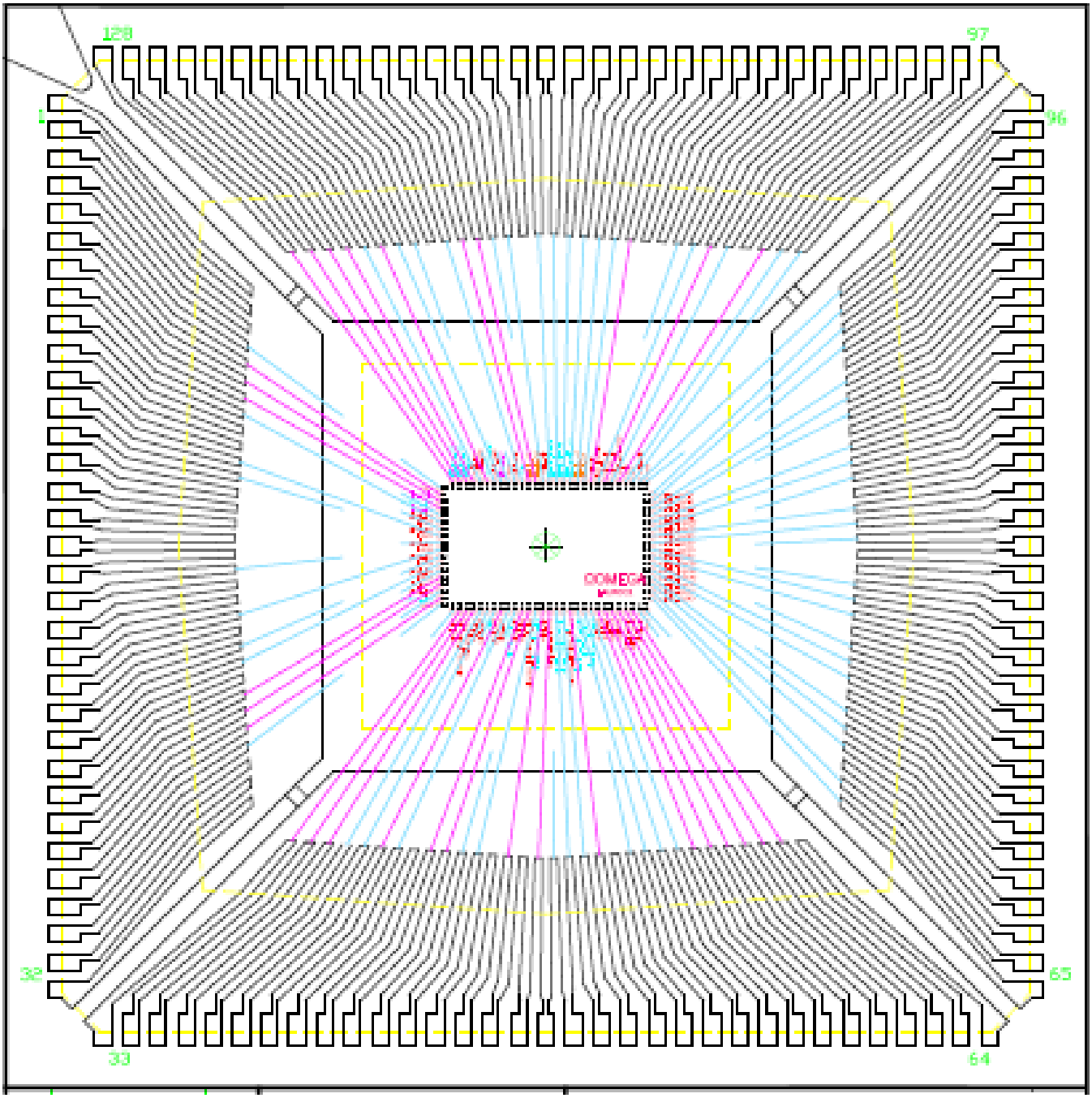


Figure 8: Bonding diagram of Lauroc2 in LQFP128 14x14

Pin list

		LAUROC2		Comments		sim
	Pin_number	Pin_name	Pin_type	Bias/power Ref	Decoupling Capacitor recommended on board	
WEST	1	NC	NC			
	2	NC	NC			
	3	NC	NC			
	4	vss	GROUND			
	5	ib_scb	ANALOG	Bias/2V5/1.8kΩ to gnd (1mA)	100nF/2,5V	1.824
	6	vcasc_pa	ANALOG	Bias/2V5/9kΩ to gnd +16kΩ to VDD	100nF/GND	0.9
	7	ibo_pa	ANALOG	Bias/2V5/600Ω to gnd (2.5 mA or 5mA if sw_ibo)	100nF/2,5V	1.663
	8	in_ch<1>	INPUT			
	9	NC	NC			
	10	NC	NC			
	11	in_ch<2>	INPUT			
	12	vss	GROUND			
	13	NC	NC			
	14	NC	NC			
	15	NC	NC			
	16	NC	NC			
	17	NC	NC			
	18	vss	GROUND			
	19	NC	NC			
	20	NC	NC			
	21	in_ch<3>	INPUT			
	22	NC	NC			
	23	vss	GROUND			
	24	in_ch<4>	INPUT			
	25	NC	NC			
	26	in_ch<5>	INPUT			
	27	in_pac	INPUT			
	28	vcasc_pa	ANALOG	Bias/2V5	100nF/GND	1.663
	29	vss	GROUND			
	30	NC	NC			
	31	NC	NC			
	32	NC	NC			
SOUTH	33	analog_probe_pa	OUTPUT			
	34	vdd_sc_2V5	POWER_2V5			
	35	vdd_pa	POWER_2V5			
	36	vdd_g10	POWER_2V5			
	37	vcasc_g10	ANALOG	Bias/2V5/90kΩ to gnd +160kΩ to VDD	100nF/GND	0.904
	38	vbg_1V	ANALOG			0.923
	39	vref_350mV	ANALOG	Bias/1V/30kΩ to gnd +49.5kΩ to VBG	100nF/GND	0.352
	40	NC	NC			
	41	vdd_bg	POWER_1V2			
	42	analog_probe_sh_hg	OUTPUT			
	43	vss	GROUND			
	44	vb_dac_VDC_hg	ANALOG	Bias/1V2/3kΩ to gnd	100nF/GND	0.709
	45	NC	NC			
	46	vdd_sh	POWER_1V2			
	47	NC	NC			
	48	outp_HG_ch<5>	OUTPUT			
	49	vss	GROUND			
	50	vref_700 mV_sum	ANALOG	Bias/1V/50kΩ to gnd +15.7kΩ to VBG	100nF/GND	0.704
	51	vref_500 mV_sum	ANALOG	Bias/1V/40kΩ to gnd +33.4kΩ to VBG	100nF/GND	0.506
	52	analog_probe_sh_lg	OUTPUT			
	53	NC	NC			
	54	vss	GROUND			
	55	vb_dac_VDC_sum	ANALOG	Bias/1V2/3kΩ to gnd	100nF/GND	0.438
	56	vref_700 mV	ANALOG	Bias/1V/50kΩ to gnd +15.7.5kΩ to VBG	100nF/GND	0.704
	57	vb_dac_VDC_lg	ANALOG	Bias/1V2/3kΩ to gnd	100nF/GND	0.677
	58	add<0>	DIGITAL INPUT	1V2 or GND		
	59	add<1>	DIGITAL INPUT	1V2 or GND		
	60	add<2>	DIGITAL INPUT	1V2 or GND		
	61	add<3>	DIGITAL INPUT	1V2 or GND		
	62	outn_sum	OUTPUT			
	63	outp_sum	OUTPUT			
	64	NC	NC			

EAST	65	outn_LG_ch<4>	OUTPUT			
	66	outp_LG_ch<4>	OUTPUT			
	67	NC	NC			
	68	outn_HG_ch<4>	OUTPUT			
	69	outp_HG_ch<4>	OUTPUT			
	70	vss	GROUND			
	71	NC	NC			
	72	outn_HG_ch<3>	OUTPUT			
	73	outp_HG_ch<3>	OUTPUT			
	74	vss	GROUND			
	75	NC	NC			
	76	outn_LG_ch<3>	OUTPUT			
	77	outp_LG_ch<3>	OUTPUT			
	78	vss	GROUND			
	79	NC	NC			
	80	NC	NC			
	81	vss	GROUND			
	82	outn_LG_ch<2>	OUTPUT			
	83	outp_LG_ch<2>	OUTPUT			
	84	NC	NC			
	85	vss	GROUND			
	86	outn_HG_ch<2>	OUTPUT			
	87	outp_HG_ch<2>	OUTPUT			
	88	NC	NC			
	89	vss	GROUND			
	90	outn_HG_ch<1>	OUTPUT			
	91	outp_HG_ch<1>	OUTPUT			
	92	NC	NC			
	93	vss	GROUND			
	94	outn_LG_ch<1>	OUTPUT			
	95	outp_LG_ch<1>	OUTPUT			
	96	vdd_sh	POWER_1V2			
NORTH	97	scl	DIGITAL INPUT	GND; 1V2		
	98	sda	DIGITAL I/O	GND; 1V2		
	99	vdd_sc_1V2	POWER_1V2			
	100	NC	NC			
	101	ck40_n	DIGITAL INPUT	differential clock 800mV;400mV Common mode voltage=600mV		
	102	ck40_p	DIGITAL INPUT			
	103	i2c_rstb	DIGITAL INPUT	GND=reset; 1V2=not reset		
	104	vss	GROUND			
	105	NC	NC			
	106	NC	NC			
	107	i2c_error	DIGITAL OUTPUT			
	108	ib_i_s2	ANALOG	Bias/1V2/600Ω to gnd (2.5mA)	100nF/1,2V	0.764
	109	ib_b_s2	ANALOG	Bias/1V2/760Ω VDD (1mA)	100nF/1,2V	0.762
	110	ib_cmfb_s2	ANALOG	Bias/1V2/704Ω VDD (1mA)	100nF/GND	0.499
	111	ib_nab_s2	ANALOG	Bias/1V2/9kΩ VDD (100µA)	100nF/GND	0.337
	112	ib_nab_s1	ANALOG	Bias/1V2/9kΩ VDD (100µA)	100nF/GND	0.337
	113	ib_cmfb_s1	ANALOG	Bias/1V2/704Ω VDD (1mA)	100nF/GND	0.498
	114	NC	NC			
	115	vdd_sh	POWER			
	116	vss	GROUND			
	117	ib_b_s1	ANALOG	Bias/1V2/760Ω VDD (1mA)	100nF/1,2V	0.762
	118	ib_i_s1	ANALOG	Bias/1V2/300Ω to gnd (2.5mA)	100nF/1,2V	0.764
	119	vcm	ANALOG	Bias/1V/61kΩ to gnd +32.5kΩ to VDD	100nF/GND	0.606
	120	NC	NC			
	121	vss	GROUND			
	122	ibo_g10	ANALOG	Bias/2V5/600Ω to gnd (3 mA or 6mA if sw_ibo_g10)	100nF/2,5V	1.614
	123	vcasc_g10	ANALOG	Bias/2V5/90kΩ to gnd +160kΩ to VDD	100nF/GND	0.904
	124	vdd_g10	POWER_2V5			
	125	vdd_pa	POWER_2V5			
	126	ibi_g10	ANALOG	Bias/2V5/variable by DAC_g10 <0:5>	100nF/GND	0.441
	127	ibi_pa_50	ANALOG	Bias/2V5/92kΩ to VDD (20 µA)	100nF/GND	0.646
	128	ibi_pa_25	ANALOG	Bias/2V5/9kΩ to VDD (200 µA)	100nF/GND	0.732

Table 4 Pin list

In the table below the list of the external components to add on the board to adapt some bias and reference levels for the measurements.

39	**vref_350mV**	**ANALOG**	Bias/1V/30kΩ to gnd +49.5kΩ to VBG	**65kΩ to GND**
101	**ck40_n**	**DIGITAL INPUT**	differential clock 800mV;400mV; Common mode voltage=600mV	**100Ω between ck40-n (pin101)**
102	**ck40_p**	**DIGITAL INPUT**		**and ck40-p (pin102)**
119	**vcm**	**ANALOG**	Bias/1V/61kΩ to gnd +32.5kΩ to VDD	**100kΩ to VBG pin38**
126	**ibi_g10**	**ANALOG**	Bias/2V5/variable by DAC_g10 <0:5>	**470kΩ to2.5V**

Table 5 External resistors to add for the measurements

I2C

I2C protocol is used to configure the ASIC. The I2C protocol used has been developed by CERN and modified by Omega team to have extended addressing.

The I2C I/0 are given in the table below:

I/O pads		comments	
SCL	Serial Clock Line	Input, 1MHz	Pull up (inside or outside)
SDA	Serial Data Line	bidirectional	Pull up (inside or outside)
Resetb_sc	Reset I2C top manager and set default values	Input, Active 'LO'	
CLK_SM_I2C	State machine clock	Input, 40MHz	
Chip_id<3:0>	4b to identify chip	Input	

Table 6 : I2C I/O

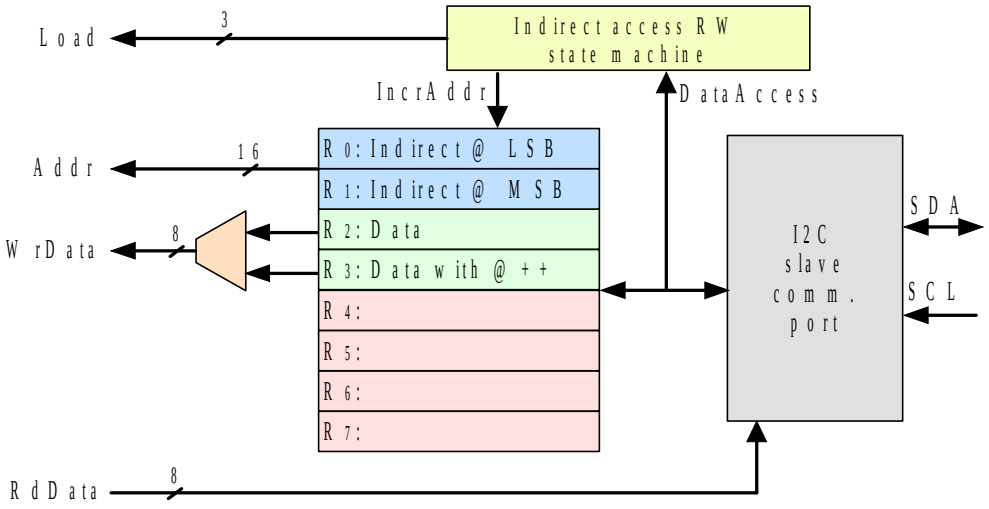
Logic levels: Low= 0 V and High=1.2 V

The I2C protocol main features are given in the table below:

I2C	Detail	Comments
Chip addressing (Chip_id)	4 bits	MSB of I2C first byte
Direct access register addressing	3 bits	Register R0 to R7
Write/read	1 bit	Write='0'; Read='1'
"Burst" writing/ reading	Yes	Accessible through R3
I2C speed	1 MHz (max)	
TMR	yes	

Table 7: I2C main features

The I2C used in the chip has 8 internal registers: R0 to R7. Inside the ASIC, some of them are connected to manage slow control. 8 bits can be written in each internal register.



I2C internal register	Data inside the register	Comments
R0	ASIC parameter address (LSB)	Indirect @
R1	ASIC parameter address 'MSB)	Indirect @
R2	Data	
R3	Data with auto @++	Increment indirect @ after each access
R4-R5-R6	Direct access SC register	
R7	Status register (reg_R7<0>=error, reg_R7<1>=parity)	Read only

Figure 9 : I2C registers

The frame of the I2C protocol is always the same:

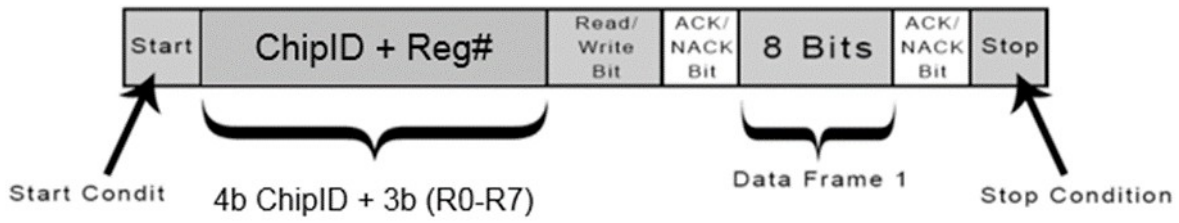
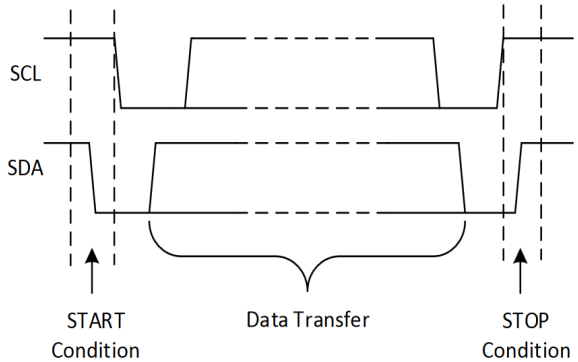


Figure 9 : I2C frame

The master sends a start condition on the bus with the slave address (Chip_id) + I2C register + last bit set to 0, which indicates that it is "a write sequence". Then the slave acknowledges at 0 if the Chip_id is identified. Then the master sends the register data to the slave.

START and STOP condition:



The I2C communication is initiated by the master by sending a START condition and terminated by the master by sending a STOP condition.
START condition: a high-to-low transition on the SDA line while the SCL is high.
STOP: condition: a low-to-high transition on the SDA line while the SCL is high.

Figure 10 : I2C start and stop condition

Data transfer format:

One data bit is transferred during each SCL clock. One byte is comprised of 8 bits on SDA line.
A byte may either be a device address, register address, or data written (R/W bit=0) to or read (R/W bit=1) from a slave. Data are transferred with MSB first.
Data on the SDA line must remain stable during the high phase of the clock period. Any change in the data line while SCL is high is interpreted as a control command (START or STOP).

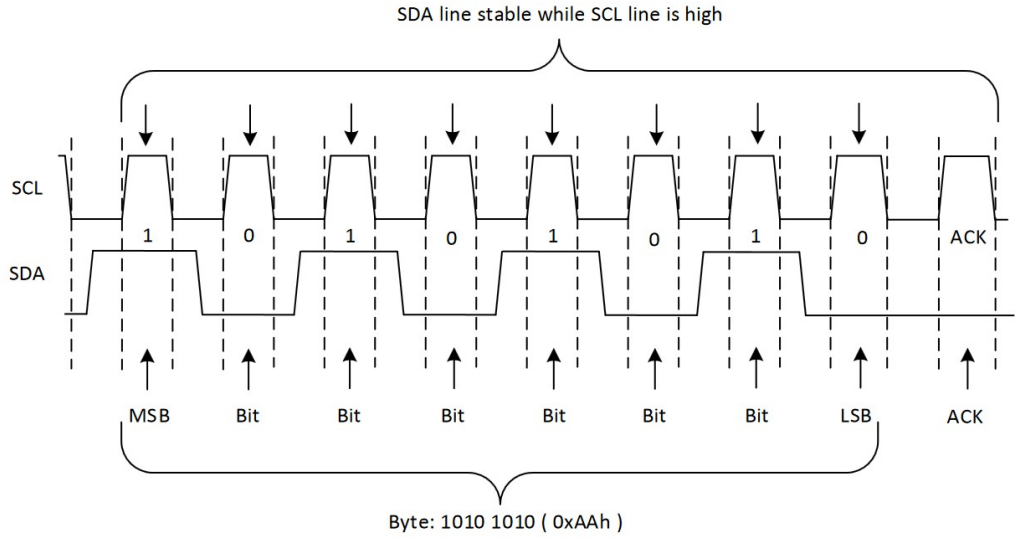


Figure 11 : SCL and SCA diagram

I2C slow control inside the ASIC

Inside LAUROC2, all slow control bits are grouped by 8 and each group is identified by a sub_address called DataIn_enable. The DataIn_enable is defined by the data written in register R1 (MSB) and R0 (LSB).

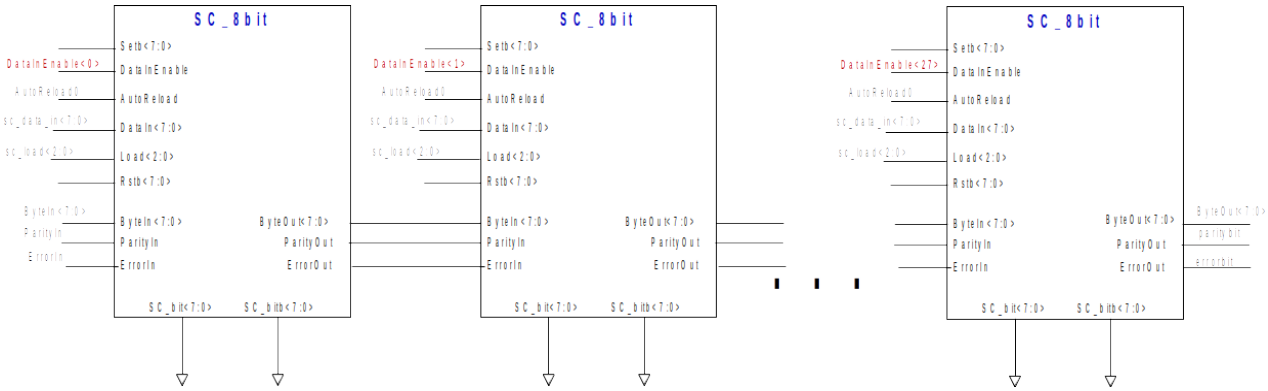


Figure 12 : Slow control chain

AutoReload0 is done by reg_R4<7>. If AutoReload is '1', we force the latch output to be reloaded if an error occurs.
SC_data_in<7:0> is given by the data written in R2 or R3. This data is the slow control data for SC_8bit identified by the DataIn_enable.
Other input signals are managed by the I2C state machine.

In LAUROC2, only 27 DataIn_enable are used:

Data in R0= DataIn_enable from DataIn_enable [0] to DataIn_enable[26]
Data in R1= always 0
Data in R2= slow control data for SC_8bit cell

For instance, to set a specific 8 bit word in the chip, the user must write in the R0 register, then in the R1 register to select the right parameters register address, and then write the data in the R2 register.

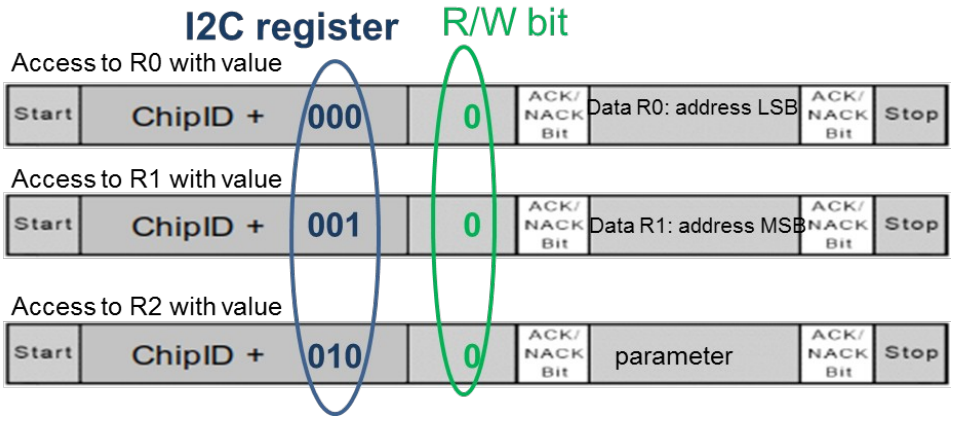


Figure 13 : I2C R0, R1, R2

Example to write:

Chip Id= 5 => pin 58 = add<0> = 1.2V; pin 59 = add<1> = 0V; pin 60 = add<3> =1.2V; pin 61 = add<3> =0V

Assuming the user wants to write data=9 on DataIn_enable = 4:

SCL and SDA scope frames :

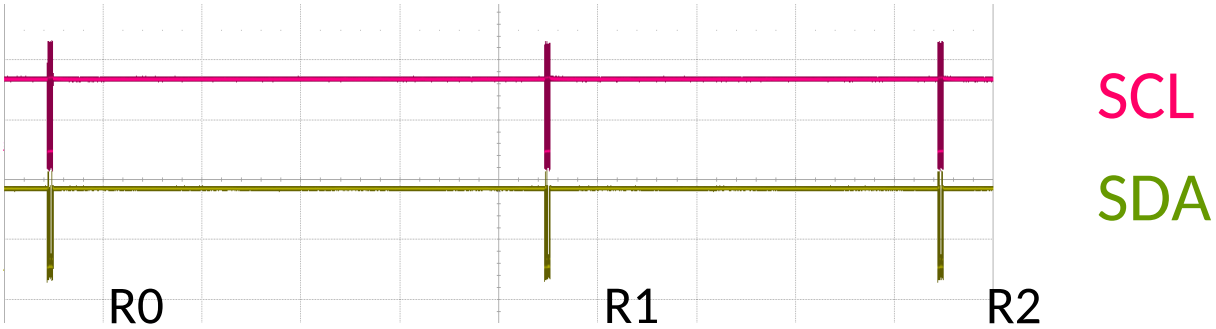


Figure 14 LAUROC2 I2C frame WRITE. Oscilloscope signals.

R0 Zoom: Data in R0 is 4 in order to select DataIn_enable[4]

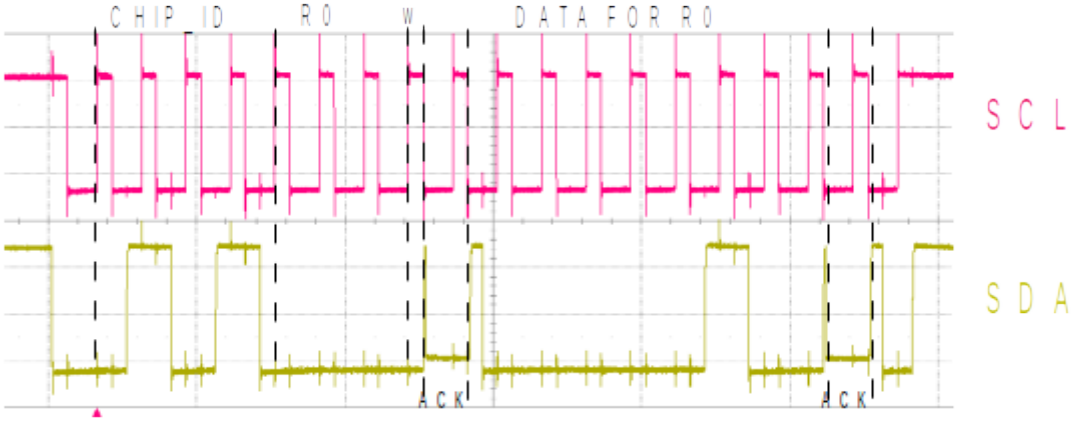


Figure 15 : ZOOM on the Register R0

R1 Zoom: Data in R1 is 0

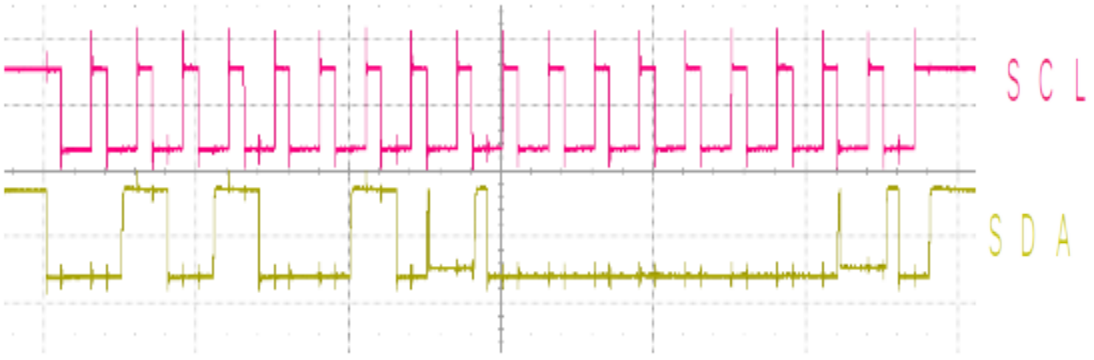


Figure 16 : ZOOM on the Register R1

R2 Zoom: data in R2 is 9

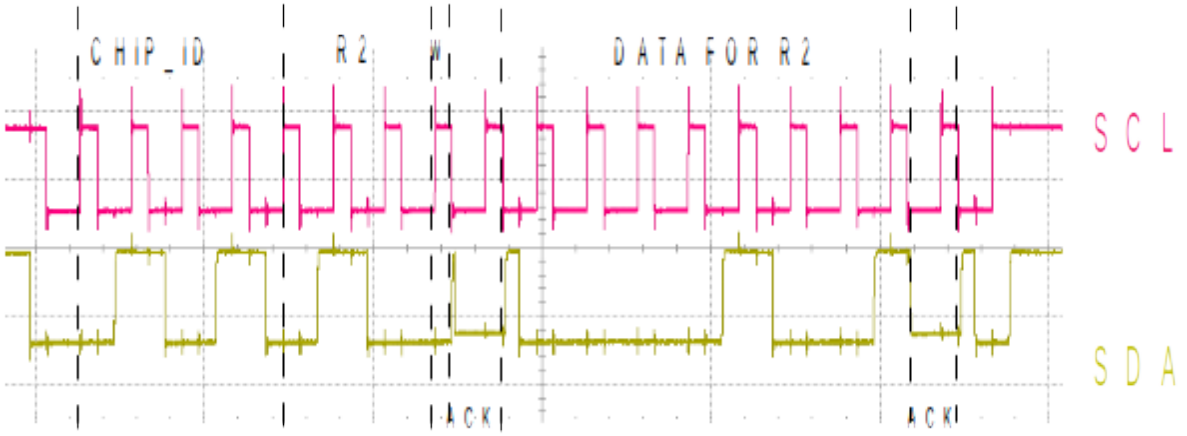


Figure 17 : ZOOM on the Register R2

If LAUROC2 identifies its chip_ID, the acknowledge is set to 0V otherwise acknowledge is 1.2V

Another way to send slow control is described below.

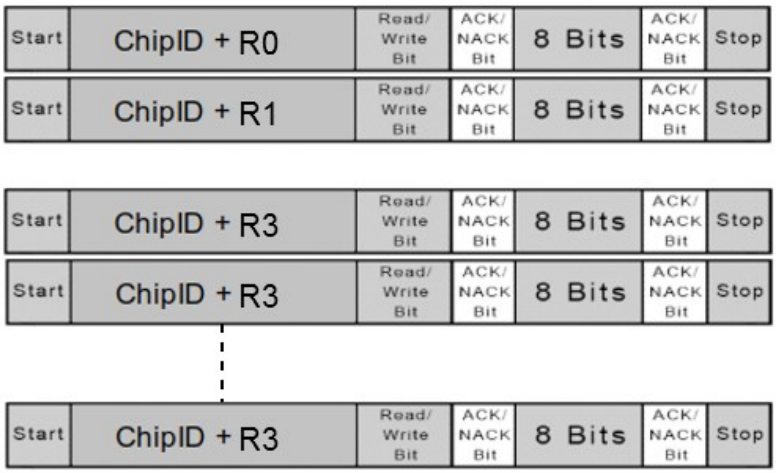


Figure 18 I2C write frame in R3

The user can also write in consecutive parameters register addresses: rather to write the parameters in the R2 register, he has to write successively in the R3 register.

<u>Example to read:</u>

Chip Id= 5

Assuming the user wants to read on DataIn_enable = 9:

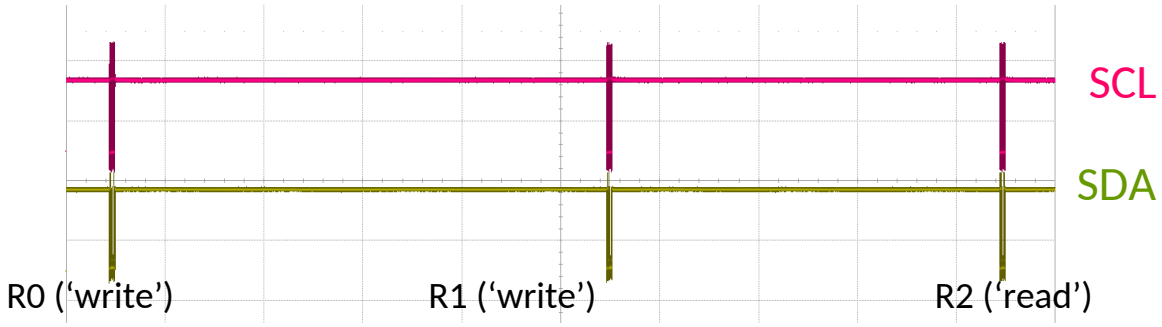


Figure 20 LAUROC2 I2C frame READ. Oscilloscope signals.

R0 Zoom: Data in R0 is 9 in order to select DataIn_enable[9]

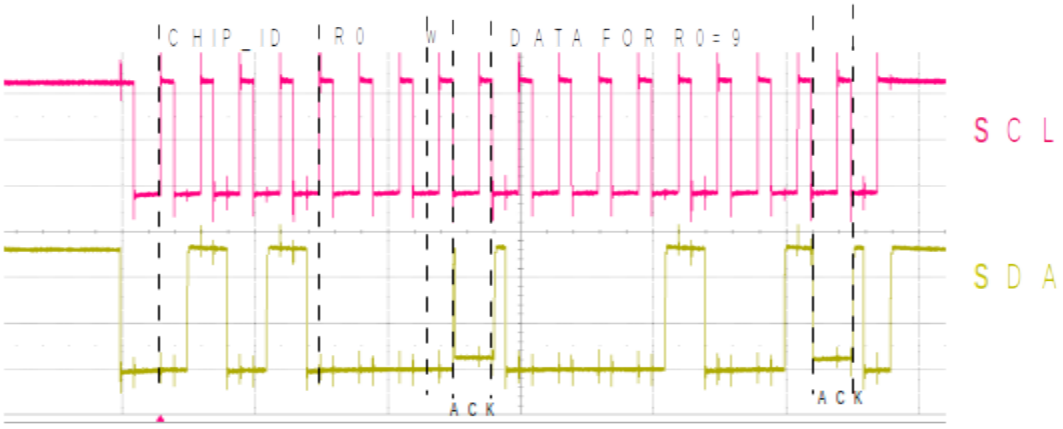


Figure 21 : ZOOM on the Register R0

R1 Zoom: Data in R1 is 0

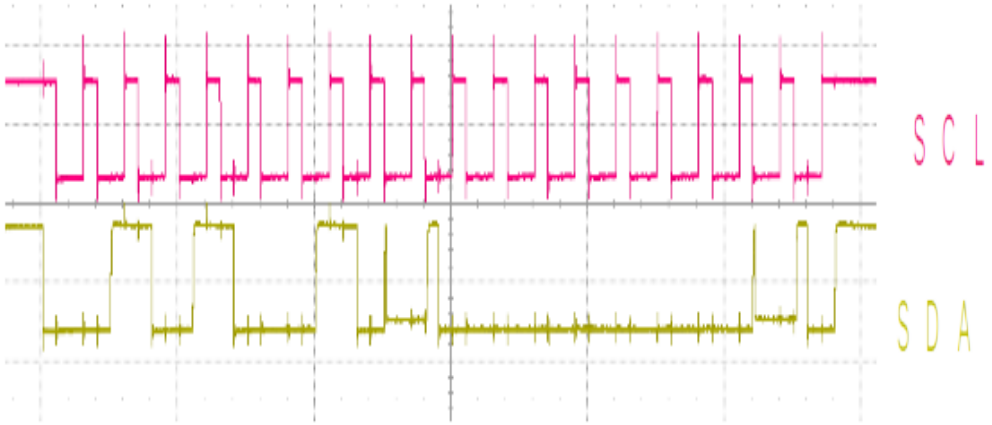


Figure 22 : ZOOM on the Register R1

R2 Zoom: data in R2 is READ

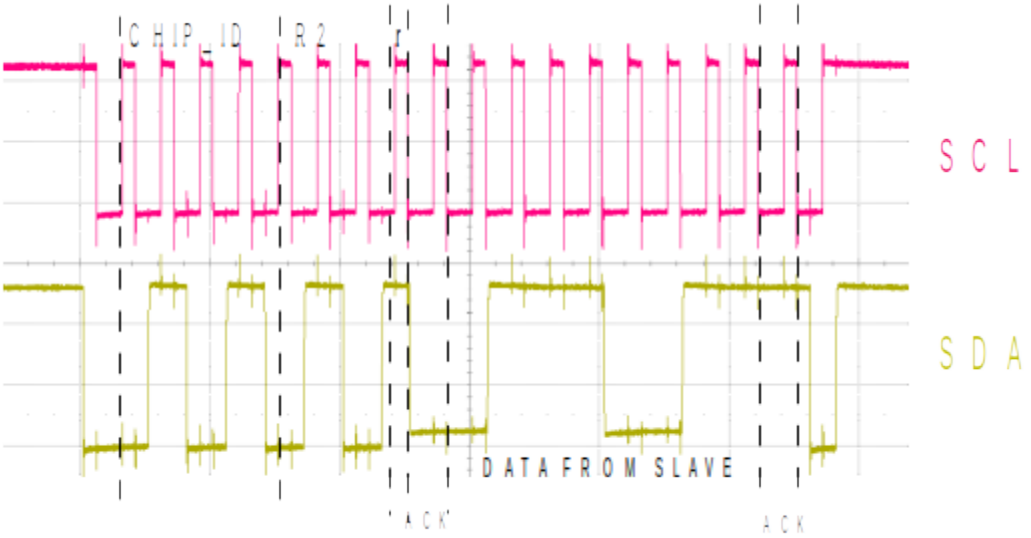


Figure 23 : ZOOM on the Register R2

In this case, data read in DataIn_enable[9]=115=[01110011] (default value done in the next table)

ASIC configuration parameters

				Default values
BIAS	**DataIn_Enable <0>**	sc_bit_7	en_probe_vref_700mV	0
		sc_bit_6	en_probe_vref_700mV_sum	0
		sc_bit_5	en_probe_vref_500mV_sum	0
		sc_bit_4	en_probe_vddsh	0
		sc_bit_3	en_probe_vcm	0
		sc_bit_2	en_probe_vref_350mV	0
		sc_bit_1	en_probe_vbg_1V	0
		sc_bit_0	en_probe_vbg_900mV	0
	DataIn_Enable <1>	sc_bit_7	ON_g20	1
		sc_bit_6	ON_ref_bg	1
		sc_bit_5	ON_Rbleed	1
		sc_bit_4	ON_pa	1
		sc_bit_3	ON_lg_s1	1
		sc_bit_2	ON_hg_s1	1
		sc_bit_1	ON_lg_s2	1
		sc_bit_0	ON_hg_s2	1
	DataIn_Enable <2>	sc_bit_7	sw_DC_g20	0
		sc_bit_6	sw_ibo_g20	0
		sc_bit_5	dac_g20<5>	1
		sc_bit_4	dac_g20<4>	1
		sc_bit_3	dac_g20<3>	0
		sc_bit_2	dac_g20<2>	0
		sc_bit_1	dac_g20<1>	0
		sc_bit_0	dac_g20<0>	0
	DataIn_Enable <3>	sc_bit_7	NC	1
		sc_bit_6	NC	1
		sc_bit_5	NC	1
		sc_bit_4	NC	1
		sc_bit_3	sw_ibi_25	1
		sc_bit_2	sw_ibo	0
		sc_bit_1	sw_R025_10mA	1
		sc_bit_0	sw_R025_5mA	0
	DataIn_Enable <4>	sc_bit_7	cr_hg_s1<2>	0
		sc_bit_6	cr_hg_s1<1>	0
		sc_bit_5	cr_hg_s1<0>	0

		sc_bit_4	NC	0
		sc_bit_3	rc_hg_s1<3>	1
		sc_bit_2	rc_hg_s1<2>	0
		sc_bit_1	rc_hg_s1<1>	0
		sc_bit_0	rc_hg_s1<0>	1
	DataIn_Enable <5>	sc_bit_7	rc_hg_s2<3>	1
		sc_bit_6	rc_hg_s2<2>	0
		sc_bit_5	rc_hg_s2<1>	0
		sc_bit_4	rc_hg_s2<0>	1
		sc_bit_3	rc_lg_s2<3>	1
		sc_bit_2	rc_lg_s2<2>	0
		sc_bit_1	rc_lg_s2<1>	0
		sc_bit_0	rc_lg_s2<0>	1
	DataIn_Enable <6>	sc_bit_7	cr_lg_s1<2>	0
		sc_bit_6	cr_lg_s1<1>	1
		sc_bit_5	cr_lg_s1<0>	0
		sc_bit_4	NC	0
		sc_bit_3	rc_lg_s1<3>	1
		sc_bit_2	rc_lg_s1<2>	0
		sc_bit_1	rc_lg_s1<1>	0
		sc_bit_0	rc_lg_s1<0>	1
	DataIn_Enable <7>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	ON_ref_sum	1
		sc_bit_4	en_sum_<4>	1
		sc_bit_3	en_sum_<3>	1
		sc_bit_2	en_sum_<2>	1
		sc_bit_1	en_sum_<1>	1
		sc_bit_0	ON_sum	1
CH1	**DataIn_Enable <8>**	sc_bit_7	c2<7>	1
		sc_bit_6	c2<6>	1
		sc_bit_5	c2<5>	1
		sc_bit_4	c2<4>	1
		sc_bit_3	c2<3>	0
		sc_bit_2	c2<2>	0
		sc_bit_1	c2<1>	0
		sc_bit_0	c2<0>	0
	DataIn_Enable <9>	sc_bit_7	dacb_VDC_hg<5>	0
		sc_bit_6	dacb_VDC_hg<4>	1
		sc_bit_5	dacb_VDC_hg<3>	1
		sc_bit_4	dacb_VDC_hg<2>	1

		sc_bit_3	dacb_VDC_hg<1>	0
		sc_bit_2	dacb_VDC_hg<0>	0
		sc_bit_1	ON_ch	1
		sc_bit_0	C2<8>	1
	DataIn_Enable <10>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	en_probe_outp_lg_s1	0
		sc_bit_4	en_probe_outn_lg_s1	0
		sc_bit_3	en_probe_outp_hg_s1	0
		sc_bit_2	en_probe_outn_hg_s1	0
		sc_bit_1	en_probe_g20	0
		sc_bit_0	en_probe_pa	0
	DataIn_Enable <11>	sc_bit_7	dacb_VDC_lg<5>	0
		sc_bit_6	dacb_VDC_lg<4>	1
		sc_bit_5	dacb_VDC_lg<3>	0
		sc_bit_4	dacb_VDC_lg<2>	1
		sc_bit_3	dacb_VDC_lg<1>	1
		sc_bit_2	dacb_VDC_lg<0>	0
		sc_bit_1	NC	0
		sc_bit_0	NC	0
CH2	**DataIn_Enable <12>**	sc_bit_7	c2<7>	1
		sc_bit_6	c2<6>	1
		sc_bit_5	c2<5>	1
		sc_bit_4	c2<4>	1
		sc_bit_3	c2<3>	0
		sc_bit_2	c2<2>	0
		sc_bit_1	c2<1>	0
		sc_bit_0	c2<0>	0
	DataIn_Enable <13>	sc_bit_7	dacb_VDC_hg<5>	0
		sc_bit_6	dacb_VDC_hg<4>	1
		sc_bit_5	dacb_VDC_hg<3>	1
		sc_bit_4	dacb_VDC_hg<2>	1
		sc_bit_3	dacb_VDC_hg<1>	0
		sc_bit_2	dacb_VDC_hg<0>	0
		sc_bit_1	ON_ch	1
		sc_bit_0	C2<8>	1
	DataIn_Enable <14>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	en_probe_outp_lg_s1	0
		sc_bit_4	en_probe_outn_lg_s1	0
		sc_bit_3	en_probe_outp_hg_s1	0

		sc_bit_2	en_probe_outn_hg_s1	0
		sc_bit_1	en_probe_g20	0
		sc_bit_0	en_probe_pa	0
	DataIn_Enable <15>	sc_bit_7	dacb_VDC_lg<5>	0
		sc_bit_6	dacb_VDC_lg<4>	1
		sc_bit_5	dacb_VDC_lg<3>	0
		sc_bit_4	dacb_VDC_lg<2>	1
		sc_bit_3	dacb_VDC_lg<1>	1
		sc_bit_2	dacb_VDC_lg<0>	0
		sc_bit_1	NC	0
		sc_bit_0	NC	0
CH3	**DataIn_Enable <16>**	sc_bit_7	c2<7>	1
		sc_bit_6	c2<6>	1
		sc_bit_5	c2<5>	1
		sc_bit_4	c2<4>	1
		sc_bit_3	c2<3>	0
		sc_bit_2	c2<2>	0
		sc_bit_1	c2<1>	0
		sc_bit_0	c2<0>	0
	DataIn_Enable <17>	sc_bit_7	dacb_VDC_hg<5>	0
		sc_bit_6	dacb_VDC_hg<4>	1
		sc_bit_5	dacb_VDC_hg<3>	1
		sc_bit_4	dacb_VDC_hg<2>	1
		sc_bit_3	dacb_VDC_hg<1>	0
		sc_bit_2	dacb_VDC_hg<0>	0
		sc_bit_1	ON_ch	1
		sc_bit_0	C2<8>	1
	DataIn_Enable <18>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	en_probe_outp_lg_s1	0
		sc_bit_4	en_probe_outn_lg_s1	0
		sc_bit_3	en_probe_outp_hg_s1	0
		sc_bit_2	en_probe_outn_hg_s1	0
		sc_bit_1	en_probe_g20	0
		sc_bit_0	en_probe_pa	0
	DataIn_Enable <19>	sc_bit_7	dacb_VDC_lg<5>	0
		sc_bit_6	dacb_VDC_lg<4>	1
		sc_bit_5	dacb_VDC_lg<3>	0
		sc_bit_4	dacb_VDC_lg<2>	1
		sc_bit_3	dacb_VDC_lg<1>	1
		sc_bit_2	dacb_VDC_lg<0>	0

		sc_bit_1	NC	0
		sc_bit_0	NC	0
CH4	**DataIn_Enable <20>**	sc_bit_7	c2<7>	1
		sc_bit_6	c2<6>	1
		sc_bit_5	c2<5>	1
		sc_bit_4	c2<4>	1
		sc_bit_3	c2<3>	0
		sc_bit_2	c2<2>	0
		sc_bit_1	c2<1>	0
		sc_bit_0	c2<0>	0
	DataIn_Enable <21>	sc_bit_7	dacb_VDC_hg<5>	0
		sc_bit_6	dacb_VDC_hg<4>	1
		sc_bit_5	dacb_VDC_hg<3>	1
		sc_bit_4	dacb_VDC_hg<2>	1
		sc_bit_3	dacb_VDC_hg<1>	0
		sc_bit_2	dacb_VDC_hg<0>	0
		sc_bit_1	ON_ch	1
		sc_bit_0	C2<8>	1
	DataIn_Enable <22>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	en_probe_outp_lg_s1	0
		sc_bit_4	en_probe_outn_lg_s1	0
		sc_bit_3	en_probe_outp_hg_s1	0
		sc_bit_2	en_probe_outn_hg_s1	0
		sc_bit_1	en_probe_g20	0
		sc_bit_0	en_probe_pa	0
	DataIn_Enable <23>	sc_bit_7	dacb_VDC_lg<5>	0
		sc_bit_6	dacb_VDC_lg<4>	1
		sc_bit_5	dacb_VDC_lg<3>	0
		sc_bit_4	dacb_VDC_lg<2>	1
		sc_bit_3	dacb_VDC_lg<1>	1
		sc_bit_2	dacb_VDC_lg<0>	0
		sc_bit_1	NC	0
		sc_bit_0	NC	0
CH5	**DataIn_Enable <24>**	sc_bit_7	c2<7>	1
		sc_bit_6	c2<6>	1
		sc_bit_5	c2<5>	1
		sc_bit_4	c2<4>	1
		sc_bit_3	c2<3>	0
		sc_bit_2	c2<2>	0
		sc_bit_1	c2<1>	0

		sc_bit_0	c2<0>	0
	DataIn_Enable <25>	sc_bit_7	dacb_VDC_hg<5>	0
		sc_bit_6	dacb_VDC_hg<4>	1
		sc_bit_5	dacb_VDC_hg<3>	1
		sc_bit_4	dacb_VDC_hg<2>	1
		sc_bit_3	dacb_VDC_hg<1>	0
		sc_bit_2	dacb_VDC_hg<0>	0
		sc_bit_1	ON_ch	1
		sc_bit_0	C2<8>	1
	DataIn_Enable <26>	sc_bit_7	en_probe_g20	0
		sc_bit_6	en_probe_pa	0
		sc_bit_5	dacb_VDC_sum<5>	0
		sc_bit_4	dacb_VDC_sum<4>	1
		sc_bit_3	dacb_VDC_sum<3>	1
		sc_bit_2	dacb_VDC_sum<2>	0
		sc_bit_1	dacb_VDC_sum<1>	0
		sc_bit_0	dacb_VDC_sum<0>	0
	DataIn_Enable <27>	sc_bit_7	NC	0
		sc_bit_6	NC	0
		sc_bit_5	NC	0
		sc_bit_4	en_probe_outn_hg_s1	0
		sc_bit_3	en_probe_outp_hg_s1	0
		sc_bit_2	cmd_gain_sum <2>	0
		sc_bit_1	cmd_gain_sum <1>	0
		sc_bit_0	cmd_gain_sum <0>	0

Table 7 LAUROC2 I2C bits and default values

ASIC configuration parameters used for the 25 Ohm -10 mA config and 50 Ohm – 2 mA config (measurements)

	25Ω 10 mA config DC connection between out_preamp and G20_amplifier input SC Parameters to get a peaking time of 49 ns SC parameters to set the gain SUM equal to 1	50Ω 2 mA config DC connection between out_preamp and G20_amplifier input SC Parameters to get a peaking time of 38 ns SC parameters to set the gain SUM equal to 1
sw_DC_g20	1	1
sw_ibo_g20	0	0
dac_g20<5:0> (dec code)	63	63
sw_ibi_25	1	1
sw_ibo	0	0
sw_R025_10mA	1	0
sw_R025_5mA	0	0
cr_hg_s1<2 :0> (dec code)	0	0
rc_hg_s1<3 :0> (dec code)	9	10
rc_hg_s2<3 :0> (dec code)	8	8
rc_lg_s2<3 :0> (dec code)	9	11
cr_lg_s1<2 :0> (dec code)	3	0
rc_lg_s1<3 :0> (dec code)	9	11
c2<8 :0> (dec code)	230	79
dacb_VDC_hg<5 :0> (dec code)	28	28
dacb_VDC_lg<5 :0> (dec code)	28	28
dacb_VDC_sum<5 :0> (dec code)	20	48
cmd_gain_sum <2 :0> (dec code)	0	0

Configuration (SC) parameters description

Preamp for channel <1:4>

Common SC parameters:

“1” logic level corresponds to 1.2V even for cells powered with 2.5V (1.2V to 2.5V translation made internally)

sw_ibo (SC0): The minimum current that flows in the input transistor is 3 mA. When set to 1, the current that flows in the input transistor is increased by 3 mA.

ON_Rbleed: For ch<1:4> 6 mA additional current in the input preamp (6 mA or 12 mA)

sw_ibi: ibi is the bias current of the SCG. When set to 1, the bias input current of the input transistor is 200 µA (otherwise it is 20 µA). This parameter must be set to 1 (200 µA).

ON_PA: when set to 1 all the preamps are ON. Preamps can then be set OFF using local SC parameters. This parameter is mainly for debug purpose.

sw_R025_2mA and SC_R025_10 mA:

	SW_R0_10m	SW_R0_5m	R0 equivalent	Gain (formula)	C2 (formula)	C2 (decimal) (SC bits: 9b)
50 mA	0	0	500	9	3.3 pF	107
25 mA	1	0	150//500= 115	3.6	8.3 pF	266

Tuning of the dynamic range for the 25 Ohms configuration only: depending on R0 choice, the dynamic range for the 25 Ohm PA is 5 mA or 10 mA.

ZIN: 25 ohm

When "SW_R025_5 mA" is equal to 0 and SW_R025_10mA is set to 1, R0 is equal to 150//500= 115 Ohms. The R0 choice also impacts the dynamic range. The input impedance is indeed given by : Zin = R0/(G+1) . If R0=115 Ohms G= (R0/Zin) -1 G= 115/25 = 3.6 and so C2 = 30 pF/3.6 =8.3 pF which corresponds to decimal code = 8.3 pF/0.03125 pF= 266. For Idet=10 mA, Vin=25*10mA= 250 mV, which gives Vout_pa = 3.6 * 250 mV = 900 mV

ZIN: 50 ohm

When "SW_R025_5 mA" is set to 0 and SW_R025_10mA is set to 0, R0 is equal to 500 Ohms. The gain G is then equal to 9 and C2 = 3.3 pF, which corresponds to decimal code = 3.3/0.03125= 107. For Idet =2 mA, Vin= 50 * 2 mA= 100 mV that gives Vout_pa= 9* 100 mV= 900 mV

Local SC for the preamp (SC per channel):

ON_ch<i> (SC 14, 24, 34): When set to 1, the channel is ON

c2<8:0> of each channel: tuning of the input impedance.

C2<8>	C2<7>	C2<6>	C2<5>	C2<4>	C2<3>	C2<2>	C2<1>	C2<0>
8 pF	4 pF	2 pF	1 pF	500 fF	250fF	125 fF	62.5 fF	32.25 fF

G=20 amplifier (channel<1:4>)

Common SC:

dac_g20<5:0>: DEF value = 110000. Tuning of the bias input current of the G20 amplifier used after the preamp for the HG path.

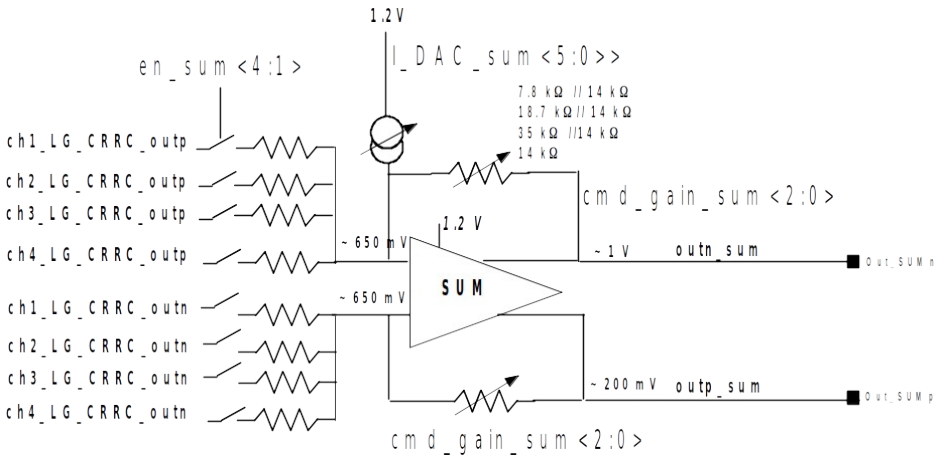
sw_DC_g20: when set to « 1 » DC connection between out_preamp and G20_amplifier input. If “0”, AC connection. Should be set to 1

ON_g20: When “1”, Gain 20 amplifier is ON.

Sw_ibo_G20: to change the output current. When set to « 0 » 3 mA, when set to « 1 » 6mA

SUM_channel

dacb_VDC_sum<5 :0> : 6-bit DAC to tune DC output level of outp_sum and outn_sum
cmd_gain_sum <2 :0> : to set the gain of the sum



Config 25 Ohms 10 mA simulations					
Max I det	2.8 mA	3.9 mA	4.5 mA	6.7 mA	10 mA
I_DAC_sum setting Dec code	44	42	38	32	24
Cmd_gain_sum_setting Dec code	7	6	5	3	0
GAIN SUM	**3.6**	**2.6**	**2.2**	**1.5**	**1**

Config 50 Ohms 2 mA simulations				
Max I det	0.6 mA	0.9 mA	1.3 mA	2 mA
I_DAC_sum setting Dec code	44	38	32	24
Cmd_gain_sum_setting Dec code	7	5	3	0
GAIN SUM	**3.3**	**2.2**	**1.5**	**1**

ON_ref_sum : when OFF (=0), the bias currents are equal to 0. DEF value= 1

en_sum_<4 :1> : to send (1) or not (0) each CRRC ouput to SUM input (« 1 »= ENABLE)

ON_sum : to set ON or OFF the SUM block (DEF value= 1= ON)

CRRC2 shaper

One LG shaper and one HG shaper, both made of two stages: Stage 1 (s1) and stage 2(s2)

Stage 1: CR + RC stage, Stage 2: RC stage

HG CRRC settings

ON_HG_s1

rc_hg_s1<3:0>

cr_hg_s1<2:0>

ON_HG_s2

rc_hg_s2<3:0>

HG C1R1			
Code	C (pF)	R (Ω)	τ (ns)
0	***20***	***500***	***10***
1	22,5	***500***	11,25
2	*25*	*500*	*12,5*
3	27,5	*500*	13,75
4	30	*500*	15
5	32,5	*500*	16,25
6	35	*500*	17,5
7	37,5	*500*	18,75

HG R1C1			
Code	C (pF)	R (Ω)	τ (ns)
0	0	3600	0,0
1	0,462	3600	1,7
2	0,924	3600	3,3
3	1,386	3600	5,0
4	1,848	3600	6,7
5	2,31	3600	8,3
6	2,772	3600	10,0
7	3,234	3600	11,6
8	3,696	3600	13,3
9	***4,158***	***3600***	***15,0***
10	4,62	3600	16,6
11	5,082	3600	18,3
12	5,544	3600	20,0
13	6,006	3600	21,6
14	6,468	3600	23,3
15	6,93	3600	24,9

HG R2C2			
Code	C (pF)	R (Ω)	τ (ns)
0	0	12000	0
1	0,14	12000	1,68
2	0,28	12000	3,36
3	0,42	12000	5,04
4	0,56	12000	6,72
5	0,7	12000	8,4
6	0,84	12000	10,08
7	0,98	12000	11,76
8	1,12	12000	13,44
9	***1,26***	***12000***	***15,12***
10	1,4	12000	16,8
11	1,54	12000	18,48
12	1,68	12000	20,16
13	1,82	12000	21,84
14	1,96	12000	23,52
15	2,1	12000	25,2

DAC_VDC_HG <i>: 6 bits DAC to tune DC output level ch by ch (around 100 -200 mV for P output, 1 – 1.1V for N output

dac_VDC_hg<5:0>_ch<1>

dac_VDC_hg<5:0>_ch<2>

dac_VDC_hg<5:0>_ch<3>

dac_VDC_hg<5:0>_ch<4>

LG CRRC settings

ON_LG_s1

cr_lg_s1<2:0>

rc_lg_s1<3:0>

ON_LG_s2

rc_lg_s2<3:0>

LG C1R1			
Code	C (pF)	R (Ω)	τ (ns)
0	10	1200	12
1	11,25	1200	13,5
2	***12,5***	***1200***	***15***
3	13,75	1200	16,5
4	15	1200	18
5	16,25	1200	19,5
6	17,5	1200	21
7	18,75	1200	22,5

LG R1C1			
Code	C (pF)	R (Ω)	τ (ns)
0	0	4000	0,0
1	0,425	4000	1,7
2	0,85	4000	3,4
3	1,275	4000	5,1
4	1,7	4000	6,8
5	2,125	4000	8,5
6	2,55	4000	10,2
7	2,975	4000	11,9
8	3,4	4000	*13,6*
9	***3,825***	***4000***	***15,3***
10	4,25	4000	17,0
11	4,675	4000	18,7
12	5,1	4000	20,4
13	5,525	4000	22,1
14	5,95	4000	23,8
15	6,375	4000	25,5

LG R2C2			
Code	C (pF)	R (Ω)	τ (ns)
0	0	12000	0
1	0,14	12000	1,68
2	0,28	12000	3,36
3	0,42	12000	5,04
4	0,56	12000	6,72
5	0,7	12000	8,4
6	0,84	12000	10,08
7	0,98	12000	11,76
8	1,12	12000	13,44
9	***1,26***	***12000***	***15,12***
10	1,4	12000	16,8
11	1,54	12000	18,48
12	1,68	12000	20,16
13	1,82	12000	21,84
14	1,96	12000	23,52
15	2,1	12000	25,2

DAC_VDC_LG <i>: 6 bits DAC to tune DC output level ch by ch (around 100 -200 mV for P output, 1 – 1.1V for N output)

dac_VDC_lg<5:0>_ch<1>

dac_VDC_lg<5:0>_ch<2>

dac_VDC_lg<5:0>_ch<3>

dac_VDC_lg<5:0>_ch<4>