FEB2 ‘Slice’ Testboard Update

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October 6th, 2021

Overview

Analog Testboard (2019)

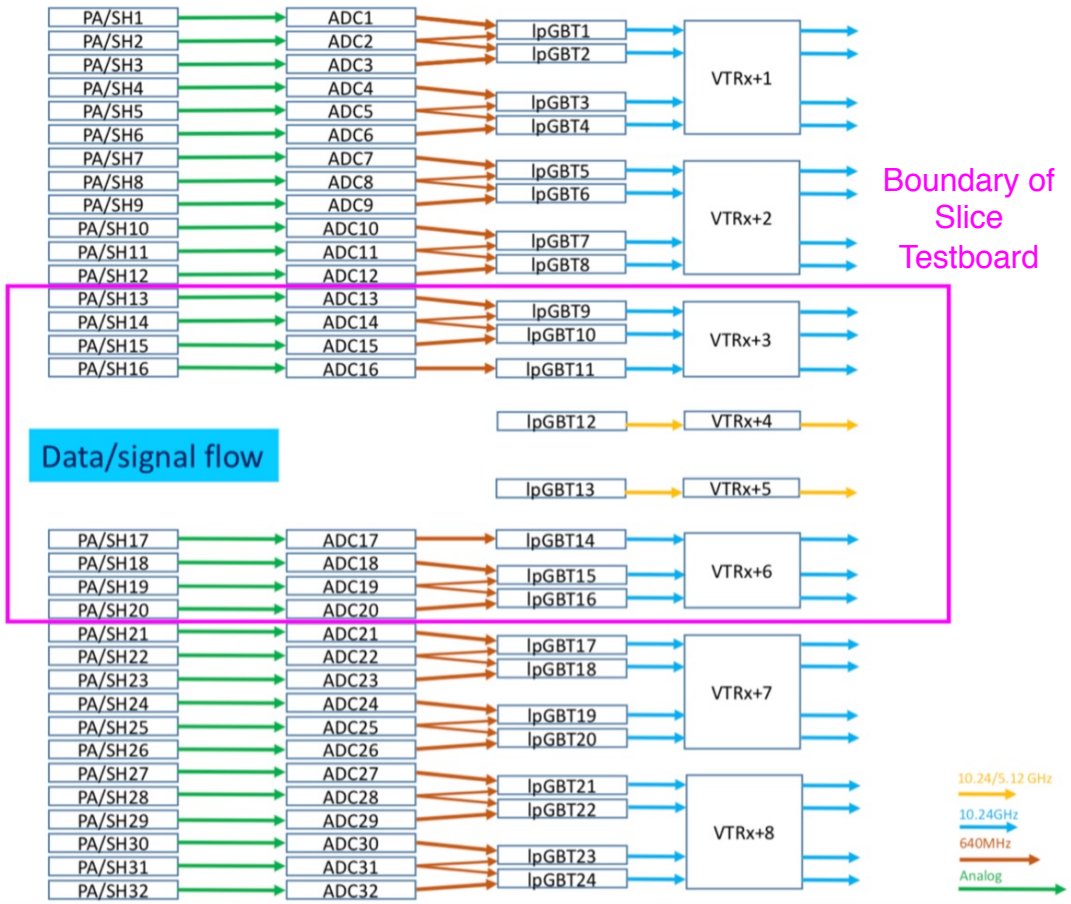
- 2 (LAUROC1 PA/S + COLUTAv2 ADC) +lpGBT
- Verified full readout chain: PA/s → ADC → optical data links

Slice Testboard (2020-2021)

- 8 (LAUROC2 PA/S + COLUTAv3 ADC +lpGBT) chips, 32 LAr channels available
- **Goal:** demonstrate multichannel performance, bi-directional control links

Full FEB2 Prototype (2022-2023)

- All 128 channels available



Timeline

Feb 15 – Began testing of 2 new fully assembled (v1.1) Slice Testboards

July 8 – Received additional LAUROC chips to allow assembly of 3 additional boards

Aug. 6 – expected to receive 3 new boards. However, had to stop assembly since PCB Assembler accidently mixed lpGBT chips together so could no longer tell which were "all good" to be used for lpGBT12/13

Sept. 8 – received new lpGBT chips (thanks Hucheng!) in exchange for the old ones, and restarted the assembly

Sept. 30 – Oct. 4 – received 3 new v1.1 Slice Testboards (bringing total to 5)

This week – send 1 v1.1 board to BNL, to replace the partially assembled v1.0 board we delivered to them at end December 2020

End October(?) – aim to be ready to distribute v1.1 Slice Testboards to other collaborators (need to discuss where)

Slice Testboard Layout + Features

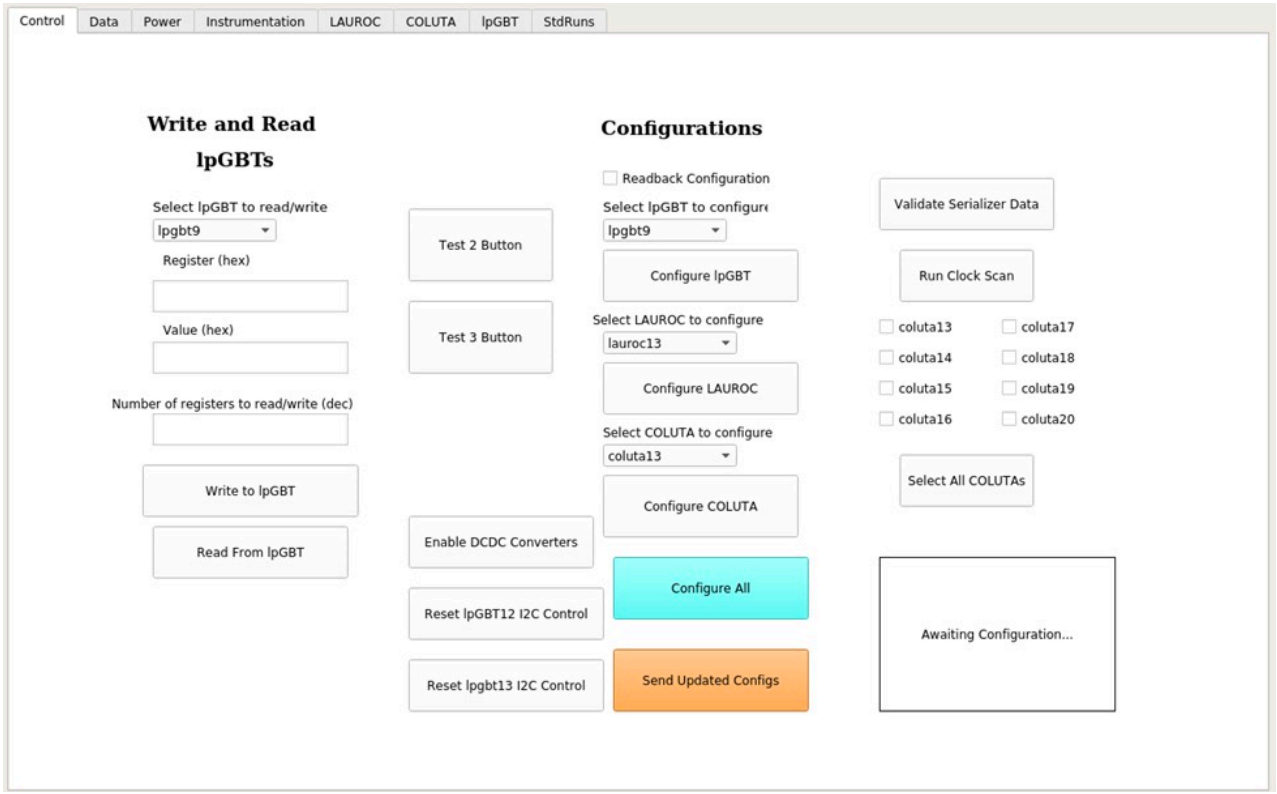
COLUTA LAUROC

- Full sized PCB, including layout and density as planned for final FEB2
  - **32** of 128 channels implemented
- Implemented and validated redundant bidirectional control links
- capable of fully programming v1.1 boards at Nevis, and confirming configuration with readbacks
  - can configure and read back all LAUROC, COLUTA, and lpGBT chips
- Pulses injected through 1500pF load injector boards (not shown), with LAUROC impedance set at 25Ohm (or 330pF boards with 50 Ohm LAUROC configuration)

GUI Developments

- Full board control + readout implemented through GUI software package integrated with FELIX
  - Board voltage and temperature monitoring available in GUI software
  - Synchronized clocks between FELIX and AWG for precise physics pulse energy + timing measurements

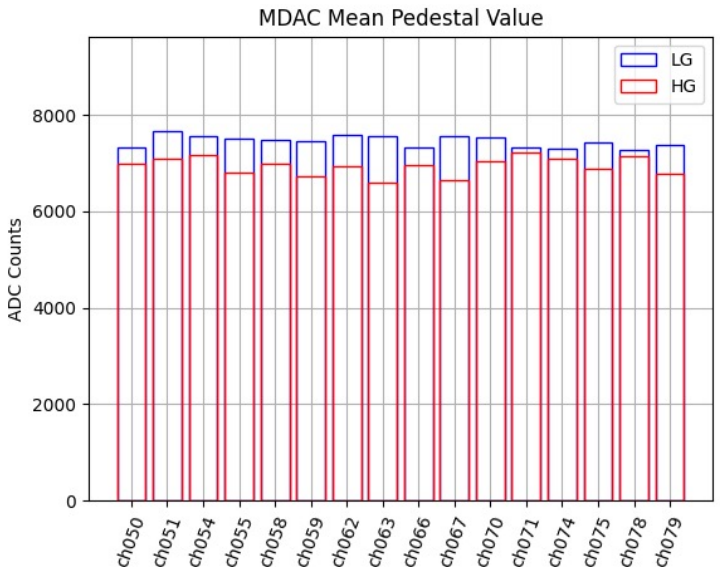
- Full ADC calibration (MDAC +SAR) available through GUI
  - Calibration done in parallel – offers speed-up relative to previous calibration method
    (**7hrs → 25 mins**)
  - Calibration constants stored in database
  - further optimization and speed-up being investigated

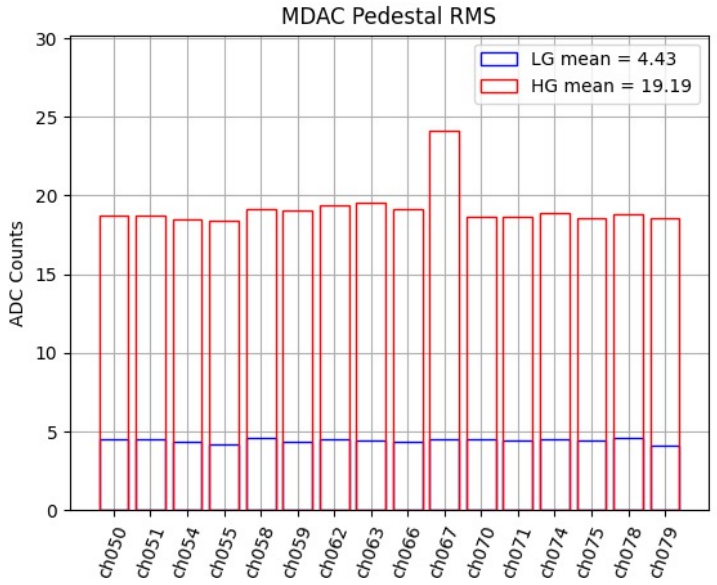


	MDAC Calibration	SAR Calibration
All channels	~4.5 minutes	N/A
Even/odd channels	~8 minutes	~18 minutes
Multi-COLUTA single ch.	~12 minutes	~32 minutes

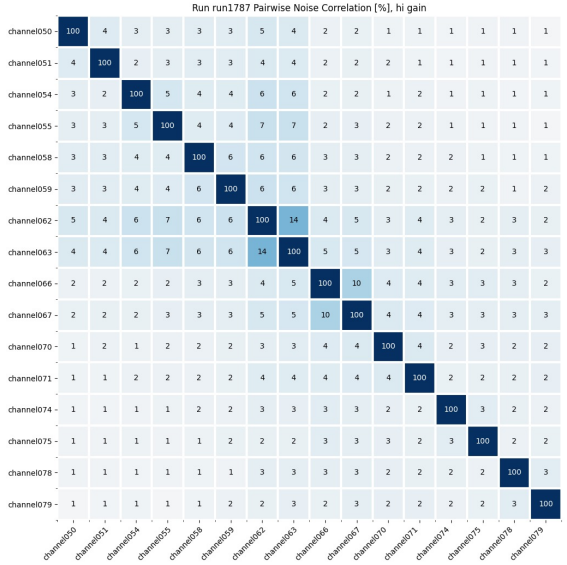
Noise Measurements (25 Ohm Setting)

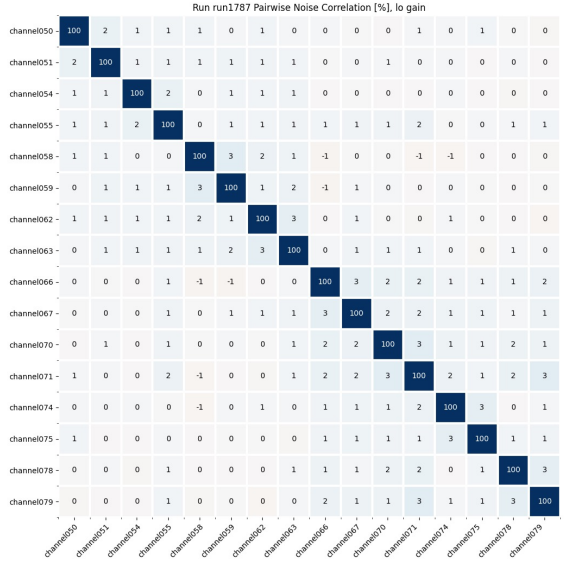
- **Pedestal Analysis**: Automated board-level summary and per-channel noise analysis
- Results shown are from **fully calibrated board**
- Adjustable pedestal levels set on each channel
  - **LG Noise:** 4.0 ADC counts; **HG Noise:** 19.2 ADC counts;
  - (**Hi/Lo Gain ratio:** 25.6)
  - Somewhat higher HG noise observed on ch67 HG (under investigation)





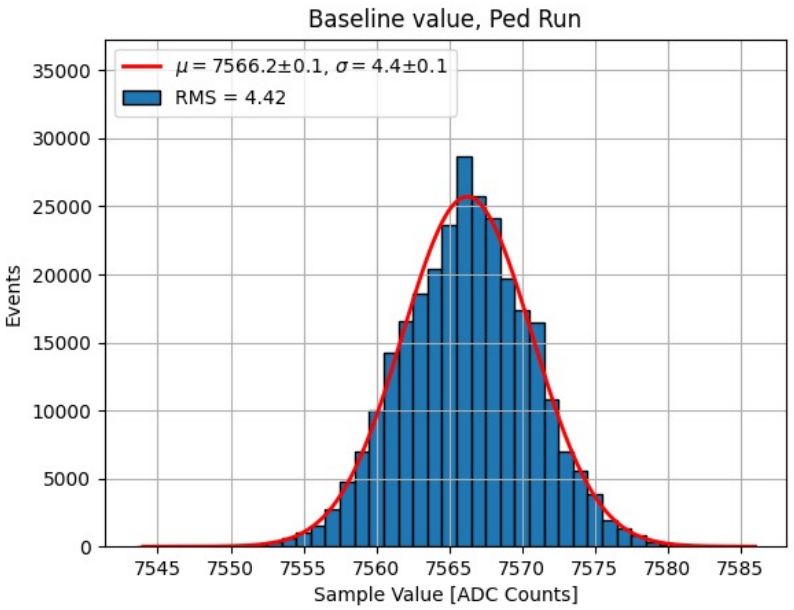
Correlated Noise

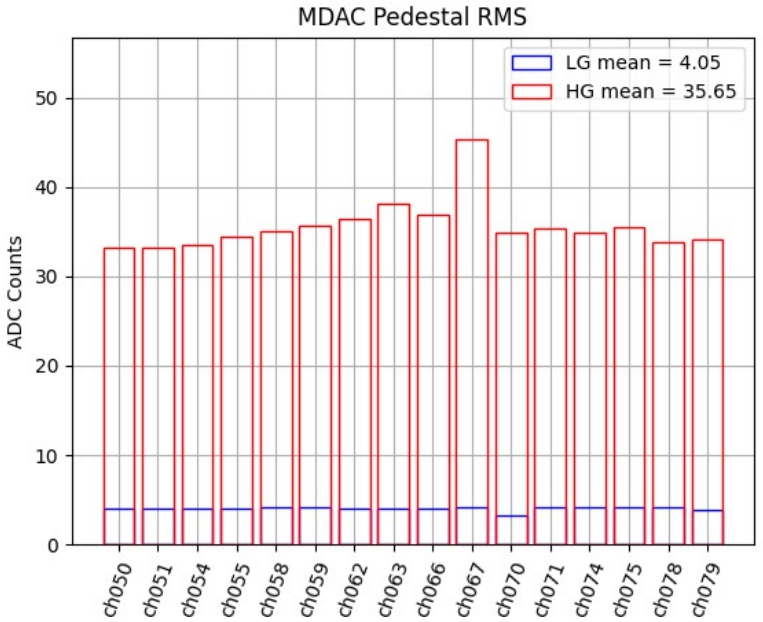




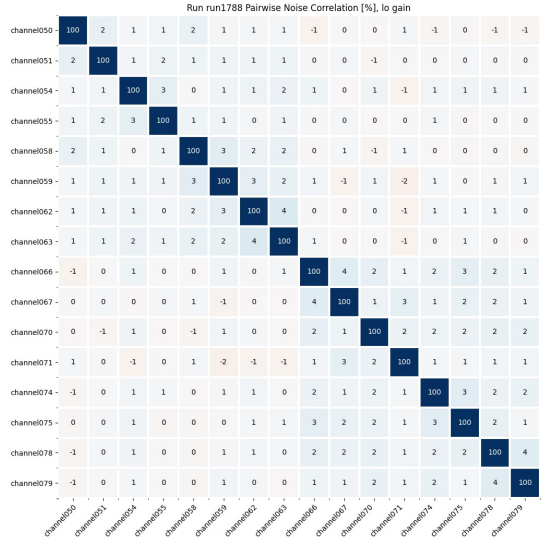
Noise Measurements (50 Ohm Setting)

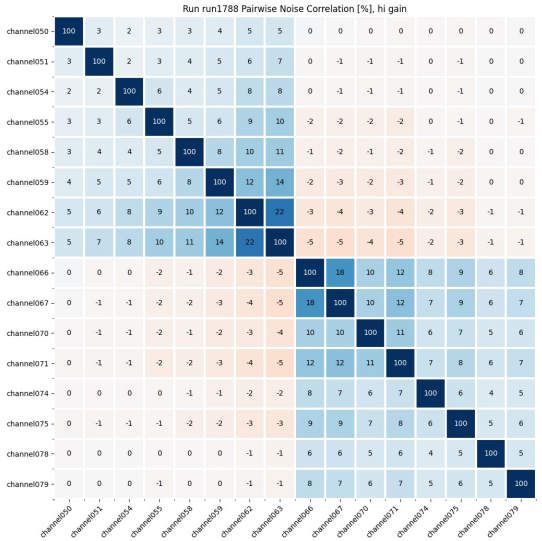
- **LG Noise:** 4.0 ADC counts; **HG Noise:** 35.65 ADC counts;
- (**Hi/Lo Gain ratio:** 37.4)
- Somewhat higher HG noise observed on ch67 HG (under investigation)
- Correlated noise towards center of the board is
  Understood: due to incomplete grounding of injector boards





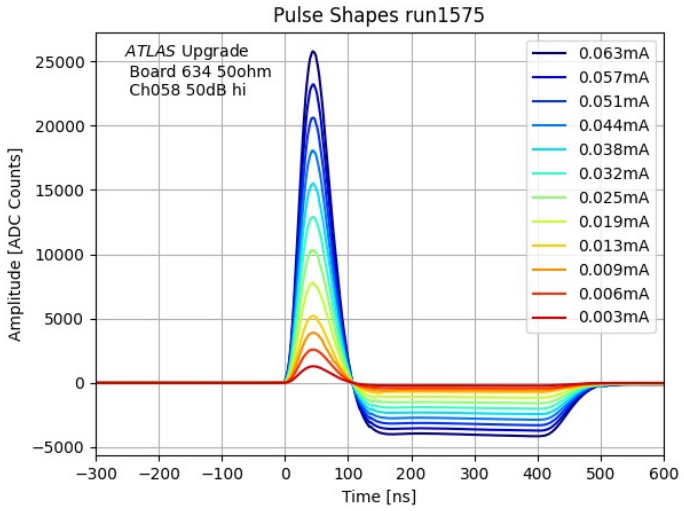
Correlated Noise

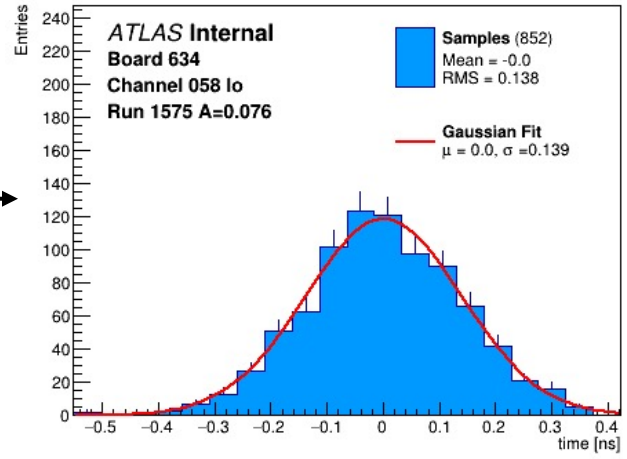


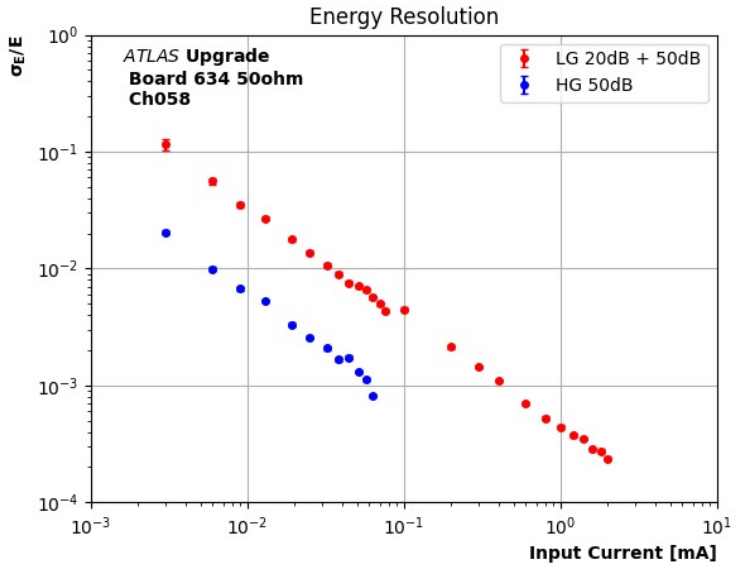


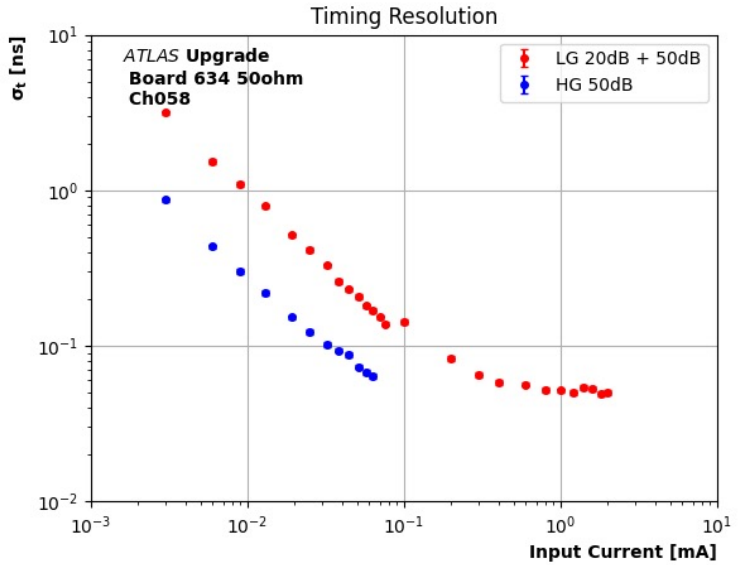
Single-Channel Performance (50 Ohm)

- ADCs derives 40 MHz CLK from FELIX, which is synchronized to AWG signal source
  - Pulse HG+LG channel at amplitudes spanning dynamic range
  - Combine different attenuations at input to access full range
  - Apply OFCs to repeated measurements, perform gaussian fit on results to obtain Energy, timing resolution
  - Energy resolution ~.02% for large pulses
  - Timing resolution ~ 50 ps (dominated by system CLK jitter, not by Slice Testboard)

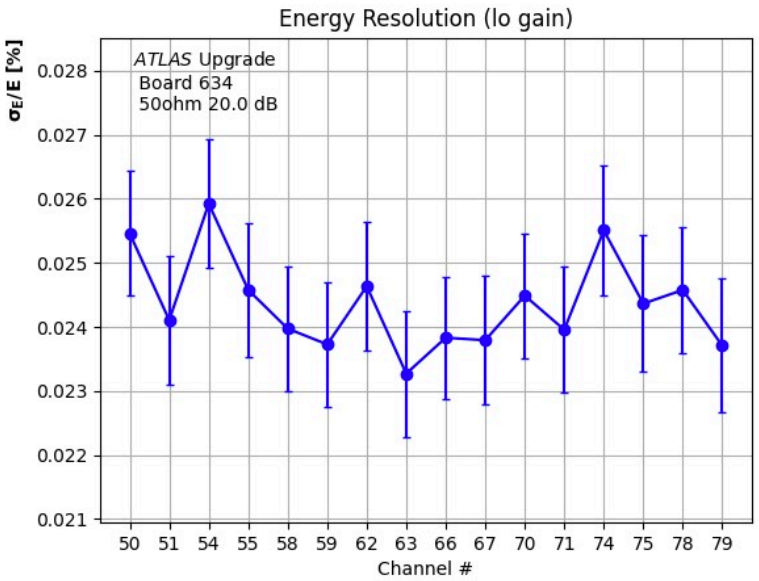


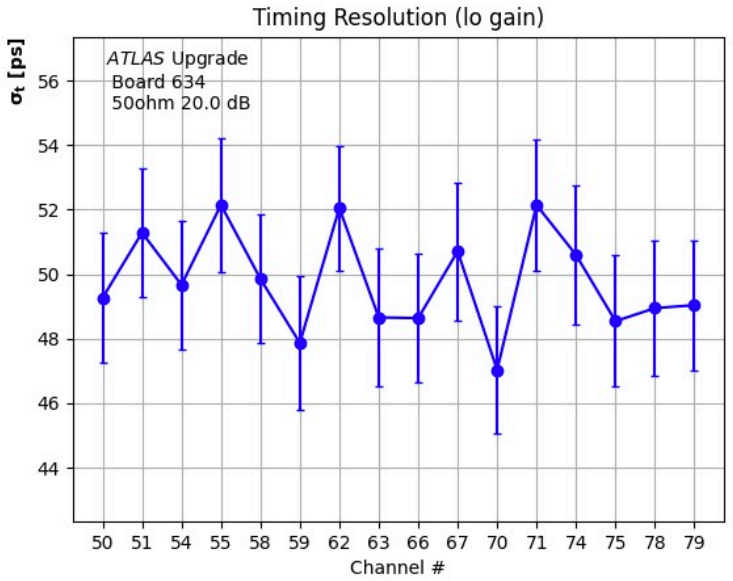


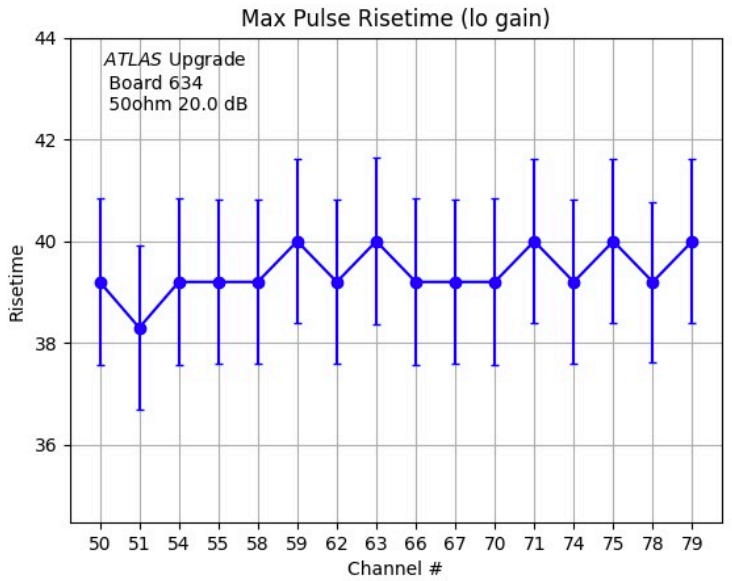




Multi-channel Performance (50 Ohm Setting)



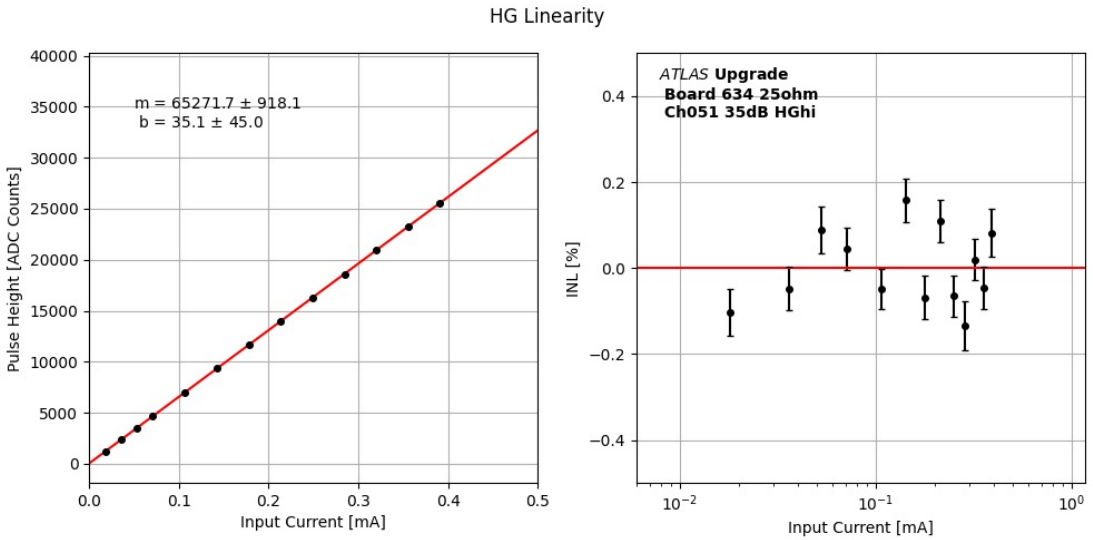


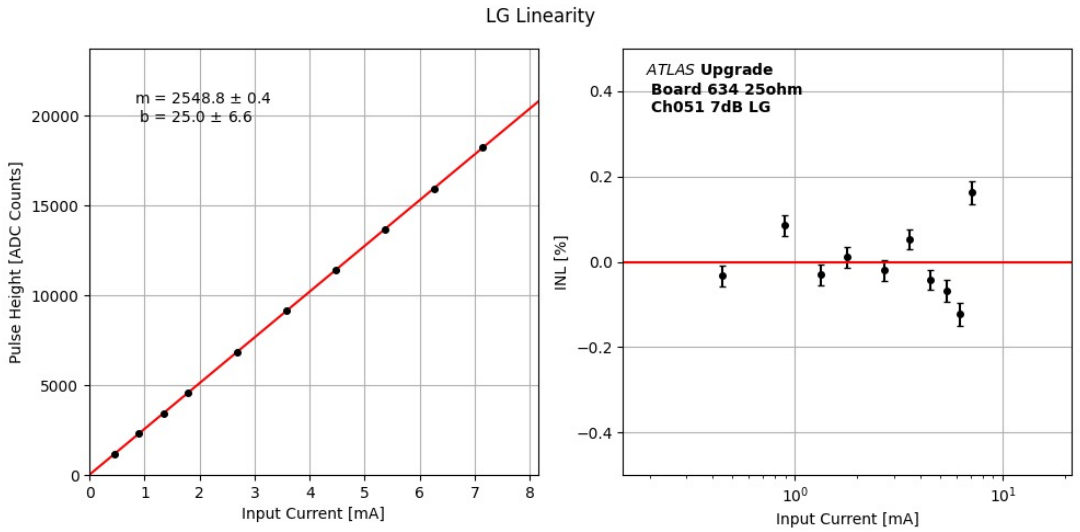


- Automated **Full-board characterization** software package in development
- Energy resolution, timing resolution, and pulse risetime for large pulse heights consistent across channels on PCB #634

Linearity (25 Ohm Setting)

- **Hi/Lo gain ratio: 25.6**



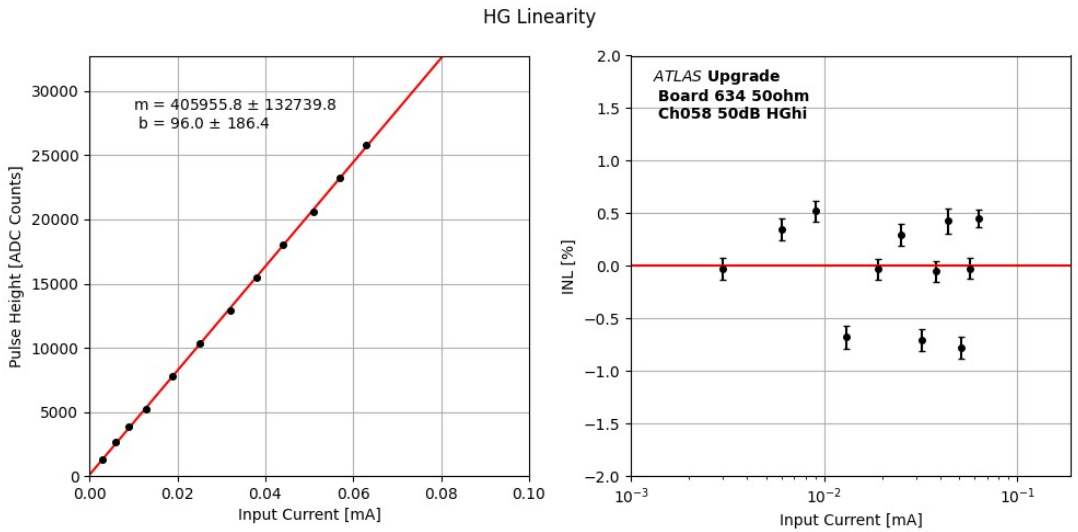


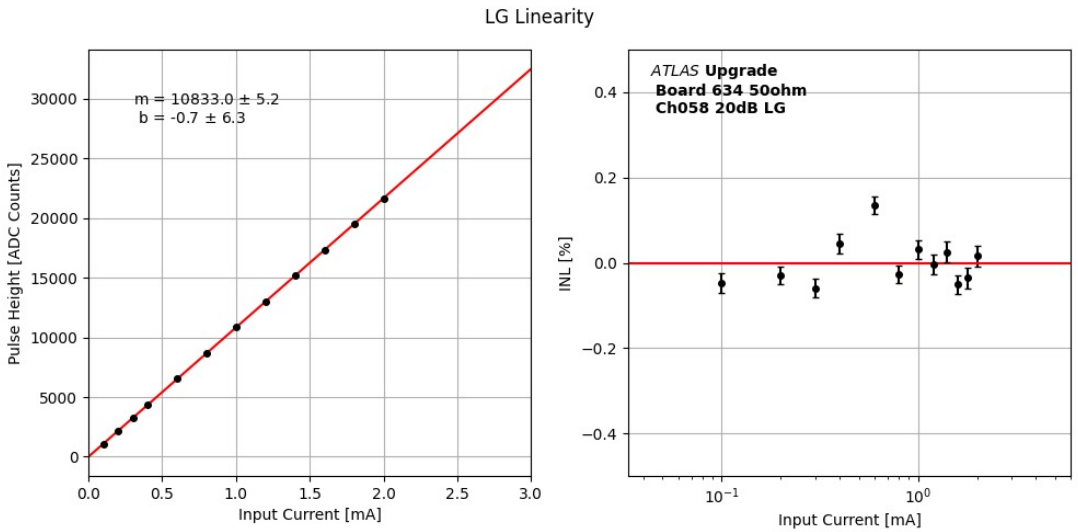
Setting	Gain	Ch	Gain [ADC/mA]	Noise [ADC]	Gain [mV/mA]	ENI [nA]	risetime [ns]
25 Ohm	HG	51	65300	18.7	3985.6	286.4	48.3
25 Ohm	LG	51	2549	4.5	155.6	1765.4	49.2

- LG INL < .2%, HG INL < .2 %
- Compare with results from LAUROC PDR :
  HG ENI 265nA, 46ns risetime, HG/LG ratio ~24

Linearity (50 Ohm Setting)

- **Hi/Lo gain ratio: 37.4**

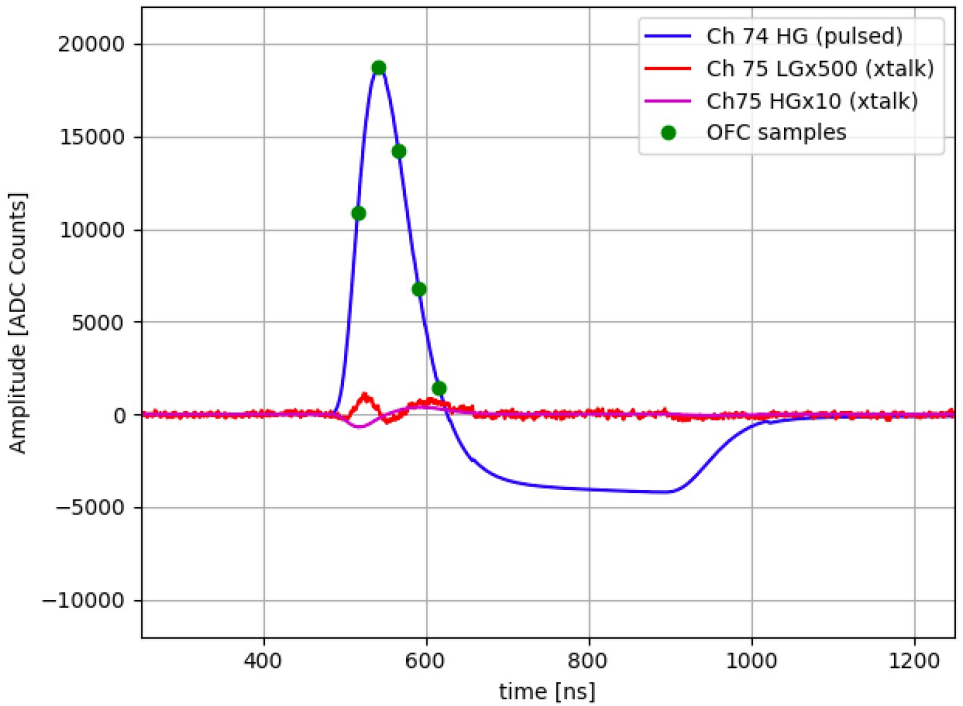


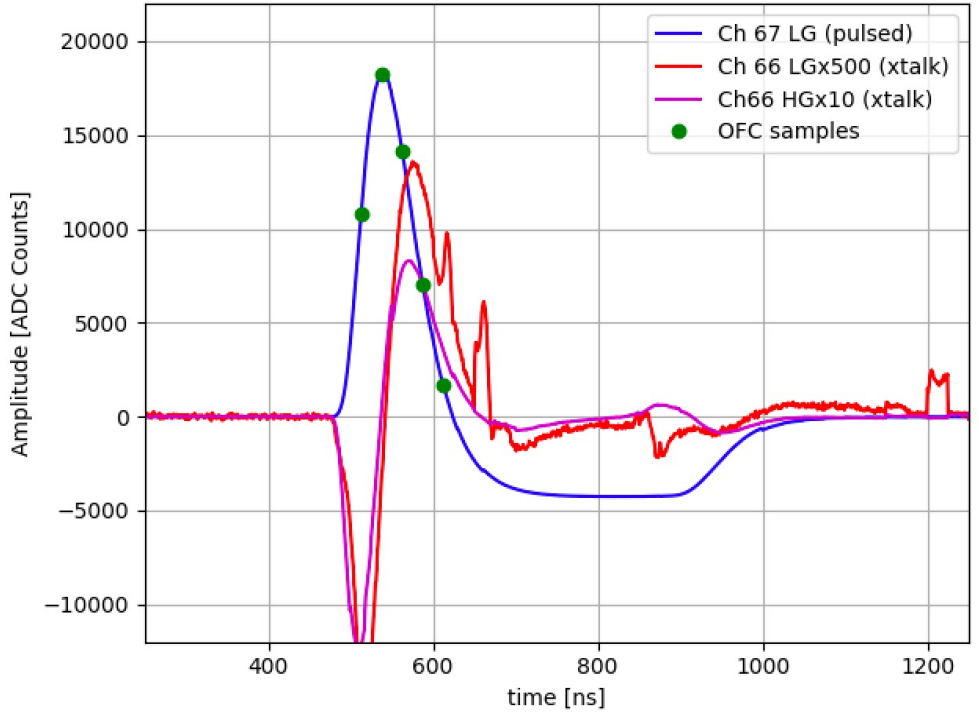


Setting	Gain	Ch	Gain [ADC/mA]	Noise [ADC]	Gain [mV/mA]	ENI [nA]	risetime [ns]
50 Ohm	HG	58	406000	35.1	24780.3	86.5	39.4
50 Ohm	LG	58	10833	4.3	661.2	396.9	39.7

- LG INL < .2%, HG INL < 1.0 % (currently investigating)
- Compare with results from LAUROC PDR :
  HG ENI 78nA, 38ns risetime, HG/LG ratio ~35

Crosstalk Studies (25 Ohm)





Pulsed Channel	OFC Pulse Height [ADC]	PP LG xtalk [%]	OFC LG xtalk [%]	PP HG xtalk [%]	OFC HG xtalk [%]
ch 74 HG 25 Ohm	18728	0.41	0.14	0.58	0.07
ch 67 LG 25 Ohm	18247	0.33	0.01	0.44	0.02

- Send near-saturating pulse to single channel, measure HG+LG response on neighbor
- Use HG/LG ratio from linear fits to convert between gain scales for xtalk calculation
- Applying OFCs suppresses measured crosstalk by ~order of magnitude (xtalk is mostly capacitive)

Conclusions

- Testing on v1.1 of Slice Testboard is well underway

  - ✓ We have demonstrated fully functional data readout on all 32 channels
  - ✓ We have demonstrated use of the redundant control feature between lpGBT12 & lpGBT13
  - ✓ We have implemented parallel ADC calibration method, which offers 16x speedup from previous calibration setup

- Pulse injection analysis is proceeding

  - ✓ Pulse data has been taken and validated on all channels of board 64
  - ✓ Pulse data analysis is fully automated
  - Measurements show relatively good agreement with those from LAUROC PDR

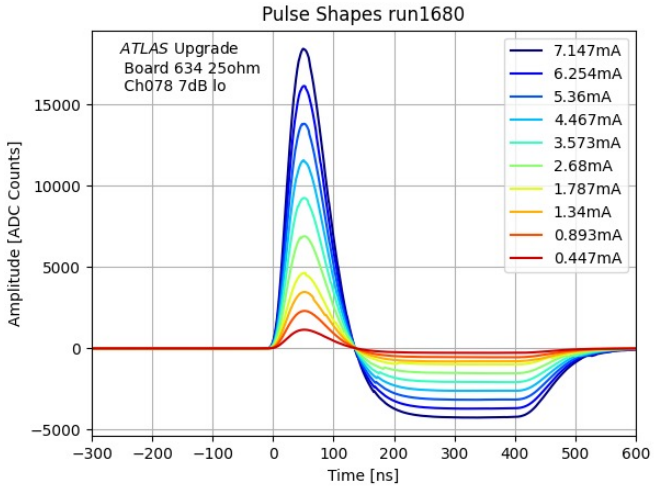
- **An additional 3 boards have arrived at Nevis last week, testing is currently underway**

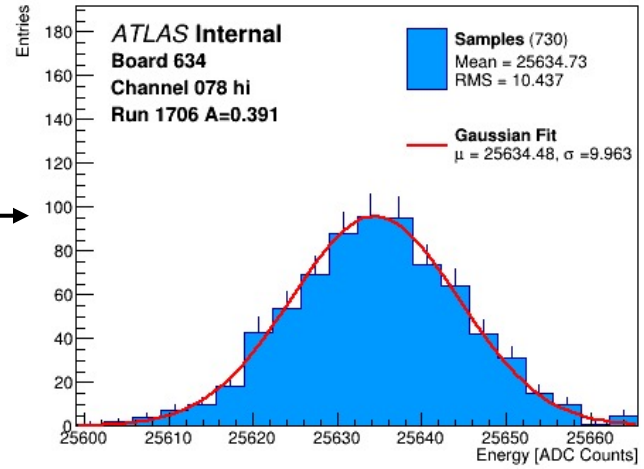
  - **This week –** send 1 v1.1 board to BNL, to replace the partially assembled v1.0 board we delivered to them at end December 2020
  - **End October(?) –** aim to be ready to distribute v1.1 Slice Testboards to other collaborators (need to discuss where)

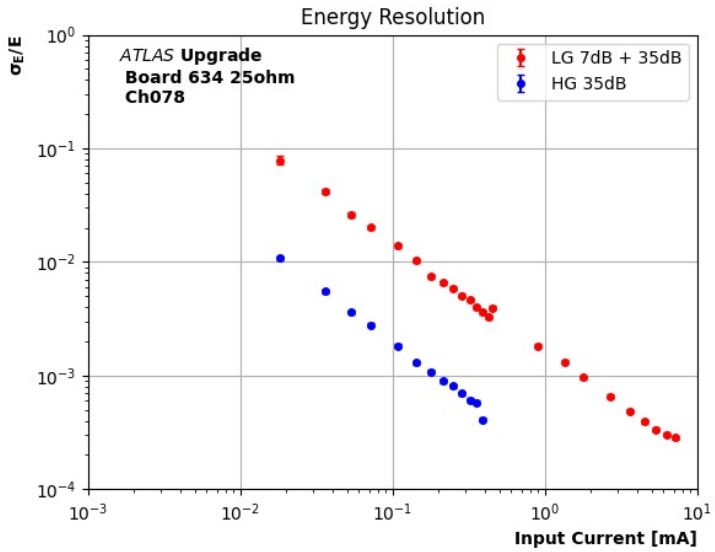
BACKUP

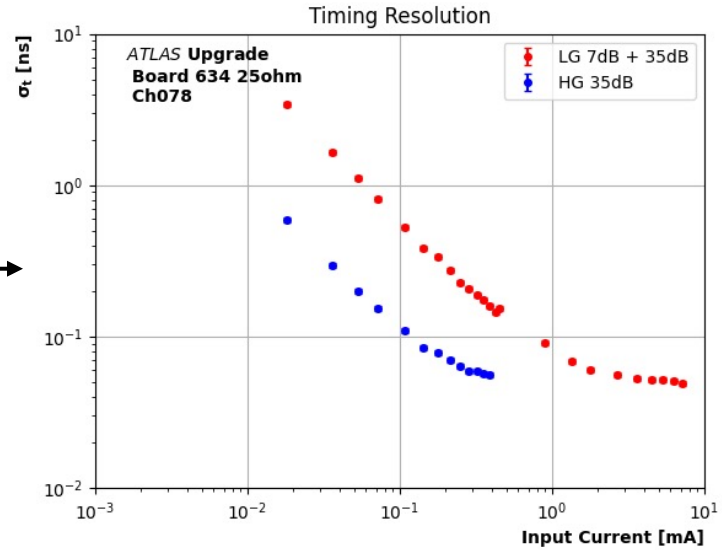
Single-channel Performance (25 Ohm)

- FELIX Clock Synchronized to AWG
  - Pulse HG+LG channel at amplitudes spanning dynamic range
  - Apply OFCs to repeated measurements, perform gaussian fit on results to obtain Energy, timing resolution
  - Energy tesolution ~.02% for large pulses
  - Timing resolution ~ 50 ps (dominated by clock jitter)

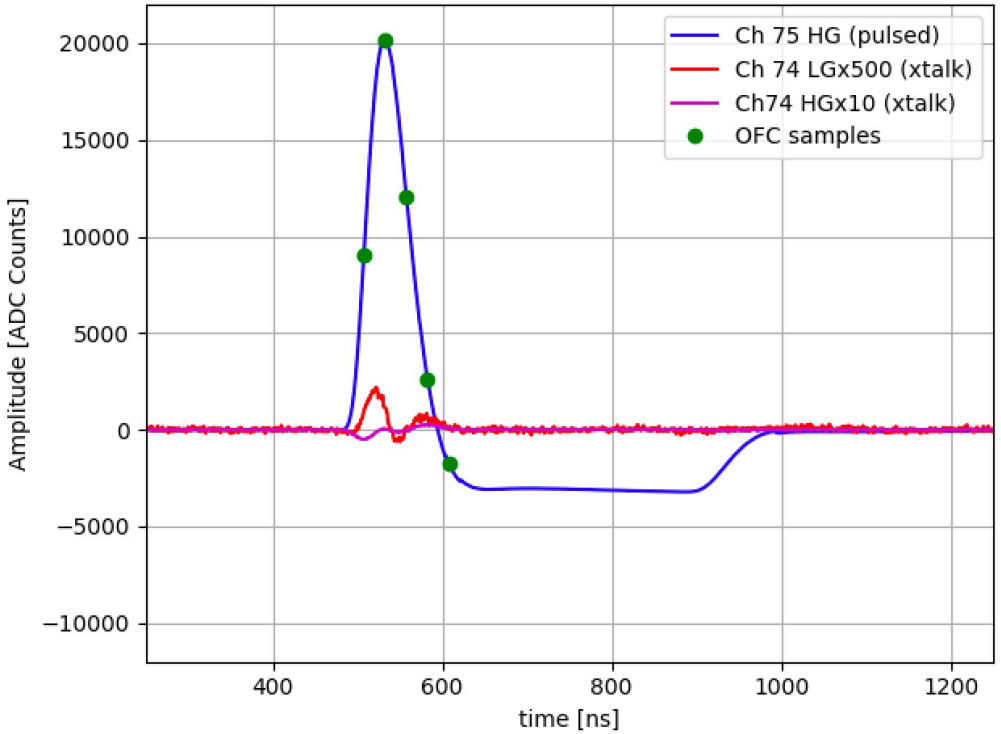


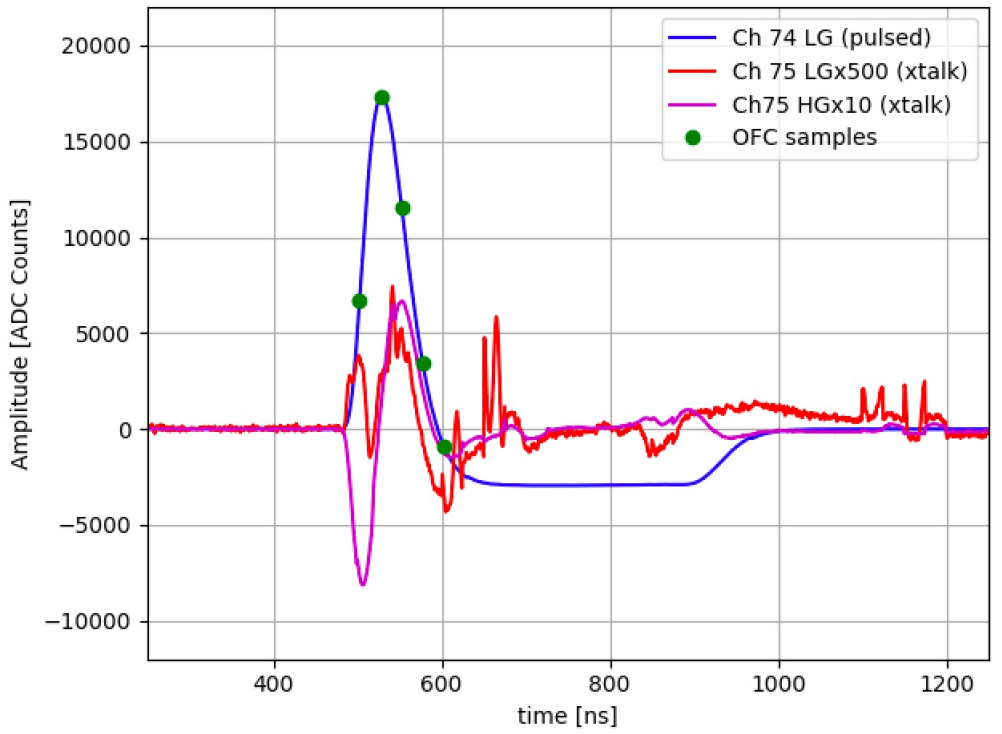






Crosstalk Studies (50 Ohm)



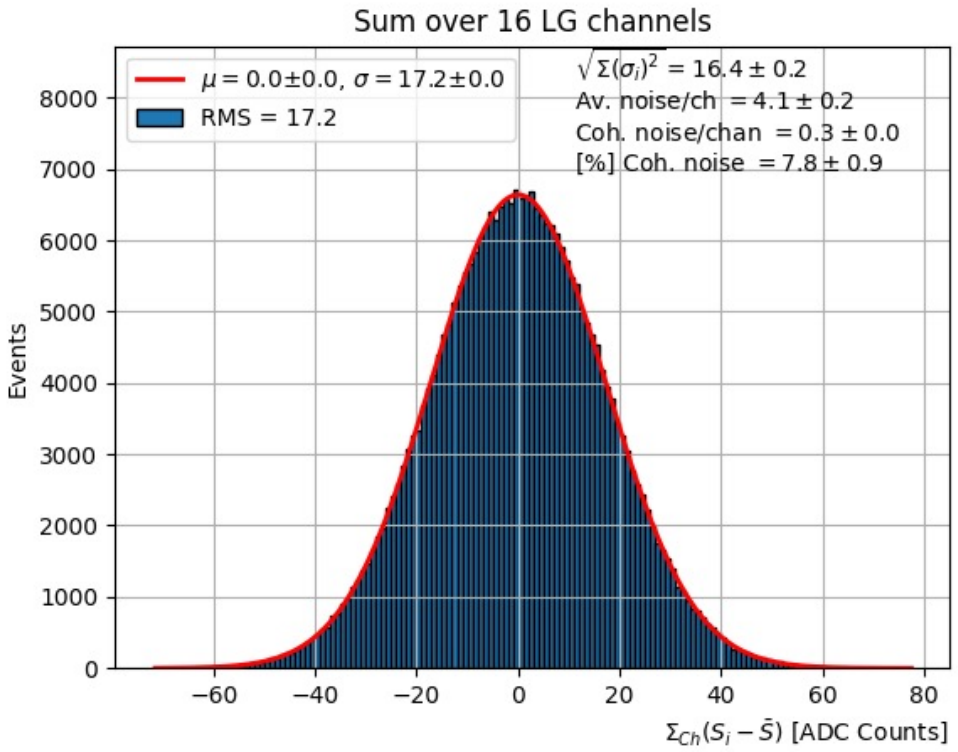


Pulsed Channel	OFC Pulse Height [ADC]	PP LG xtalk [%]	OFC LG xtalk [%]	PP HG xtalk [%]	OFC HG xtalk [%]
ch 75 HG 50 Ohm	20200	0.56	0.19	0.38	0.04
ch 74 LG 50 Ohm	17342	0.14	0.05	0.23	0.03

- Send near-saturating pulse to single channel, measure HG+LG response on neighbor
- Use HG/LG ratio from linear fits to convert between gain scales for xtalk calculation

Coherent noise histograms (Pedestal analysis)

50 Ohm Setting



25 Ohm Setting