Status of FEB2 Architecture and Design of "Slice Testboard"

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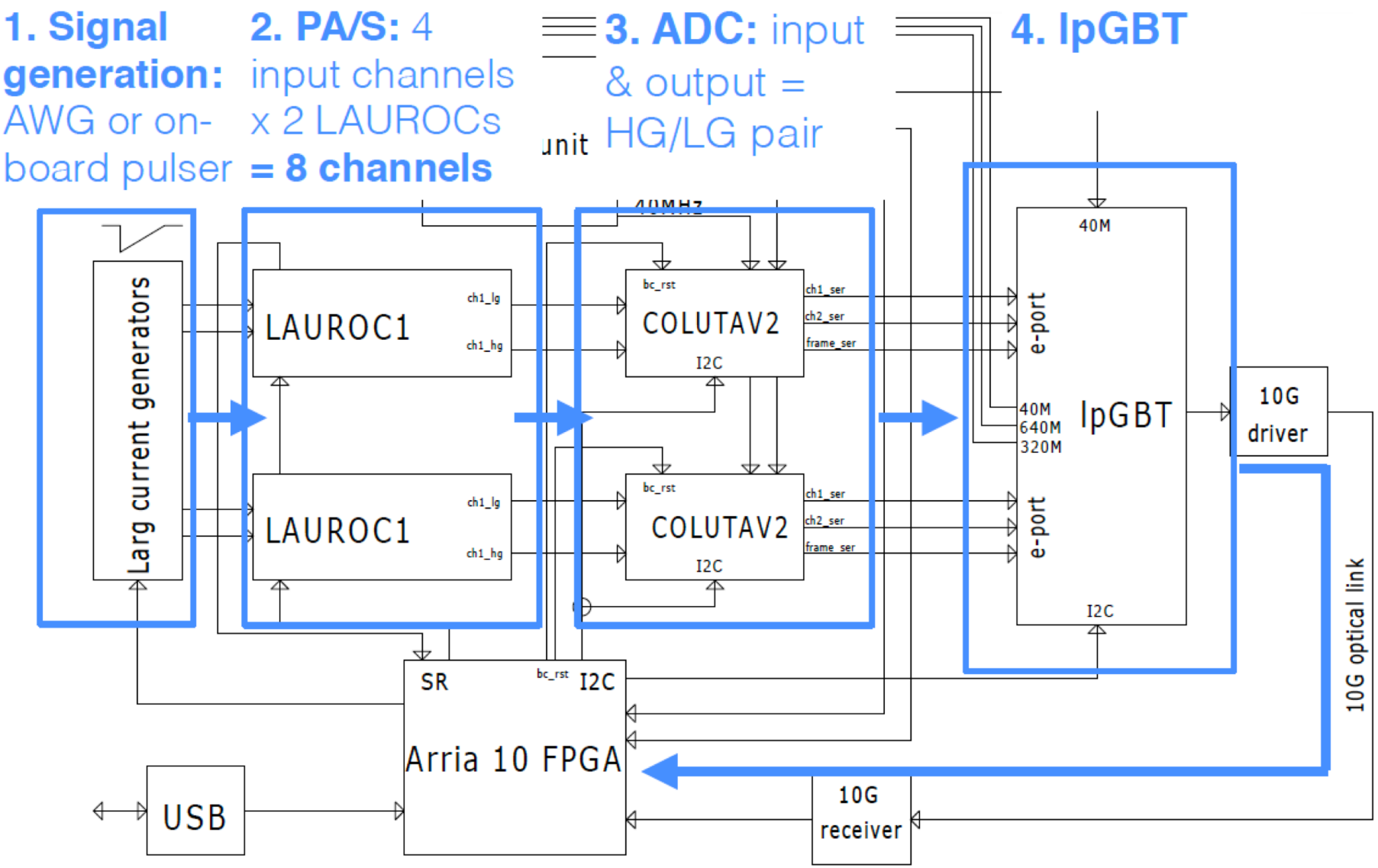
Introduction

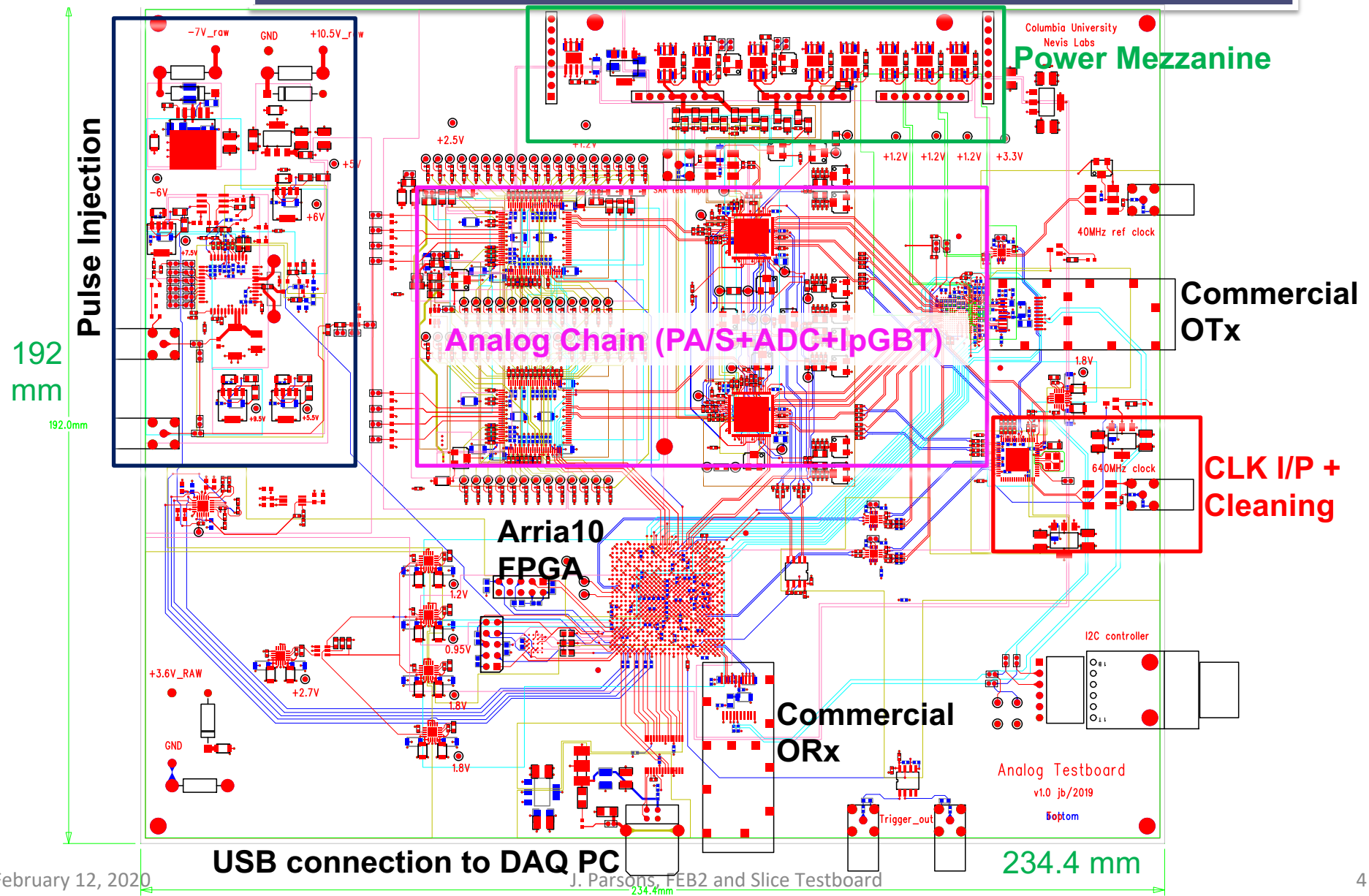
- Recall that (as described in TDR) FEB2 development has been planned as a sequence of steps of increasing complexity, integrating at each step the latest iterations of the various custom ASICs

1. Analog Testboard (2019)
   - Integrates 2 LAUROC1 PA/S chips, 2 COLUTAv2 ADC chips, 1 lpGBT chip
   - Limited to reading out 2 LAr channels (cf. 128 on FEB2)
   - Used to demonstrate full readout chain of PA/S + ADC + optical data links
2. "Slice Testboard" (2020)
   - Integrates up to 8 (LAUROC2/ALFE1B PA/S + COLUTAv3 ADC + lpGBT) chips
   - Capable of reading out up to 32 LAr channels (cf. 128 on FEB2)
   - Use to demonstrate multichannel performance, Control links, radtol power, …
3. FEB2 Prototype (2021-2022)
   - Full 128-channel prototype
   - Use to validate performance before launching FEB2 (pre)production (2023-2024)

Analog Testboard Block Diagram

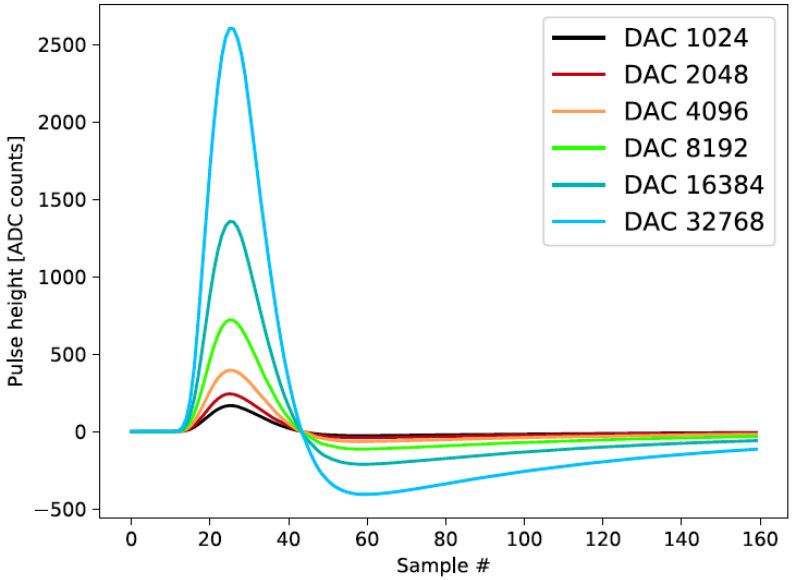


Analog Testboard Layout

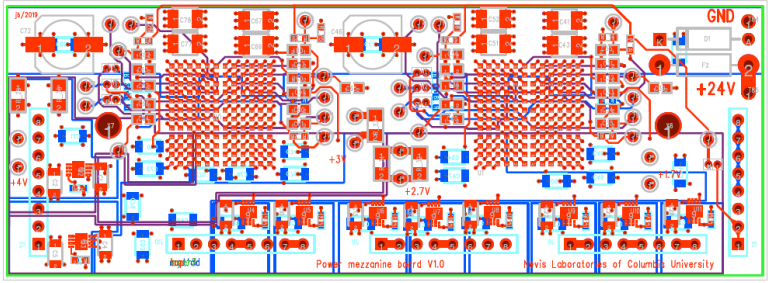


Analog Testboard Summary

- Full readout chain works!
- Promising performance measurements, such as presented in
  - September 2019 LAr week
  - Phase II Upgrade Mtg in October 2019
  - November 2019 ATLAS Upgrade week
  - November 2019 LAr week



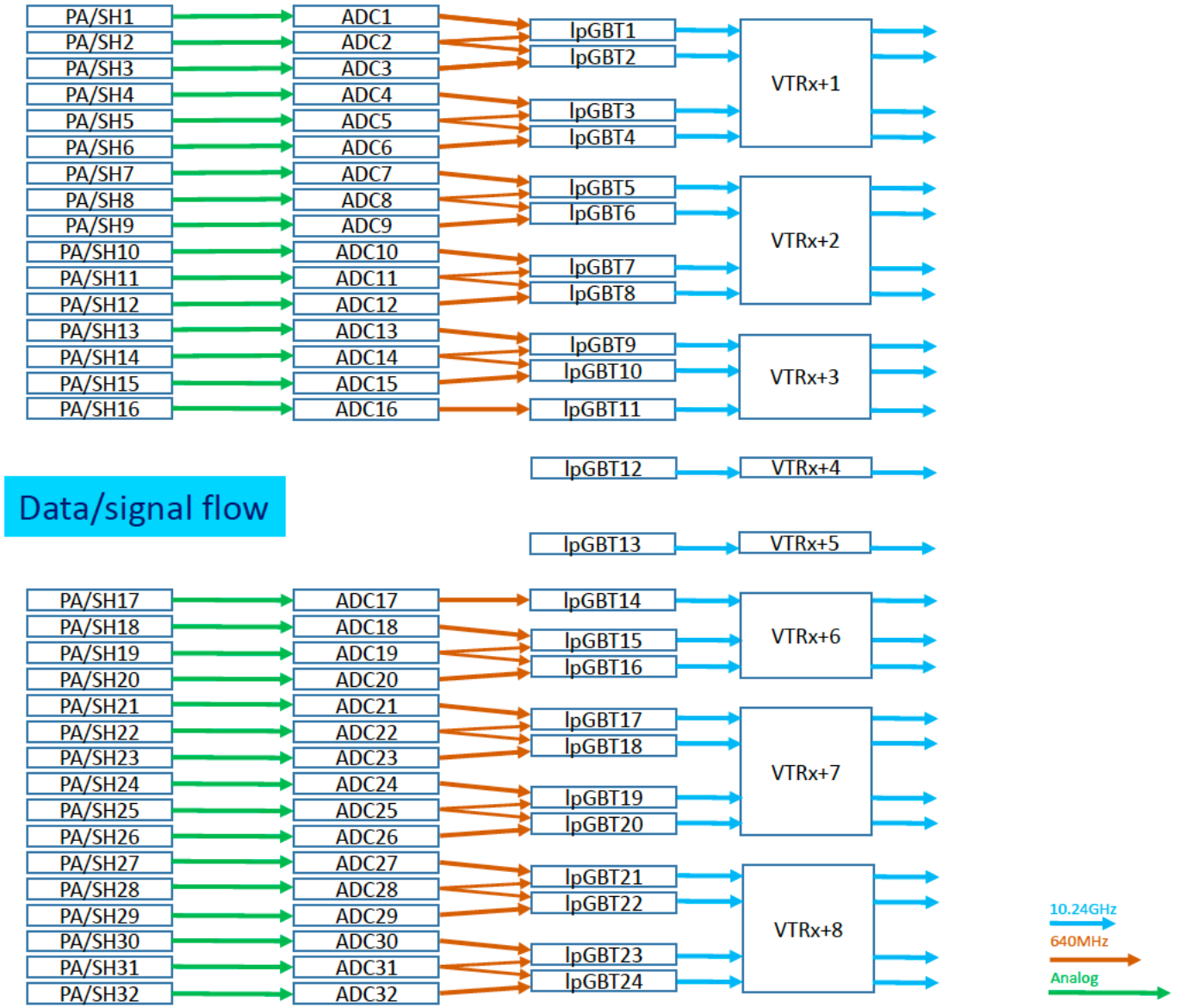
- Columbia delivered boards to BNL, UT Austin in US, + Orsay, Saclay in France
  - Tests ongoing in multiple labs to fully characterize performance
  - BNL has made good progress integrating Analog Testboard readout to FELIX
- Using PWR mezzanine, recently implemented candidate rad-tol pwr scheme
  - No observable increase in coherent noise
  - Mezzanine has been provided to INFN for more detailed characterization



FEB2 Architecture Development

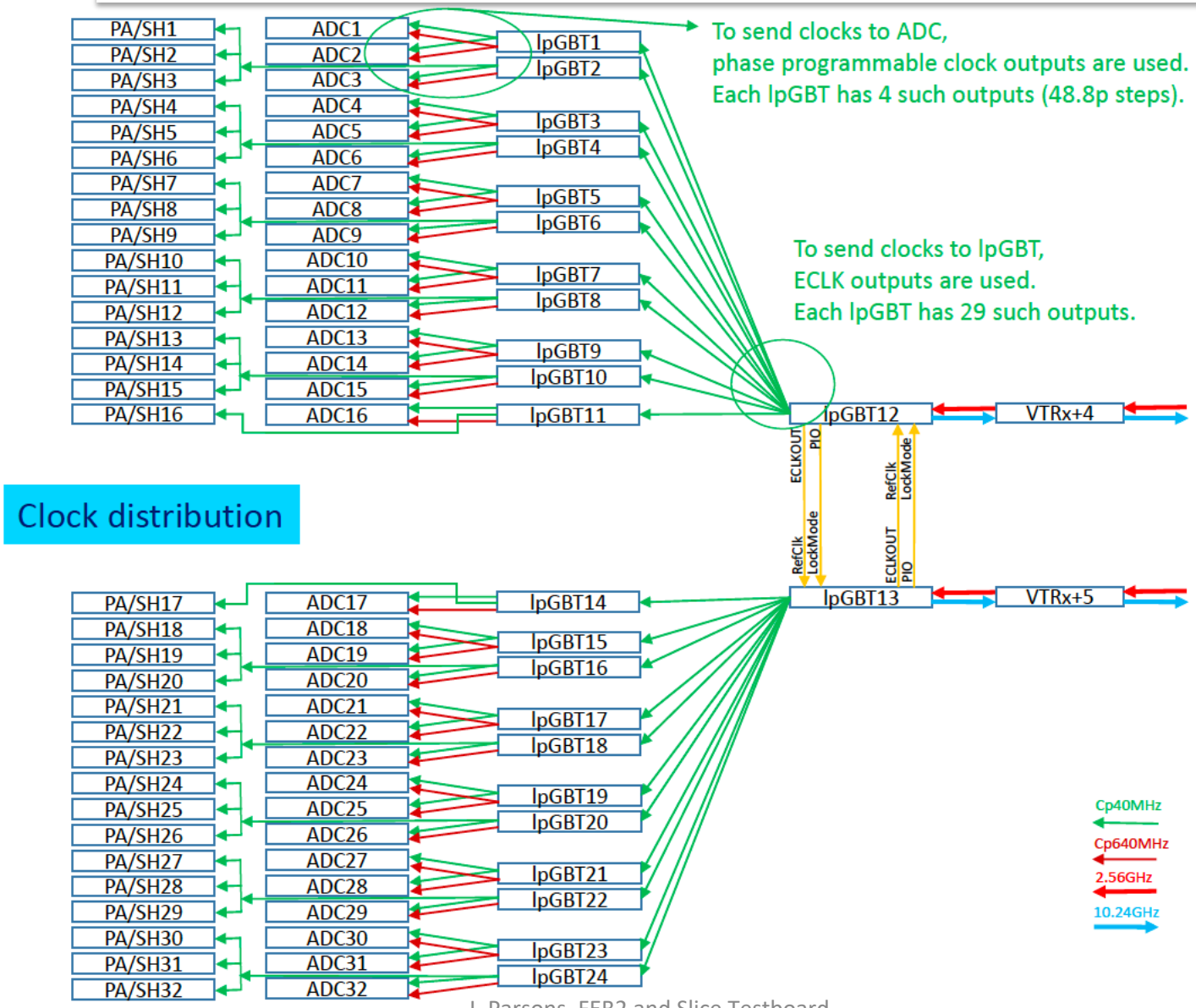
- Building on the success of the Analog Testboard, we are now focused on design of Slice Testboard as the next step, the challenges for which include
  - Integrating next versions of PA/S (including I2C control, L1 trigger sums) and ADC (including full 8-channel/chip density and on-chip Vrefs)
  - Scaling up to 32-channel readout, instead of just 2 channels
  - Implementing redundant bi-directional control/monitoring links using lpGBTs (guided by the recommendations from the work of the SMU group)
  - Implementing VTRx+ for data and control links
  - Implementing rad-tol power scheme
- To have the Slice Testboard represent, as closely as possible, a "slice" of the final FEB2, it is necessary to progress in parallel on the FEB2 architecture
  - We have developed a number of FEB2 block diagrams, presented in the following, that provide details of various aspects of the FEB2 functionality
  - In addition to informing the Slice Testboard design, these block diagrams can guide the needed discussions of other system interfaces (to LATS, LASP, LVPS, …)
  - Would like to finalize these discussions with the goal to hold the ATLAS Specifications Review for the FEB2 by around the time of the April AUW

FEB2 Data/Signal Flow

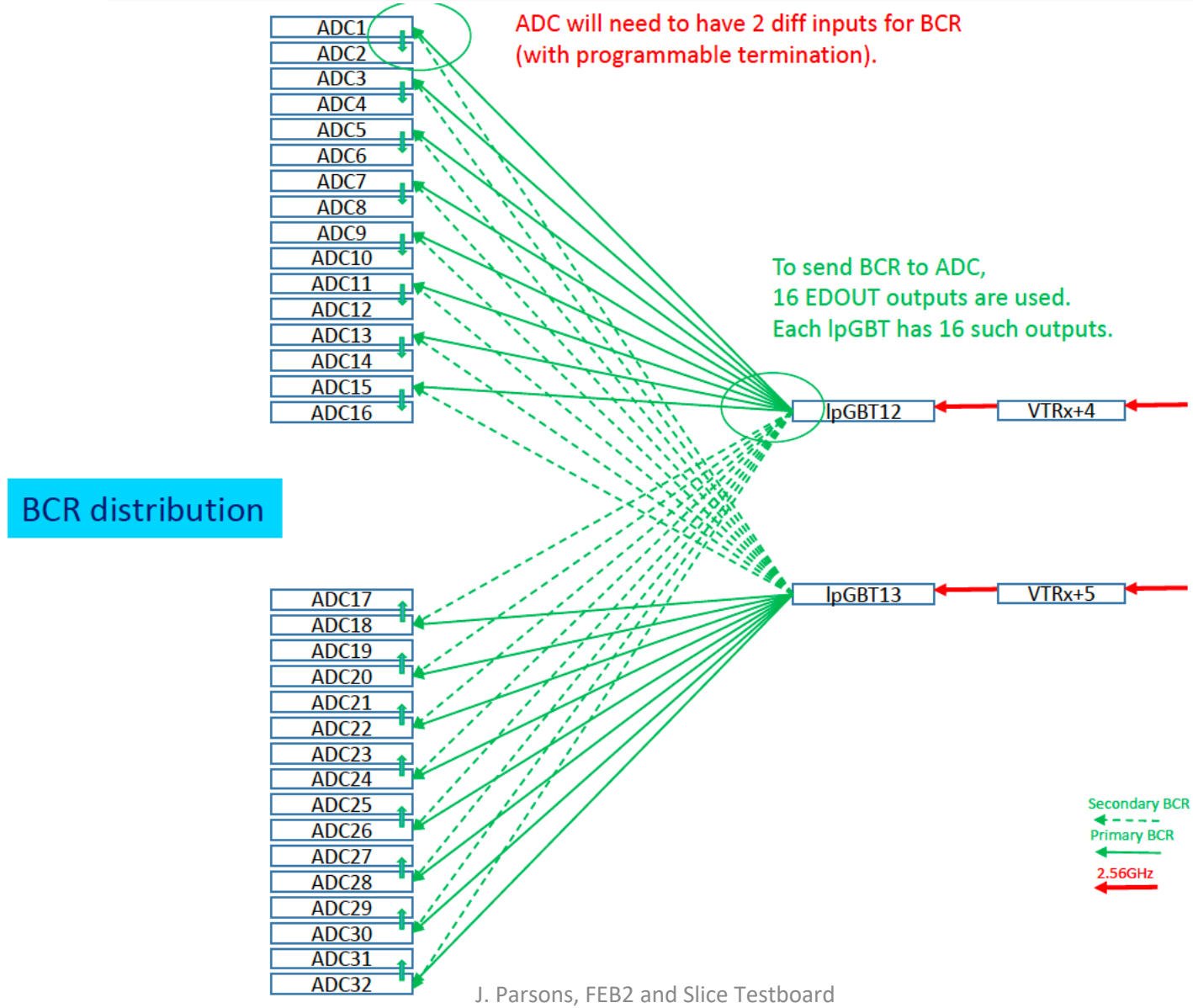


Data/signal flow

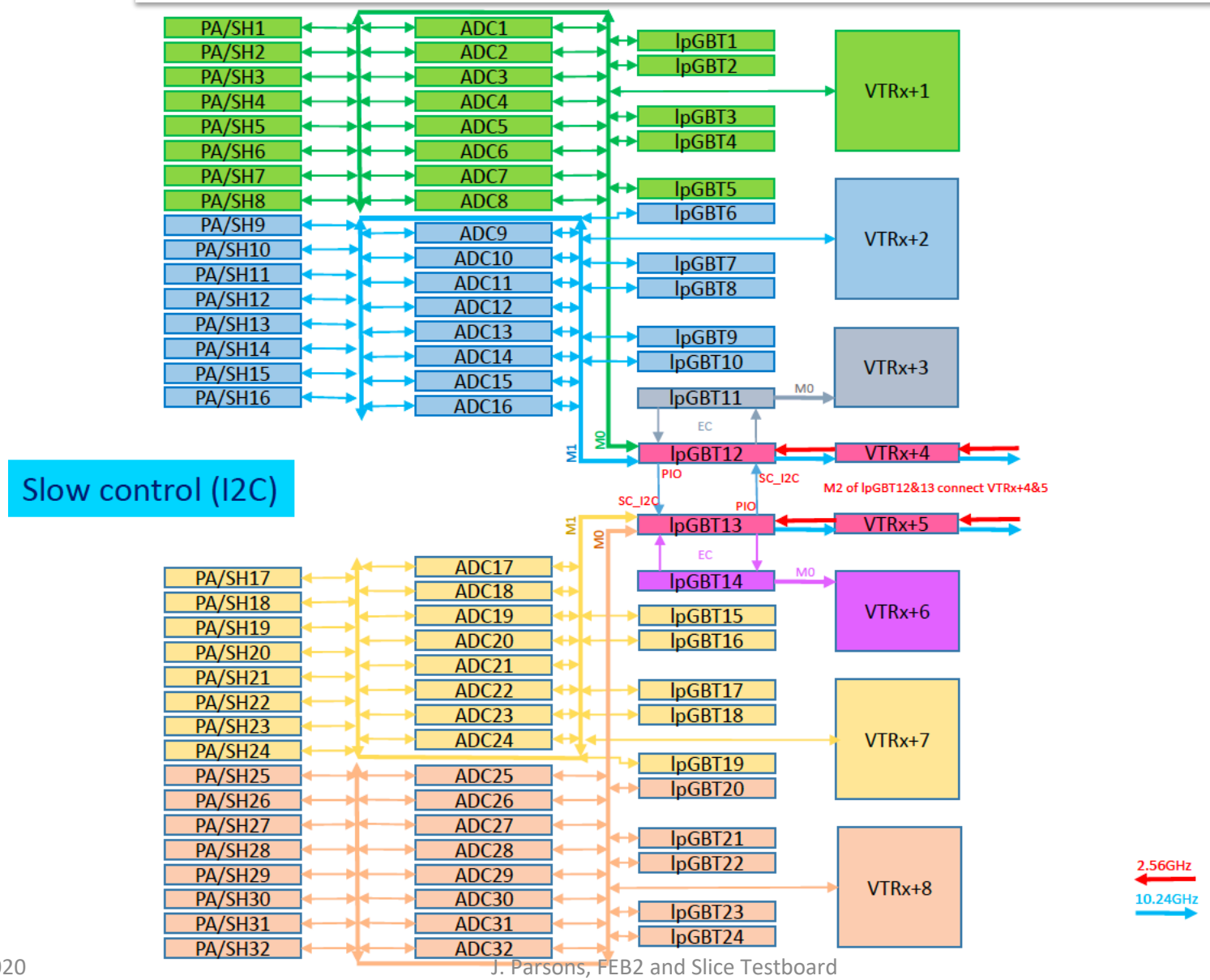
FEB2 Clock Distribution



FEB2 BCR Distribution



FEB2 Slow Control Distribution

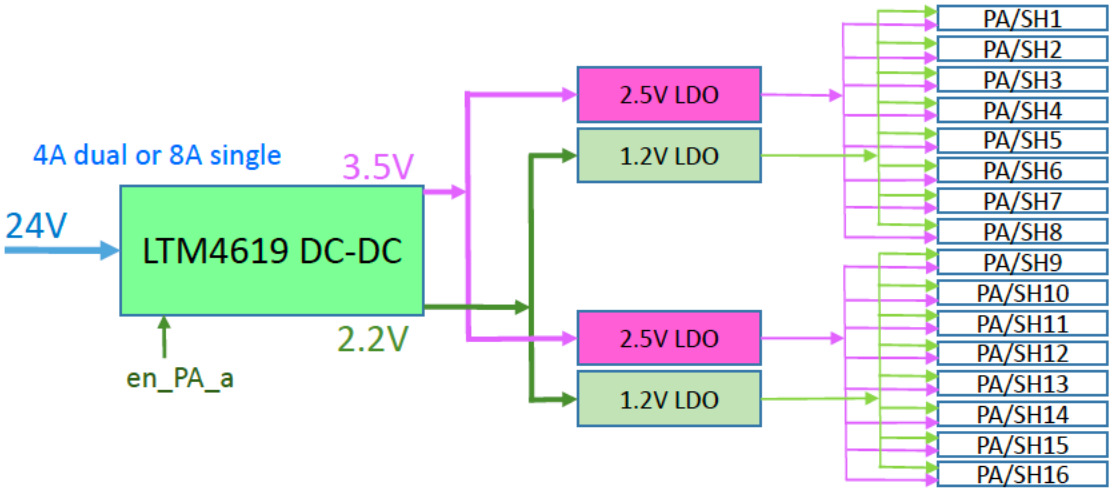


Slow control (I2C)

FEB2 Power Distribution

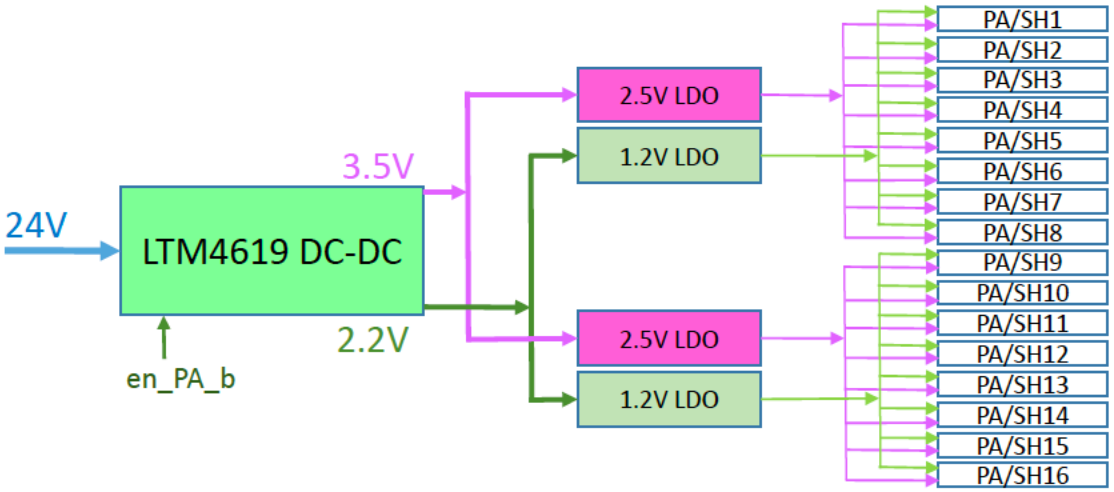
- Goal has been to achieve total FEB2 power budget similar to that of current FEB, namely 80 – 100 W per 128-channel board
  - However, while FEB power is used at typically ~5 V, most FEB2 power is needed at 1.2 V → FEB2 will need much more (~ 5X) regulated current than FEB
  - The current FEB has 6 input voltages, followed by 19 low-dropout (LDO) voltage regulators, each limited to a current of < 1 A
    - For the current FEB, about 20% of the power is dissipated in the LDOs
  - The FEB2 will have 1 input voltage (24 or 48 VDC), and will use DC-DC convertors before LDOs to be able to operate LDOs with ~ 1V dropout
  - Given the higher regulated current needs, FEB2 will need MANY more LDOs than current FEB
    - As shown in following slides, we expect up to 68 LDOs per FEB2 !
    - For the FEB2, the DC-DC inefficiencies + LDO drops will contribute ~50% of the total power (assuming Vin = 24V, DC-DC effic = 90%, Dropout = 1V)
- The current FEB2 power estimate is ~ 106 W per board (see backup)
  - This would increase by ~10% if Vin = 48V and we need another layer of DC-DC to first get down to 24V (assuming 90% efficiency for the new DC-DC convertor)

FEB2 PA/S Power Distribution



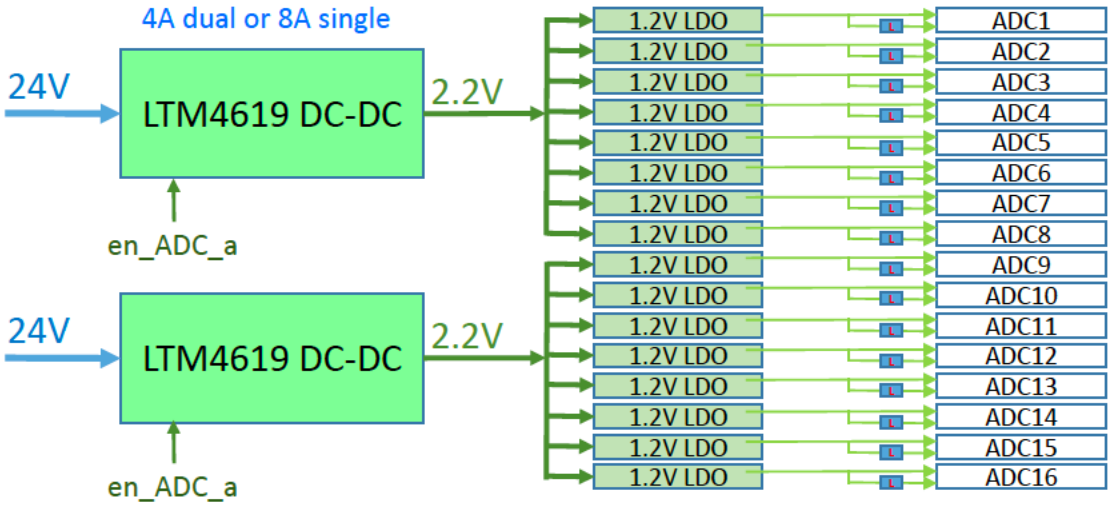
PA power
@2.5V < 100mA
@1.2V < 100mA

PA/SH power regulators



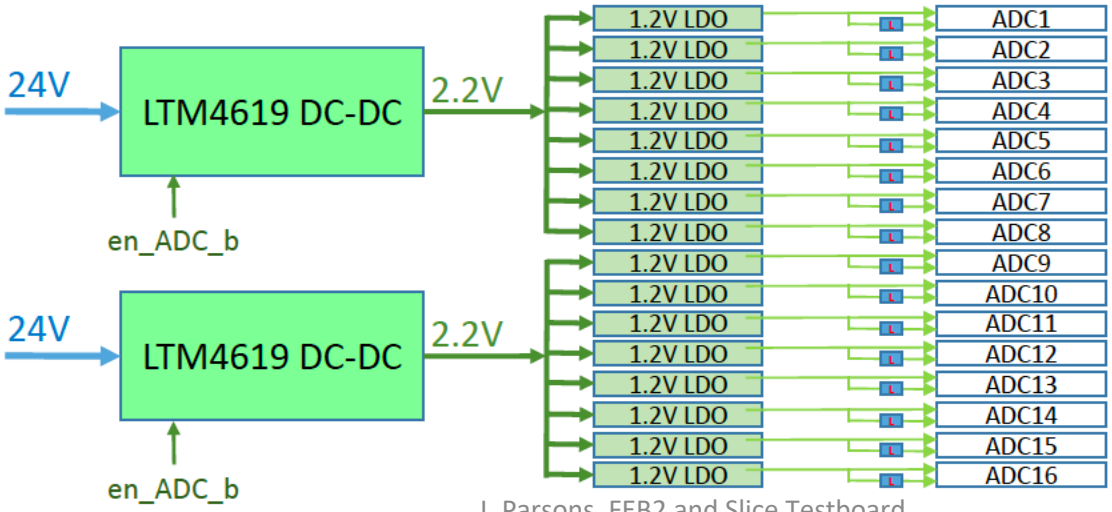
8 LDO's
2 DC-DC

FEB2 ADC Power Distribution



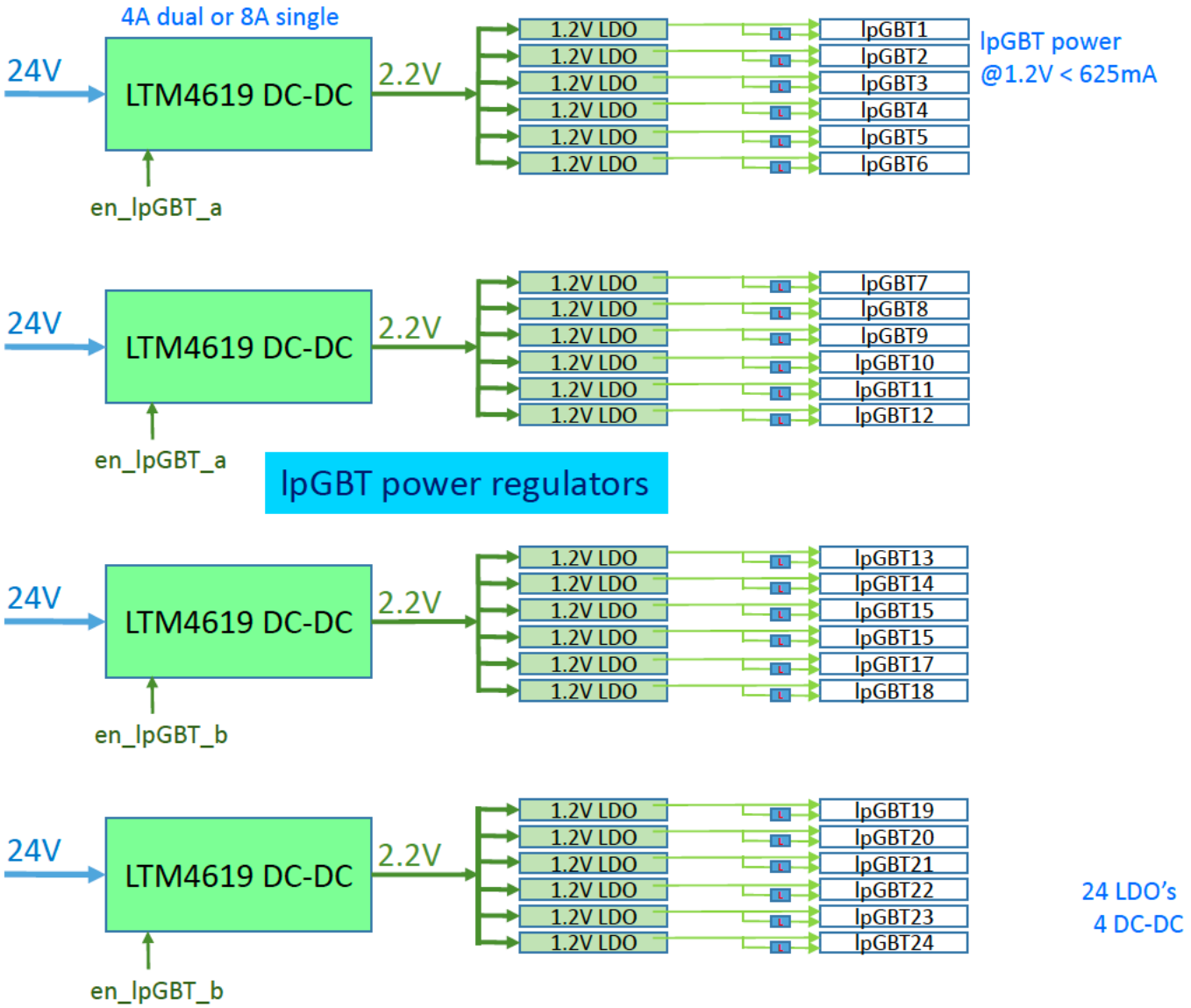
ADC power
@1.2VA < 610mA
@1.2VD < 70mA

ADC power regulators

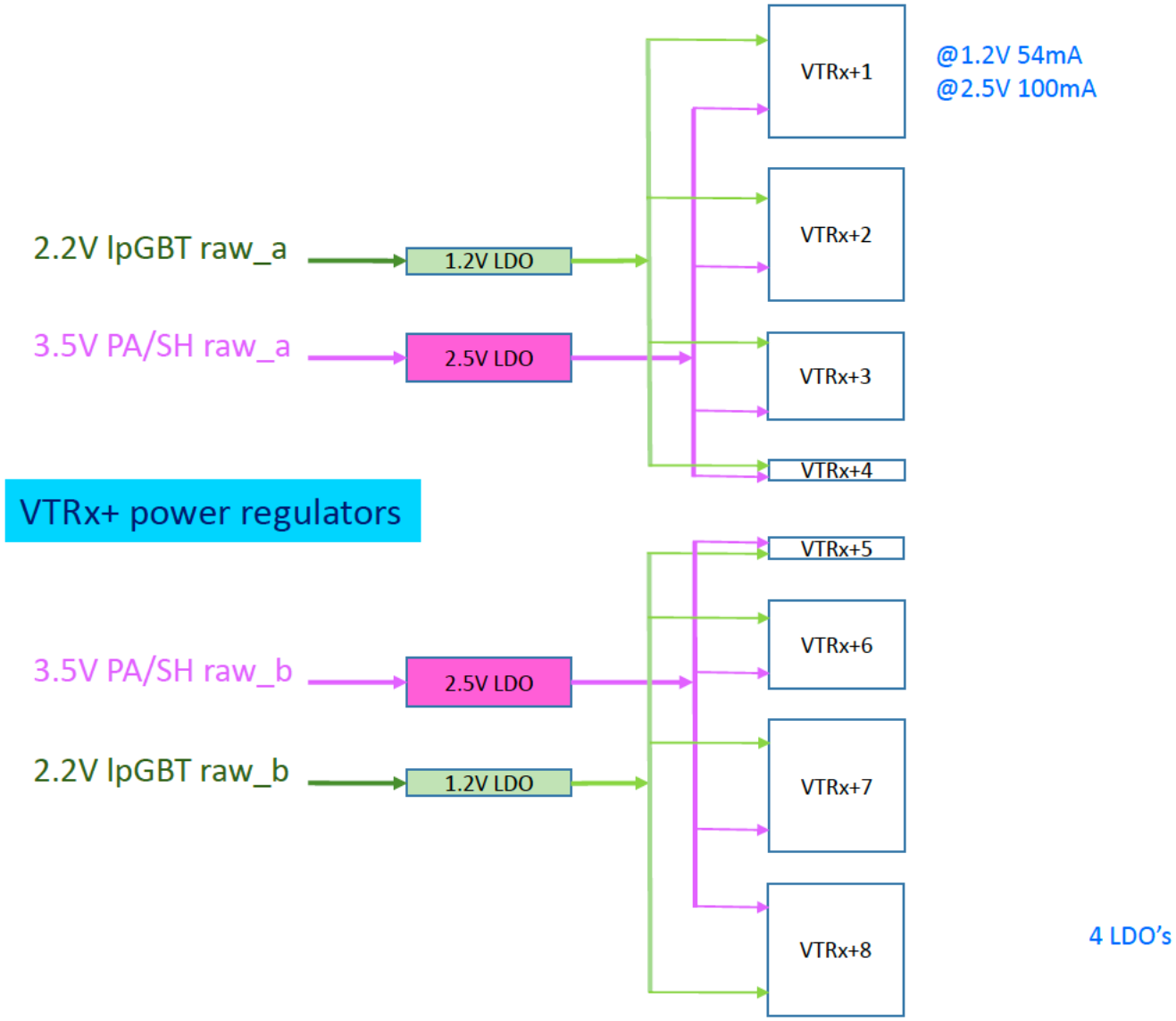


32 LDO's
4 DC-DC

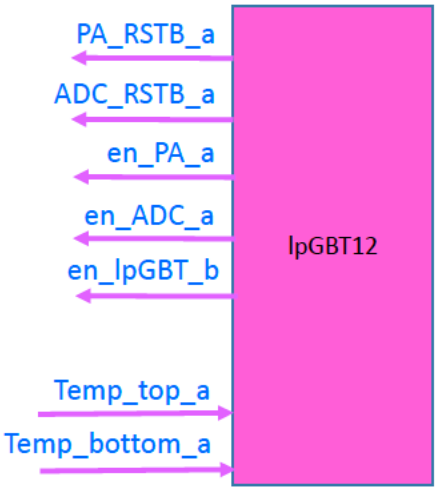
FEB2 lpGBT Power Distribution



FEB2 VTRx+ Power Distribution



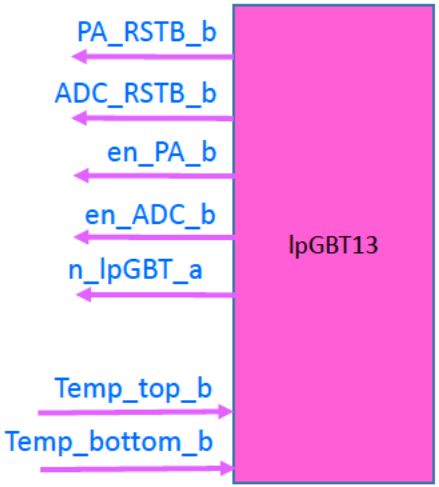
FEB2 Slow Control/Monitoring (1)



To generate resets and enable DC-DC conveters,
PIO pins are used.
Each lpGBT has 16 such outputs.

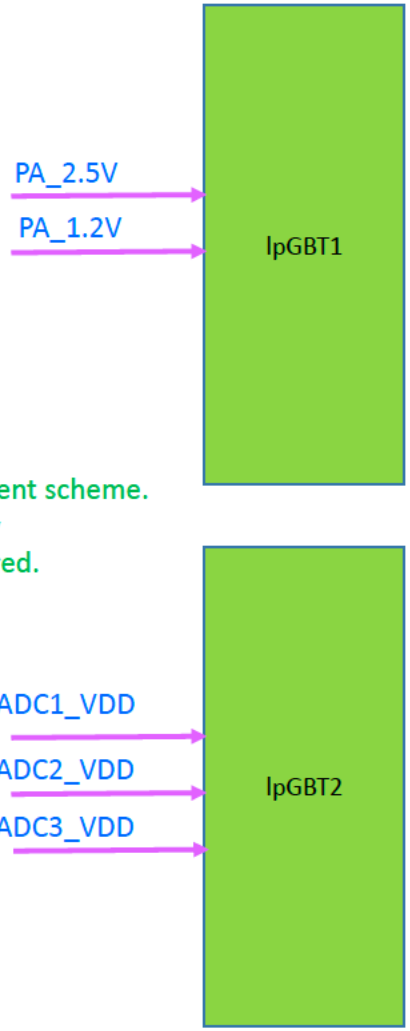
To measure the board temperatures,
Internal ADC is used.
Each lpGBT has 7way MUX to ADC.

Slow control & monitoring (1)



FEB2 Slow Control/Monitoring (2)

Slow control & monitoring (2)



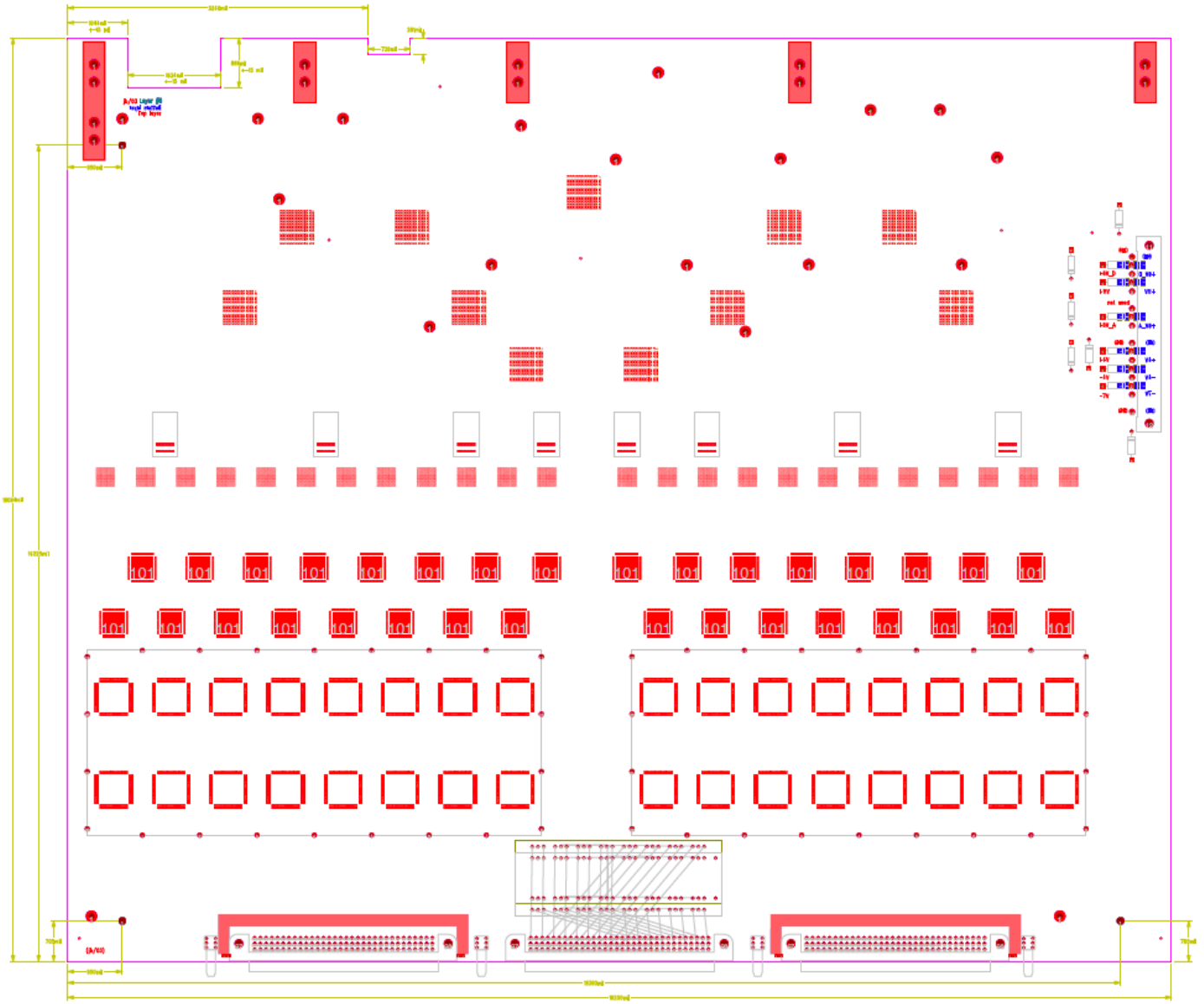
To measure the regulator voltages, an internal lpGBT ADC is used. Each lpGBT has 7way MUX to ADC.

Typical PS output measurement scheme. All PA and ADC power supply voltages are going to measured.

FEB2 Layout Topology

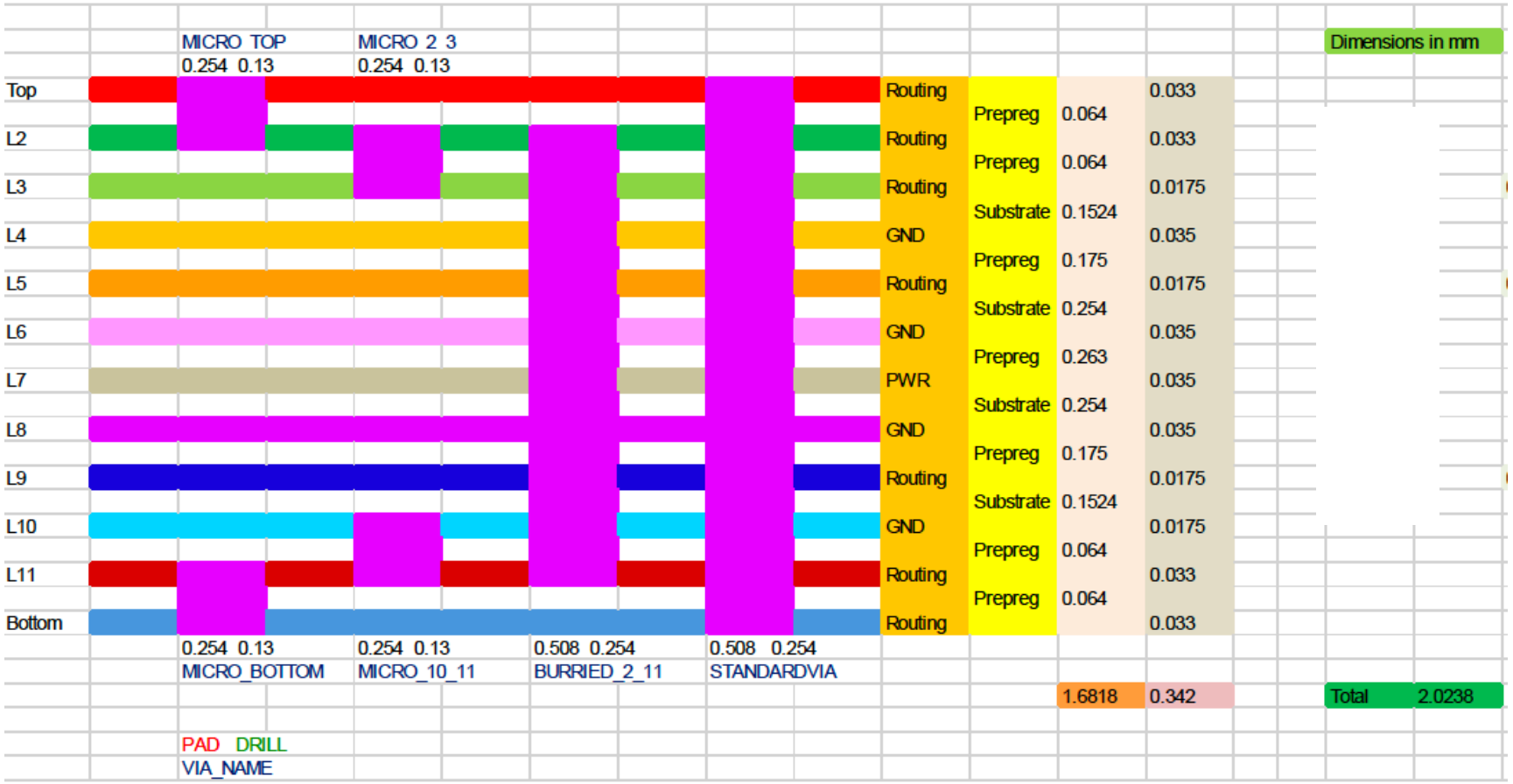
- The large number of LDOs required means that the FEB2 will not be able to have large non-segmented power planes
  - Instead, it is necessary to get the LDOs near to the components they will power
- This reason and others necessitate the need to place all (or most) or the active components on ONE SIDE of the FEB2 PCB, leaving the other side largely to powering (ie. placement of LDOs and filters, …)
- This single-sided topology is very different from the current FEB (which places Preamps + Shapers + ADCs on both sides), and places stringent constraints on the sizes of the packages of the custom ASICs
  - The current COLUTAv3 ADC package (100-pin QFN) is (marginally) OK, but the current LAUROC2 package is too large
  - We have, in any case, been considering moving both PA/S and ADC to BGA packages, which offer a number of potential advantages
    - Potentially smaller size, better analog performance due to more pwr/gnd pins and lower inductance, easier handling for robotic QC testing and for PCB assembly, …
  - For now the Slice Testboard development assumes the current packages, but we will adapt FEB2 development at a future date assuming a move to BGA packages

FEB2 Floorplan Study

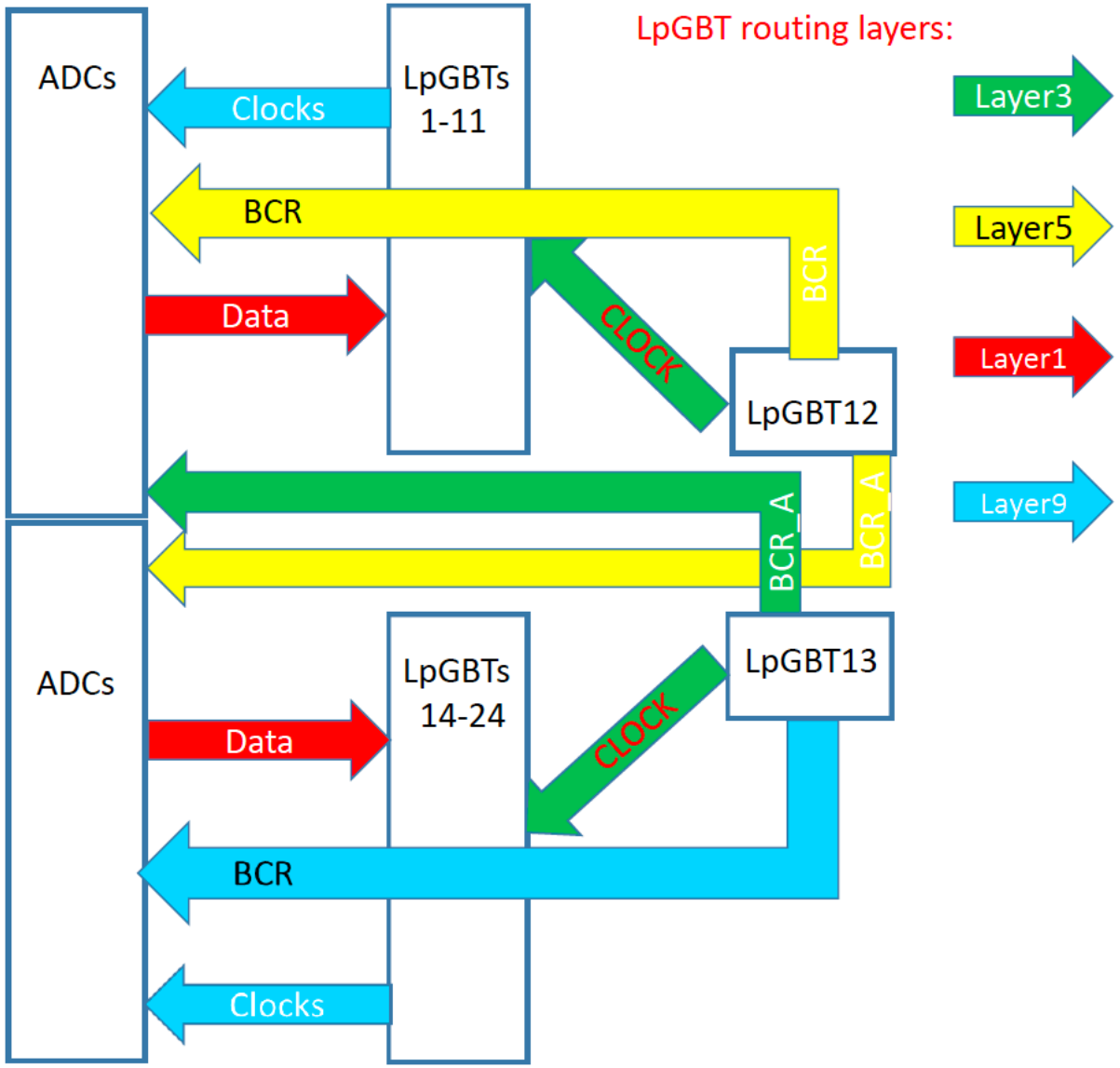


Tentative FEB2 Layout Stack-Up

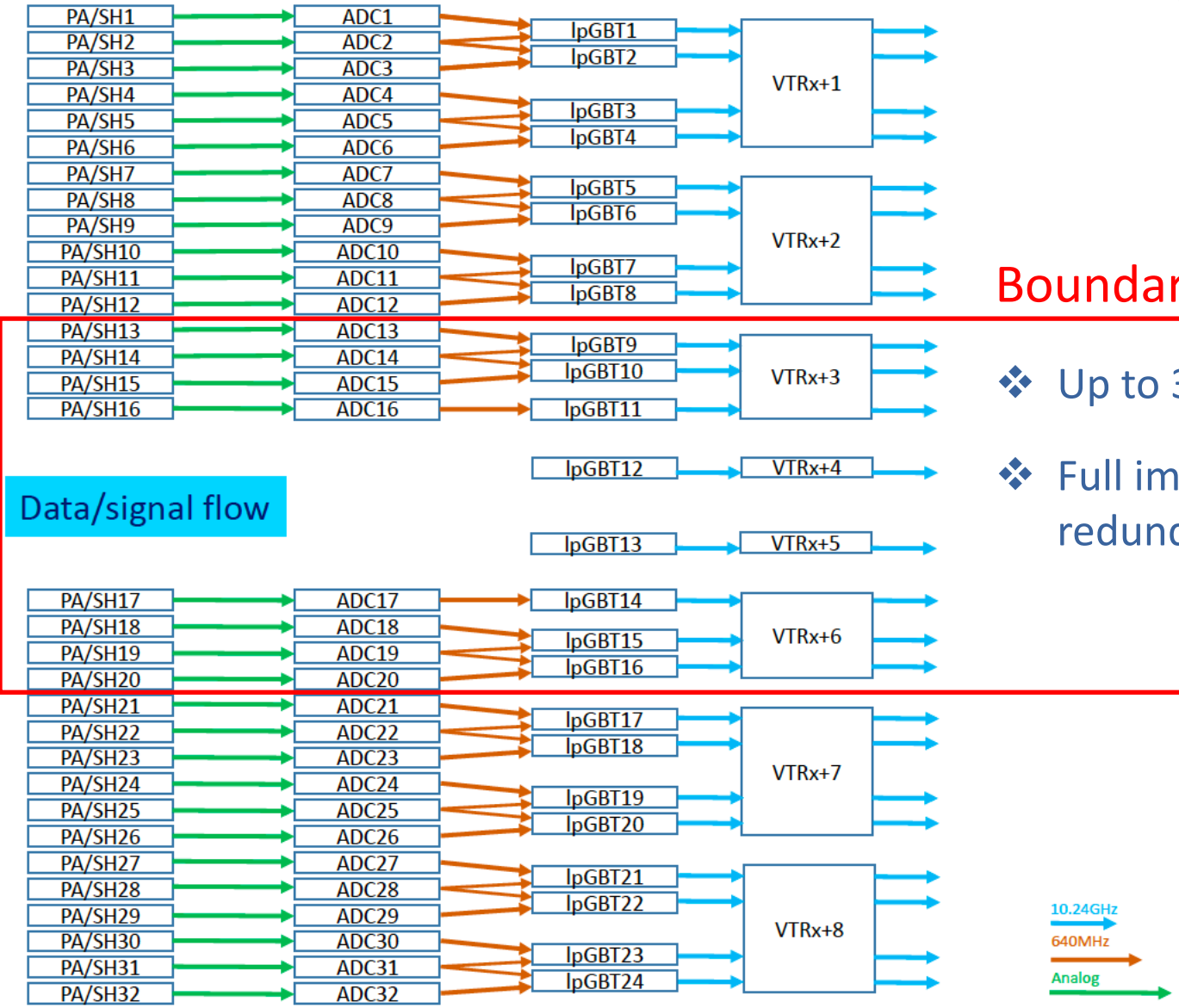
PCB stack-up



FEB2 Layout Routing



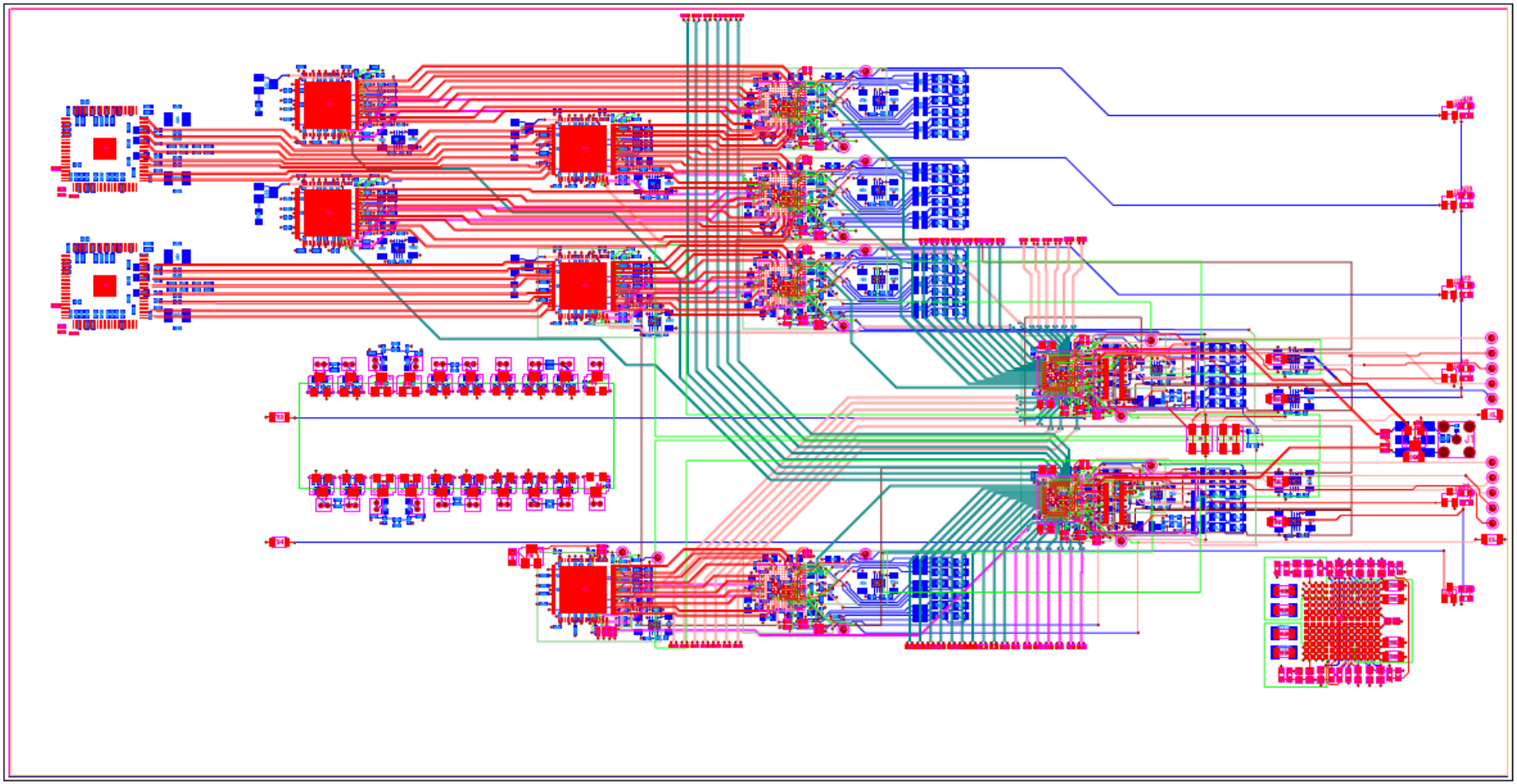
Slice Testboard Implementation



Boundary of Slice Testboard

- Up to 32 channels
- Full implementation of redundant control links

Slice Testboard Layout Exercise



Slice Testboard Timeline

- Good progress is being made on the design of the Slice Testboard, both schematic and layout
  - Starting with version for LAUROC2 + COLUTAv3, and using current packages
    - If versions for other solutions are needed, they will come later
- April 1 - aim to have Slice Testboard design complete
- May 15 – assuming ASIC availability, start debugging/testing of first 2 boards (partially assembled only, due to limited number of ASICs) at Columbia
- August 1 – could start assembling more boards for delivery to other labs
- September – testing could start in other labs

Note: this timeline is “success oriented”, and assumes all goes smoothly. For example, should the PCB design require iteration (not unlikely, given the large step in complexity), it is likely necessary to add 1-2 months.

Summary

- The FEB2 architecture has been specified in much greater detail, as represented in the block diagrams shown
  - With these details worked out, we can now proceed with the discussions of FEB2 specifications and interfaces
  - Aim to be ready to hold ATLAS SVR for FEB2 around time of April AUW
- The design of the Slice Testboard is proceeding well
  - Aim to have design complete by April 1, with board debugging at Columbia during the summer and testing in multiple labs starting in fall

Backup Slides

FEB2 Power Estimate

Component	Number/FEB2	Voltage (V)	Current (mA)	Power/Device (W)	Power/FEB2 (W)	Total/FEB2 (W)	Comment
Preamp/Shaper	32	2.5	63	0.16	5.04		125 mA measured for 2 LAUROC on Analog Testboard
	32	1.2	84.5	0.10	3.24		169 mA measured for 2 LAUROC on Analog Testboard
						8.28	Based on LAUROC1 measurements on Analog Testboard
ADC	32	1.2	610	0.73	23.42		VDD_analog
	32	1.2	70	0.08	2.69		VDD_digital
						26.11	Based on simulations of COLUTAv3
lpGBT	22	1.2	625	0.75	16.50		Data transmitters @ 10 Gbps
	2	1.2	625	0.75	1.50		Redundant bidirectional CLK/Control
						18.00	Based on upper bound from lpGBT datasheet
VTRx+	6	2.5	80	0.20	1.20		Data transmitters @ 10 Gbps
	6	1.2	45	0.05	0.32		Data transmitters @ 10 Gbps
	2	2.5	80	0.20	0.40		Redundant bidirectional CLK/Control
	2	1.2	45	0.05	0.11		Redundant bidirectional CLK/Control
						2.03	Based on VTRX+ datasheet for 4 Tx + 1 Rx (ie. conservative)
DC-DC							Assume 90% efficiency
For PA/S	2	Vin=24,Vout=3.5	1008	0.35	0.71		
	2	Vin=24,Vout=2.2	1352	0.30	0.59		
For ADC	4	Vin=24,Vout=2.2	5440	1.20	4.79		
For lpGBT	4	Vin=24,Vout=2.2	3750	0.83	3.30		
For VTRx+	2	Vin=24,Vout=3.5	320	0.11	0.22		
	2	Vin=24,Vout=2.2	180	0.04	0.08		
						9.69	Assume 90% efficiency
LDO							Assume 1 V dropout
For PA/S	4	2.5	504	0.50	2.02		
	4	1.2	676	0.68	2.70		
For ADC	32	1.2	680	0.68	21.76		
For lpGBT	24	1.2	625	0.63	15.00		
For VTRx+	2	2.5	80	0.08	0.16		
	2	1.2	45	0.05	0.09		
						41.73	Assume 1 V dropout
	68						
						105.85	**Grand Total**