# LAUROC2 Measurements

## ATLAS LAr Phase II Preamp/Shaper PDR

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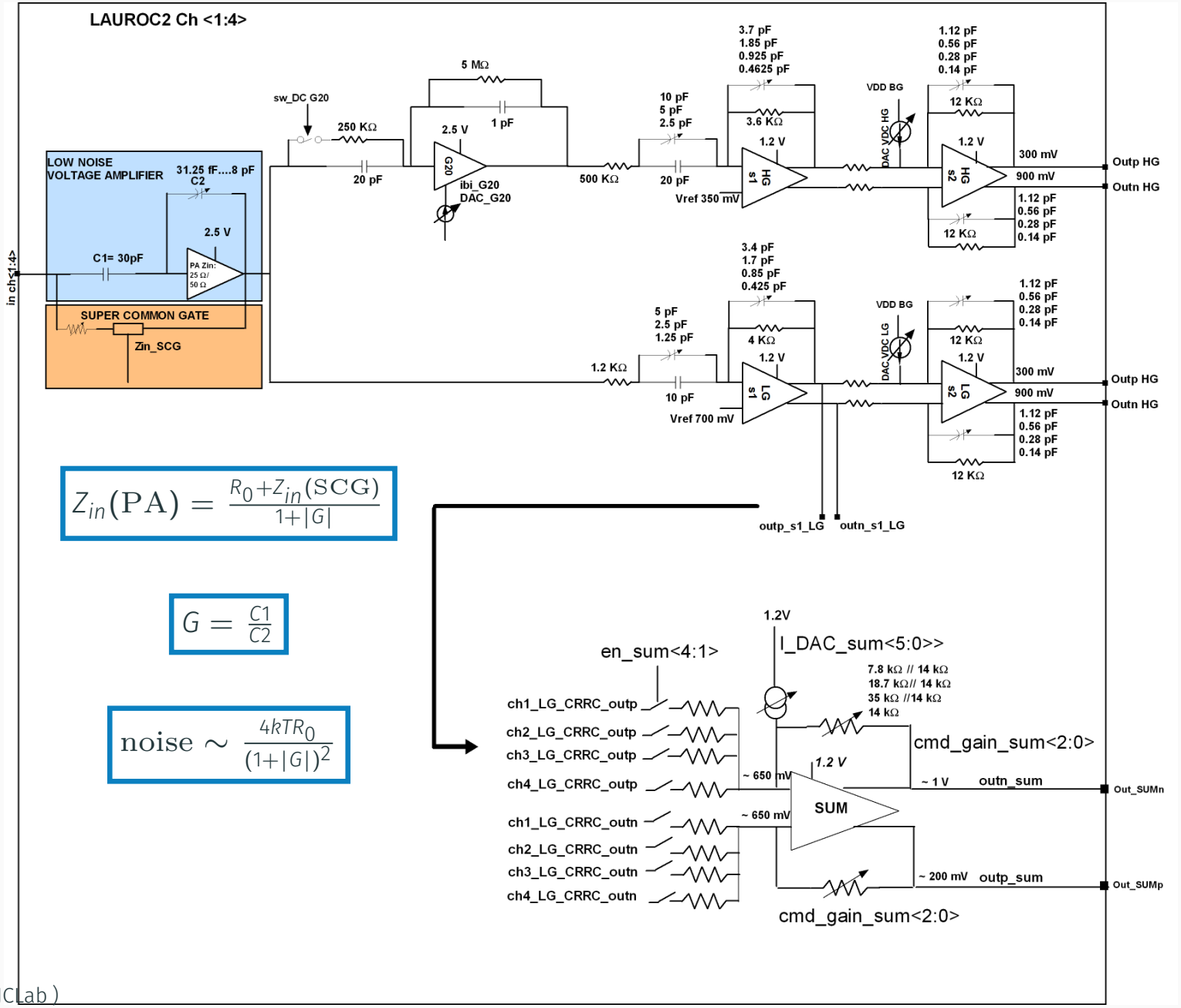
## LAUROC

- LAUROC: Liquid Argon Upgrade Readout Chip
- TSMC 130nm process
- Third iteration:
  - LAUROC0 (2016): test preamplifier design
  - LAUROC1 (2018): full functionality for main readout
  - LAUROC2 (2019): first chip with complete features

## Contents

LAUROC is our backup solution for preamp/shaper, despite passing basically all specifications

- Brief overview of the measurements
- With some more details on the I2C




$$Z_{in}(\mathrm{PA}) = \frac{R_0 + Z_{in}(\mathrm{SCG})}{1+|G|}$$

$$G = \frac{C1}{C2}$$

$$\mathrm{noise} \sim \frac{4kTR_0}{(1+|G|)^2}$$

## Functionality

- Allows 5bit addresses, each storing a byte of data

  ⇒ ∼ 256 config bits available

- Structure triplicated:
  - 3 clock inputs
  - 3 reset inputs
- Inputs: SCL, SDA, CLK40MHz, RST, chipID

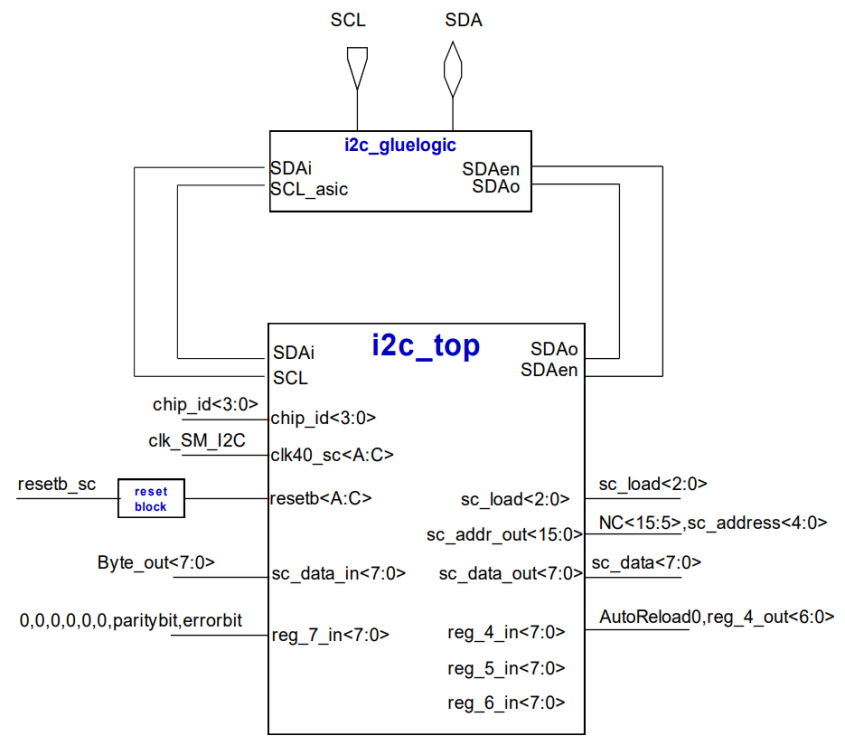
## Common design

- Design originally done for CMS HGCROC

  ⇒ Known to work in conjunction with lpGBT

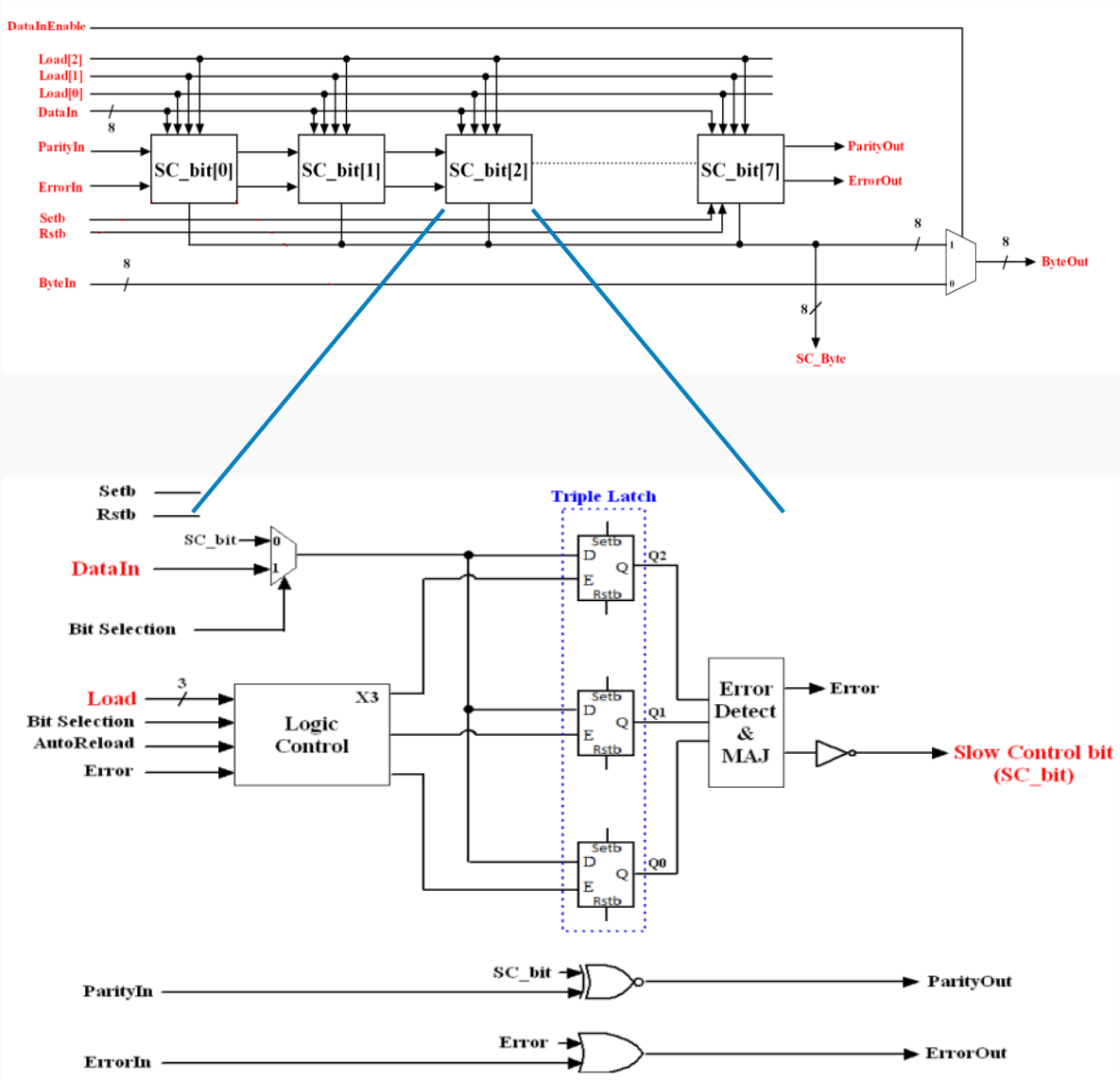
- LAUROC2 successfully integrated on the first FEB2 slice test board

  ⇒ Use demonstrated in ATLAS conditions



- Base cells aggregated by 8 to form SC Registers (byte)
- Inside a SC bit, triplicated structure with Triple voting
- Parity and Error propagated to next bit
- AutoReload functionality: force latch output to be reloaded if an error occurs

⇒ Intended use at the HL-LHC



# I2C Evolution

## Issue

Problem observed with some test boards with HGCROC

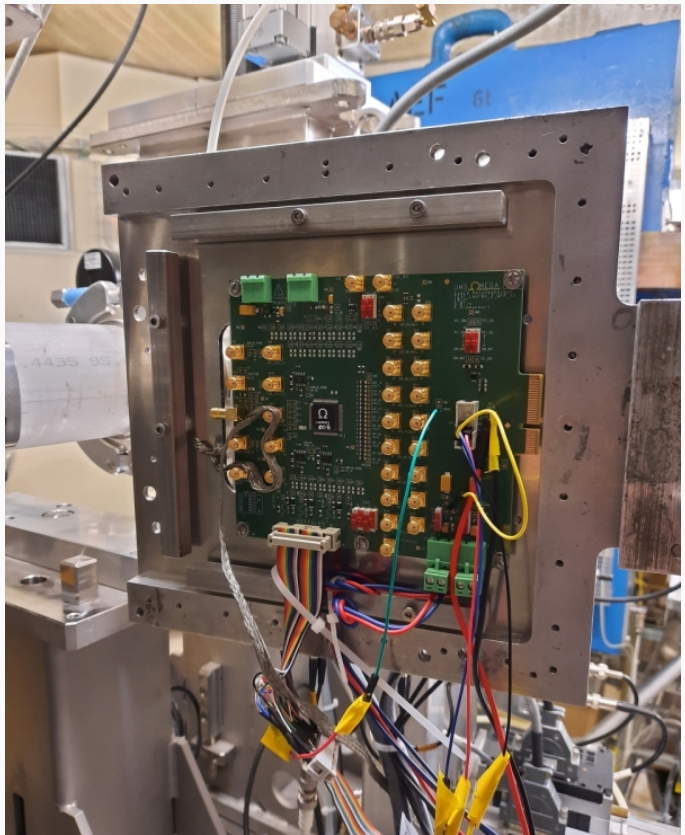
- When SCL and CLK40MHz not in sync
- In some cases the I2C gets stuck when writing the config
- Needs I2C reset then write the whole config again
- Could be reproduced on LAUROC when using different source for CLK40MHz than for SCL

## New Design

- I2C gets stuck because of clock gating mechanism
- Clock gating removed in new I2C version
- Also added resync of start and stop
- New I2C design shared on SOS server, to be used by ALFE and HPS

# I2C SEU TESTS

- Irradiation with protons on September 5-6 at the PIF facility at PSI
- 230 MeV protons, $\sim$ 15 hours beam time, irradiating a single board.
  - Total dose: 6.5 MRad
  - Total fluence: 1.4 $10^{14}$ p/cm$^2$ $\sim$ 14 times expected for HL-LHC
- I2C config read every 10 s and compared to original one
- Also monitor the error bit: flips whenever at least one latch flips in any SC bit.
- Runs in various configurations, typically with/without Autoreload functionality

## SEU

- 1 SC bit flip observed, in an Autoreload=OFF run.
- From the measurement of single latch flips (through the error bit), we expected 2 SC bit flips from independent latch flips during a 10 s window.
  - i.e flips that would not happen if we were running with Autoreload=ON
- Therefore no measurement of 'true' SEU rate possible
- Limit: $N < 3 \Rightarrow \sigma < 2\,10^{-14}\,\mathrm{cm}^2/\mathrm{chip}$ (95% CL)
- Translated to ATLAS: total number of bit flips over the whole calorimeter and for full HL-LHC lifetime: <6000

## NIEL

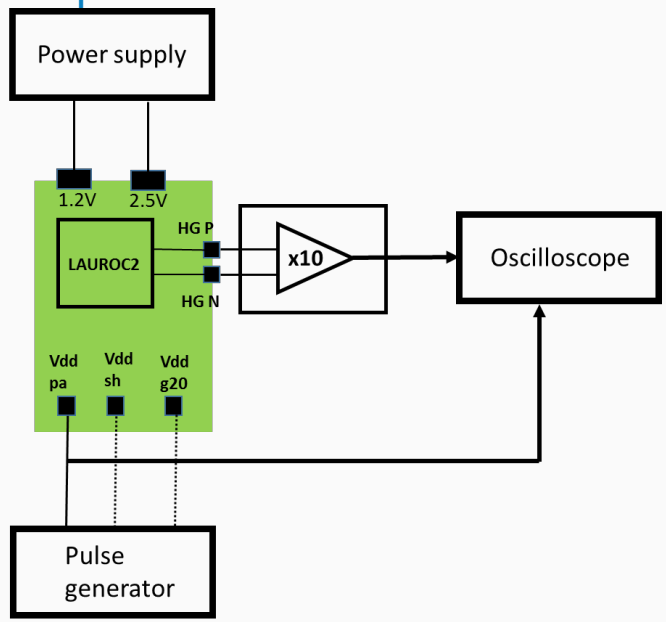
- ASIC still working at least up to 3.5 times the requirement

## TID

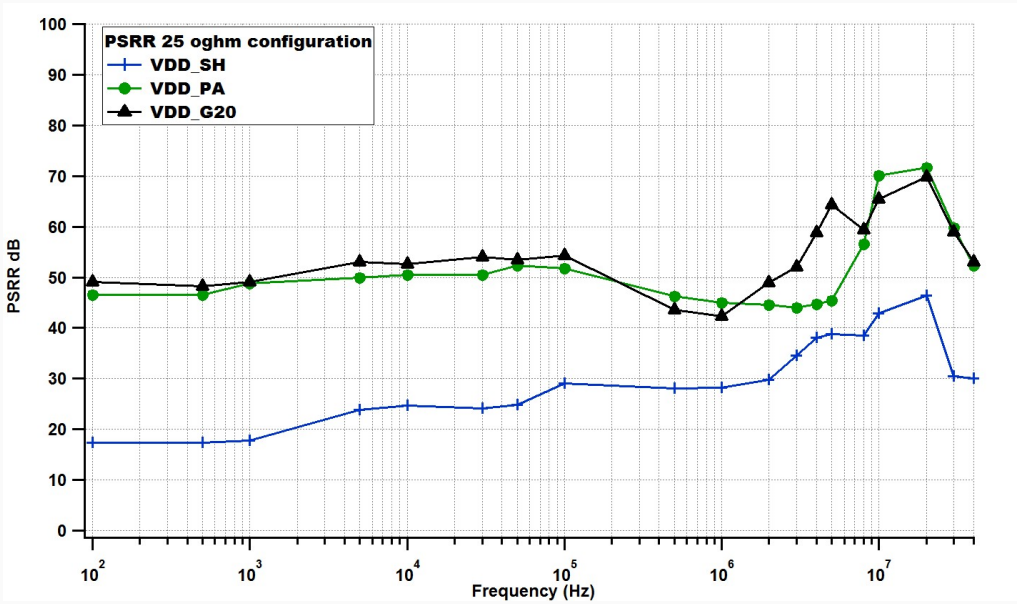
- Chip still working at 6.5 MRad
- Detailed characterization post-irradiation could not be performed at PIF due to technical issues
- Board still in active material storage at PSI
- However, LAUROC1 tested for TID at CERN (X-ray machine): no performance degradation observed on 5 boards irradiated to 1 MRad

- As LAUROC is our backup design, showing only a few significant results
- Typically only results for the 25Ω – 10mA configuration
- More in backup if needed
- Numbering scheme refers to the document listing all measurements to perform

## Setup




Sinusoidal signal
with variable frequency



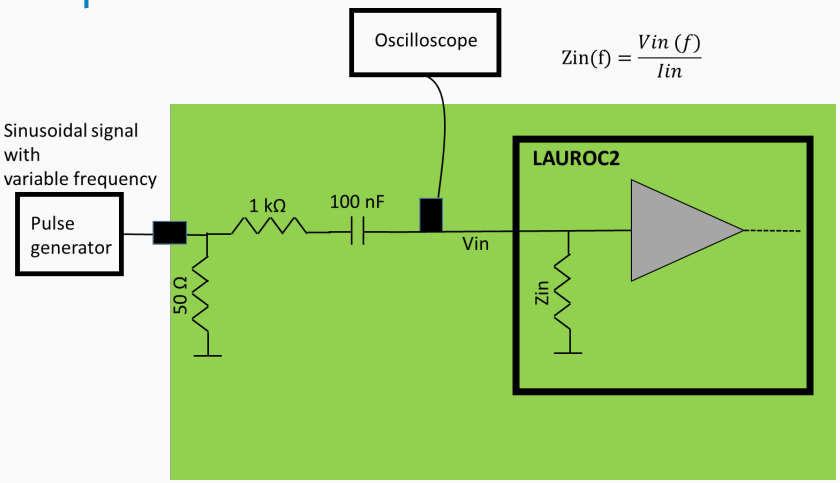

## Requirement: $>$ 10 dB up to 1 MHz

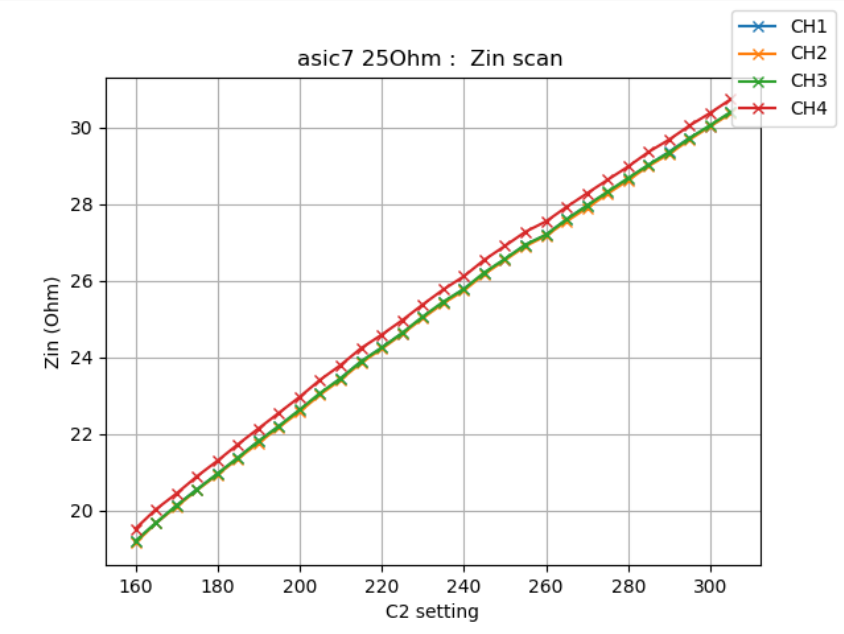
- $>$ 20 dB for VDD_SH
- $>$ 45 dB for VDD_PA and VDD_G20

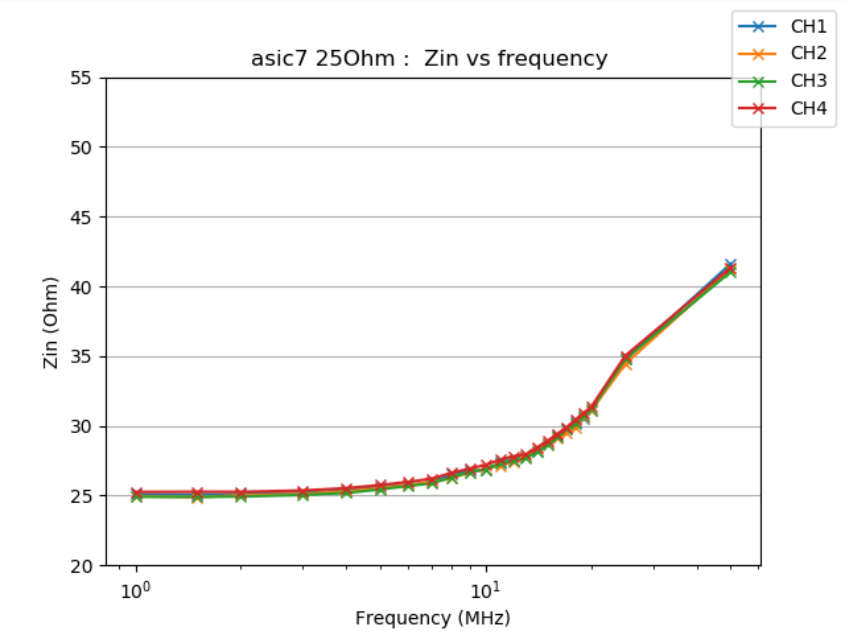
## Tuning range
From 3 Ω to 42 Ω

## Stability vs frequency
- ±10% up to 20 MHz, vs requirement ±5%
- ±5% up to 10 MHz
- Central frequency ∼ 3 — 4 MHz: no significant impact from larger deviations above 10 MHz

## Setup



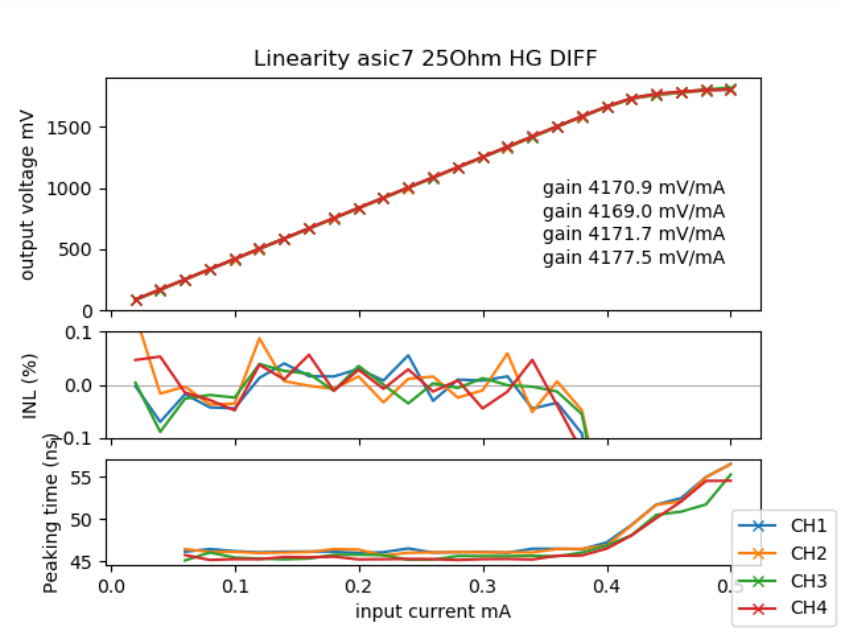



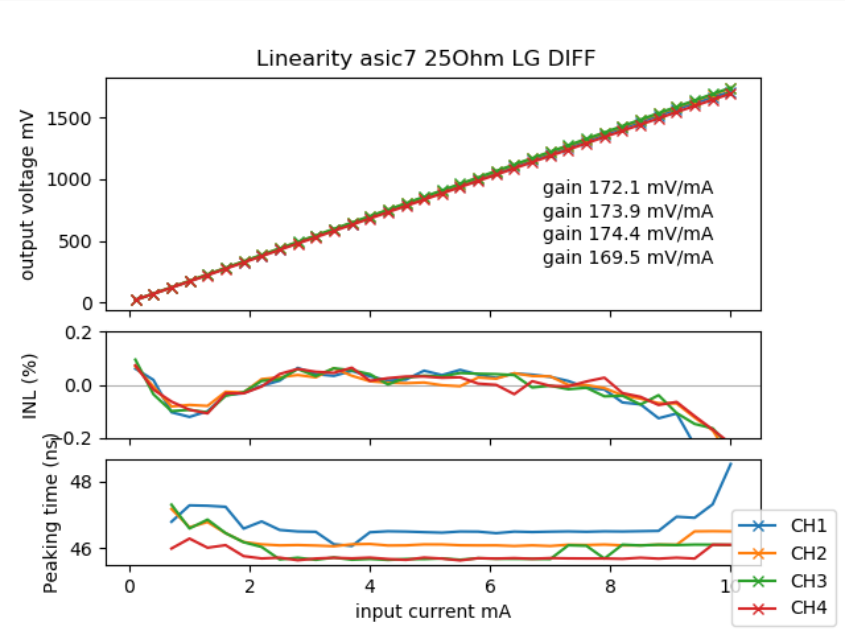
## High Gain

- INL ±0.1% vs requirement ±0.2%
- Peaking time stability: ∼ 1 ns

## Low Gain

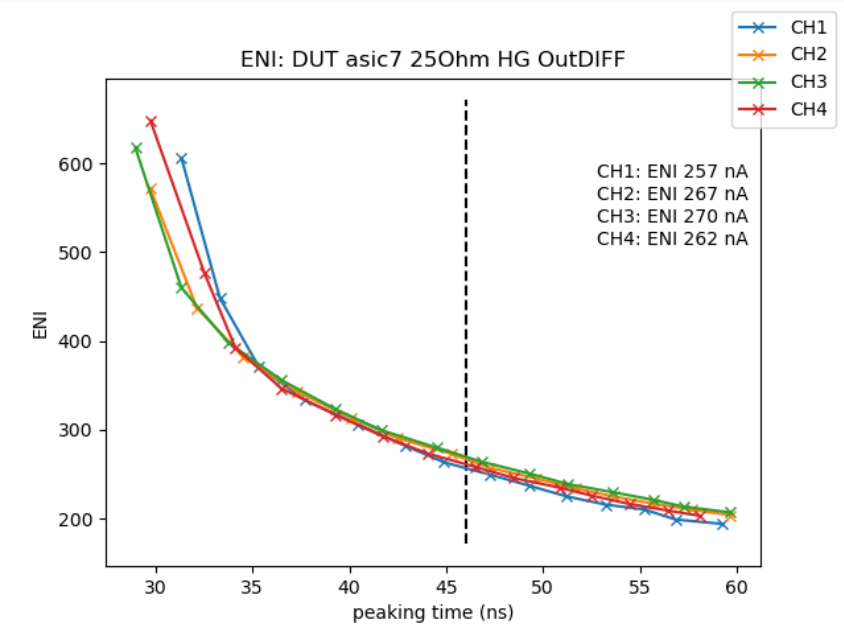
- INL ±0.2% vs requirement ±0.5%
- Peaking time stability: ∼ 1 ns
- Gain ratio HG/LG: ∼ 24 vs requirement 23 ± 5

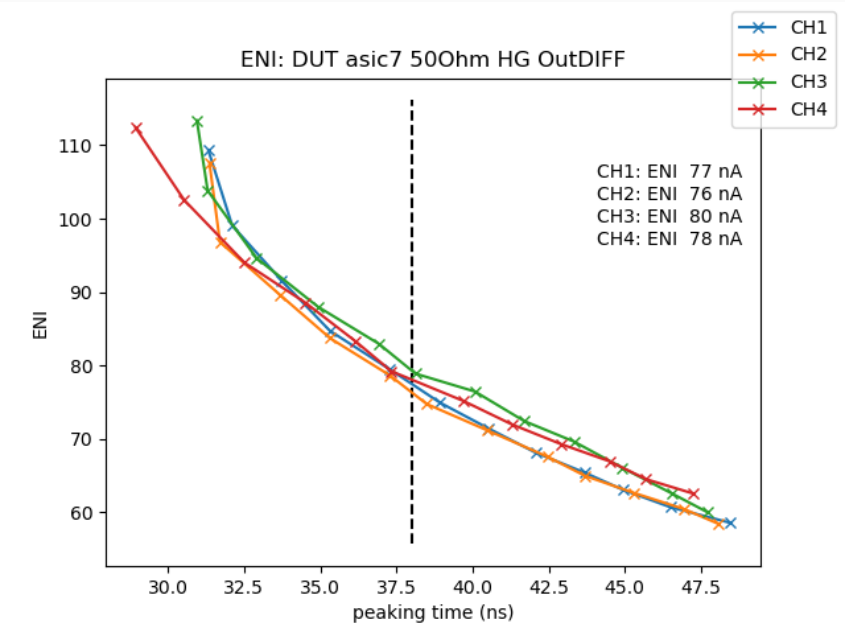


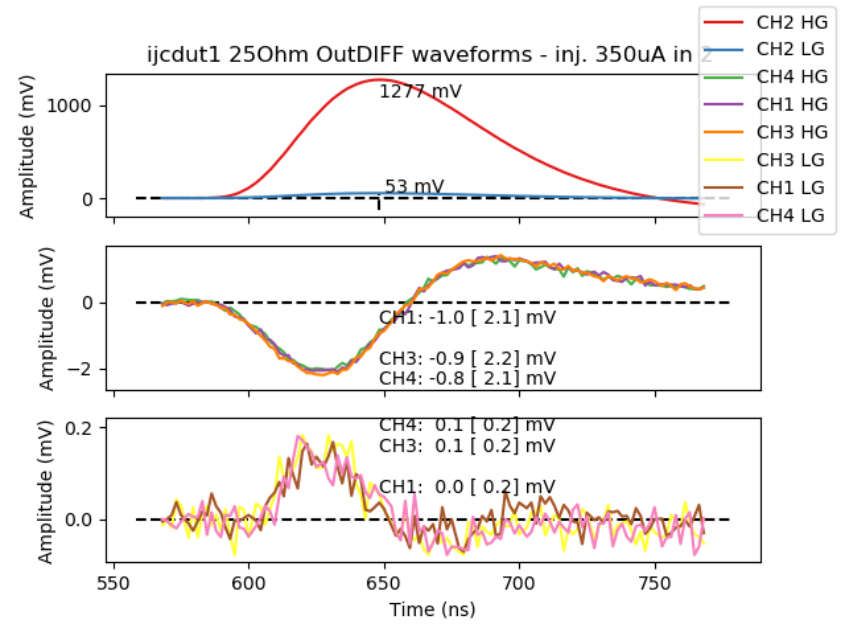
## ENI

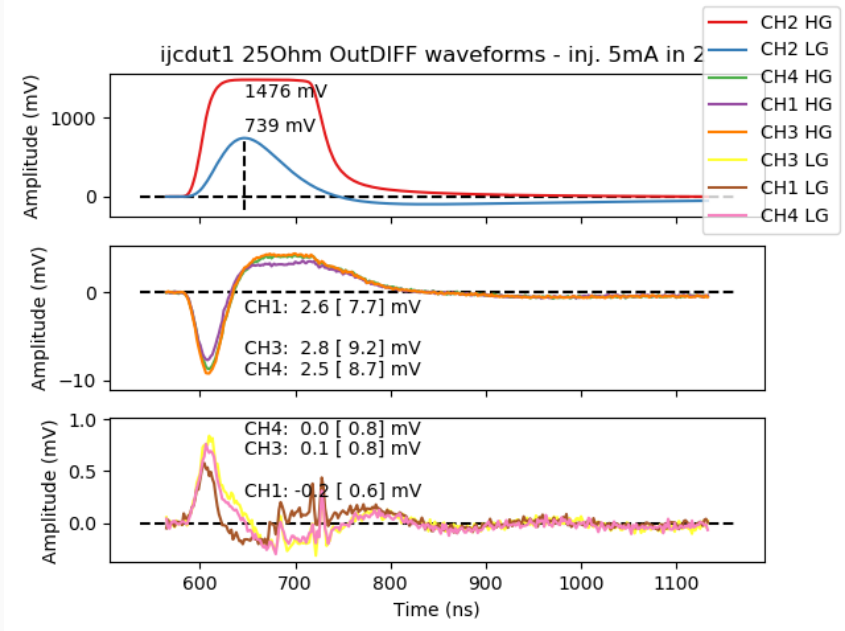
- 25Ω: ENI= 265 nA at $t_p^{5-100\%} = 46$ ns with $C_d = 1.5$ nF vs requirement $< 350$ nA
- 50Ω: ENI= 78 nA at $t_p^{5-100\%} = 38$ ns with $C_d = 330$ pF vs requirement $< 120$ nA
- Coherent noise: 22% coherent noise fraction



# 3.G.1-4 Cross-talk




| inj CH2 | HG vs HG at peak | HG vs HG pk-to-pk | LG vs HG at peak | LG vs HG pk-to-pk | LG vs LG at peak | LG vs LG pk-to-pk |
|---|---|---|---|---|---|---|
| CH1 | 0.08% | 0.16% | 0.35% | 1.04% | 0.01% | 0.11% |
| CH3 | 0.07% | 0.17% | 0.38% | 1.24% | 0.01% | 0.11% |
| CH4 | 0.06% | 0.16% | 0.34% | 1.17% | 0.02% | 0.08% |

## Cross-talk

- Evaluated at peak of injected pulse
- All good vs requirement 0.5%
- Peak-to-peak cross-talk shown as well

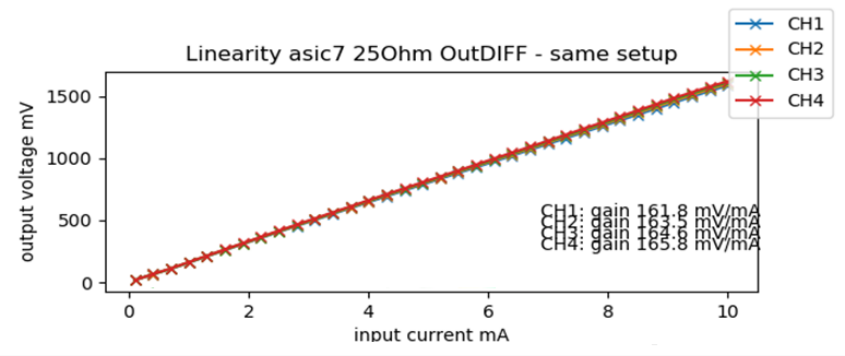
# 3.I.1-3 Uniformity

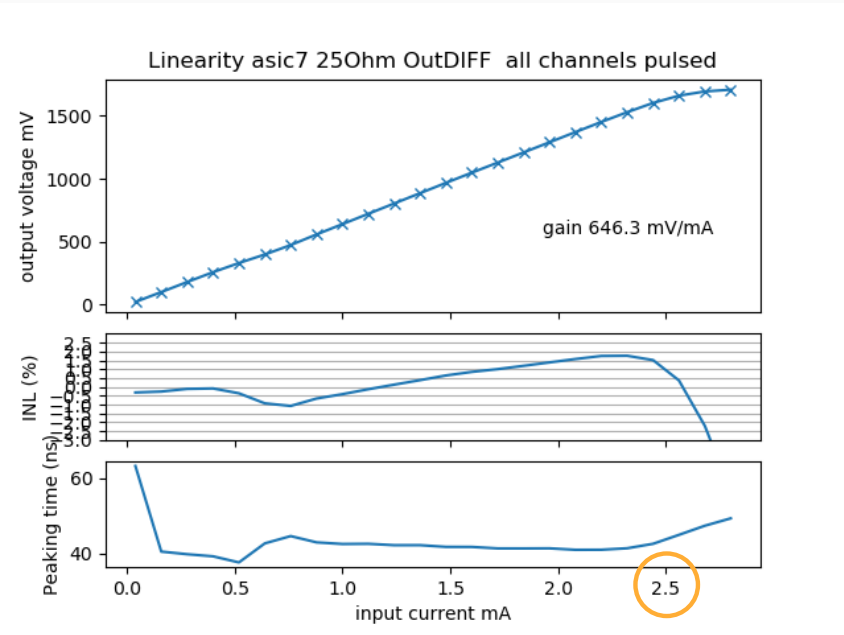
- Measured on 8 ASICs using a board with a socket
- Performance not exactly as boards with soldered chips
- But sufficient to measure dispersions (RMS)

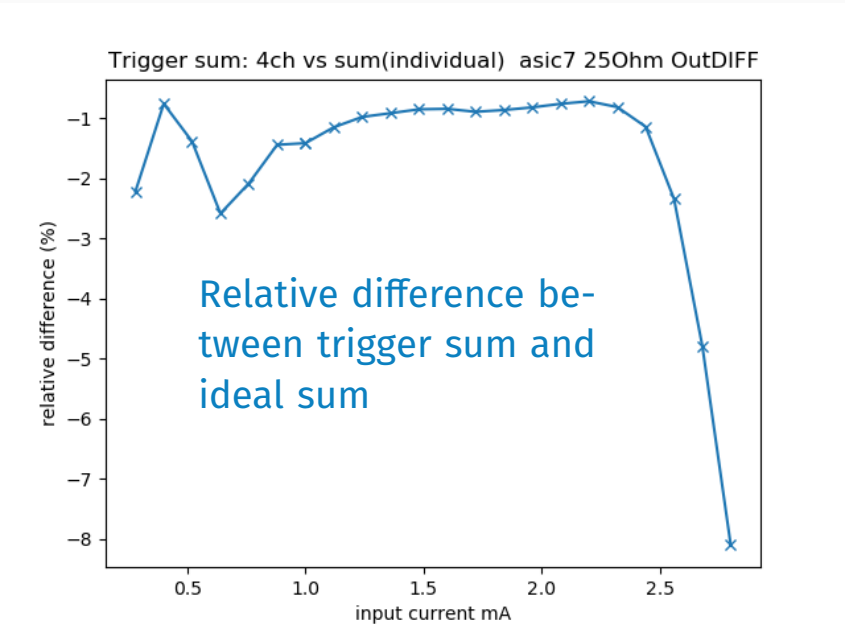
| | RMS 25Ω | RMS 50Ω |
|---|---|---|
| Gain HG | 0.8% | 1.7% |
| Gain LG | 0.6% | 2% |
| ENI | 2.7% | 4.5% |
| $Z_{in}$ | 1.1% | 1.4% |

## Trigger sum

- LAUROC2 designed with gains x1 / x1.5 / x2.5 / x3.5 before requirements were fixed with x1 / x3
- Gain uniformity: $< 1.3\%$ vs requirement $< 5\%$
- INL $< \pm 2\%$
- Peaking time tuning and stability ok
- Shaper switches working ok




2.5 mA/channel $\Rightarrow$ 10 mA total

# Summary: 25Ω

| Category | Measurement | Requirement |
|---|---|---|
| **1. Nominal settings** | | |
| 4. HG/LG Gain ratio | 24 | $23 \pm 5$ |
| Peaking time, DC levels | All ok | |
| **2. Power** | | |
| 1. Power consumption | $\sim$ 450 mW | $<$ 650 mW |
| 5. PSRR | 50 dB for VDD_PA and VDD_G20 ; 20 dB for VDD_SH | 10 dB up to 1 MHz |
| **3. Main Readout** | | |
| A. Input impedance | $\pm$5% up to 10 MHz | $\pm$5% up to 20 MHz |
| B.1 Recovery time | $\sim$ 100 ns | $<$ 450 ns |
| B.2 Output DC tuning | HG: $\pm$145 mV ; LG: $\pm$150 mV | Tuning range $\pm$150 mV |
| C.1-2 INL | HG: $\pm 0.1\%$ up to 370 $\mu A$ ; LG: $\pm 0.2\%$ up to 10 mA | HG: $\pm 0.2\%$ ; LG: $\pm 0.5\%$ |
| C.3 Optimal filtering | Same results | Same requirement |
| C.4 ADC Load | Same results | Same requirement |
| D.1 Peaking time tuning | $t_p^{5-100\%} = 46$ ns $\pm 12$ ns | $\tau = 15$ ns $\pm 5$ ns |
| D.2 Peaking time linearity | 45.5 – 46.3 ns | |
| E. Phase margin | Min: 62.4 deg ; Nom: 66 deg | 60 deg |
| F. Noise | ENI= 264 nA at $t_p^{5-100\%} = 46$ ns | 350 nA at $t_p^{5-100\%} = 46$ ns |
| G. Cross-talk | Negligible | $< 0.5\%$ |
| H. High Pileup Behaviour | No internal saturation | No saturation |
| **4. Trigger Summing Output** | | |
| 1. Gains | x1 and x3.7 | x1 and x3 |
| 2. Linearity | INL $< 2\%$ up to 10 mA | INL $< 2\%$ |
| 3. Uniformity | Gain uniformity $< 1.5\%$ | $< 5\%$ |

# Summary: 50Ω

| Category | Measurement | Requirement |
|---|---|---|
| **1. Nominal settings** | | |
| 4. HG/LG Gain ratio | 30 | $23 \pm 5$ |
| Peaking time, DC levels | All ok | |
| **3. Main Readout** | | |
| A. Input impedance | $\pm 5\%$ up to 20 MHz | $\pm 5\%$ up to 20 MHz |
| B.1 Recovery time | $\sim$ 100 ns | $<$ 450 ns |
| B.2 Output DC tuning | HG: $\pm 145$ mV ; LG: $\pm 150$ mV | Tuning range $\pm 150$ mV |
| C.1-2 INL | HG: $\pm 0.1\%$ up to 55 $\mu A$ ; LG: $\pm 0.2\%$ up to 2 mA | HG: $\pm 0.2\%$ ; LG: $\pm 0.5\%$ |
| C.3 Optimal filtering | Same results | Same requirement |
| C.4 ADC Load | Same results | Same requirement |
| D.1 Peaking time tuning | $t_p^{5-100\%} = 38$ ns $\pm 10$ ns | $\tau = 15$ ns $\pm 5$ ns |
| D.2 Peaking time linearity | 37 – 38 ns | |
| F. Noise | ENI$= 74$ nA at $t_p^{5-100\%} = 38$ ns | 120 nA at $t_p^{5-100\%} = 38$ ns |
| G. Cross-talk | Negligible | $< 0.5\%$ |
| **4. Trigger Summing Output** | | |
| 1. Gains | x1 and x3.7 | x1 and x3 |
| 2. Linearity | INL $< 2\%$ up to 10 mA | INL $< 2\%$ |
| 3. Uniformity | Gain uniformity $< 1.5\%$ | $< 5\%$ |

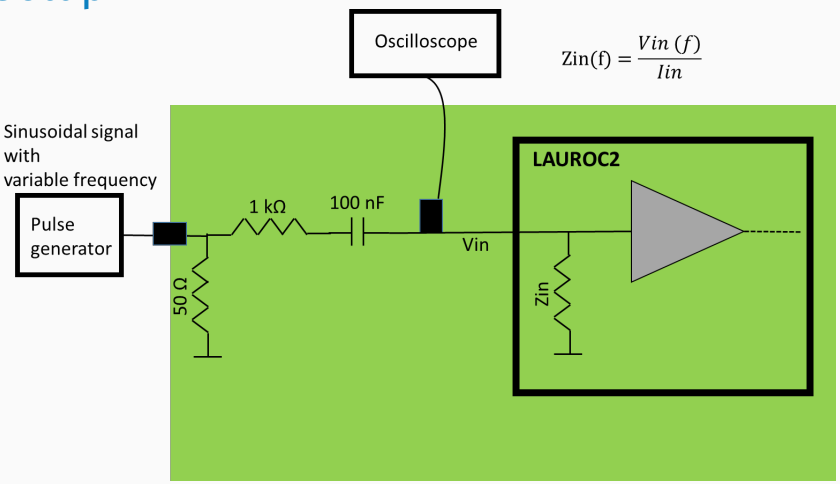
# Backup Material

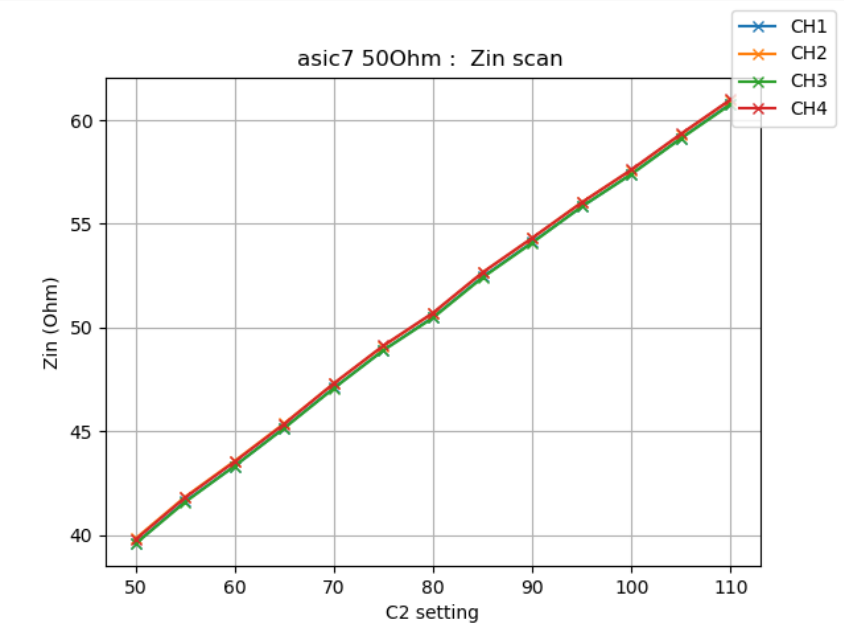
# 3.A.1-2 Input Impedance 50ω

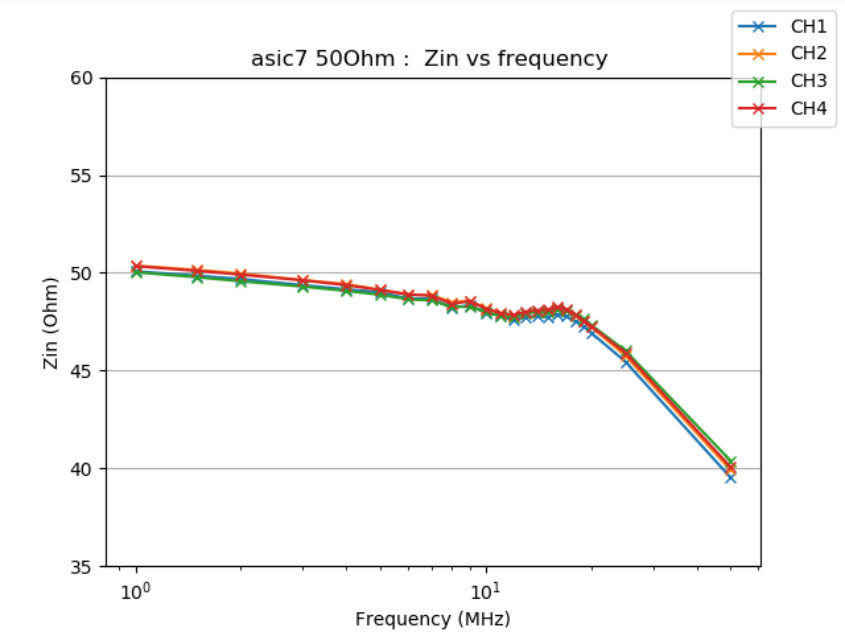
## Tuning range
From 19 Ω to 148 Ω

## Stability vs frequency
- ±5% up to 20 MHz, vs requirement ±5%

## Setup



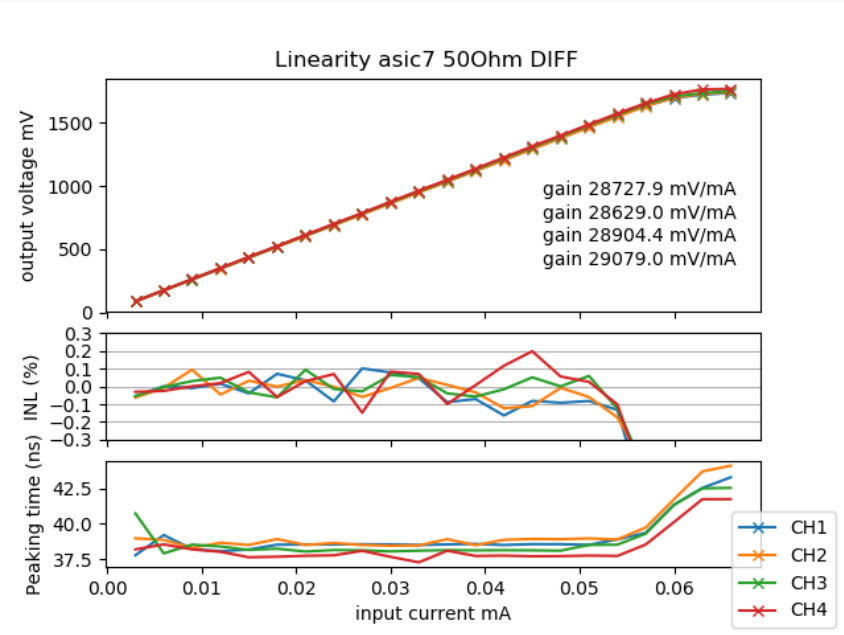



# 3.C.1-2 Linearity 50Ω

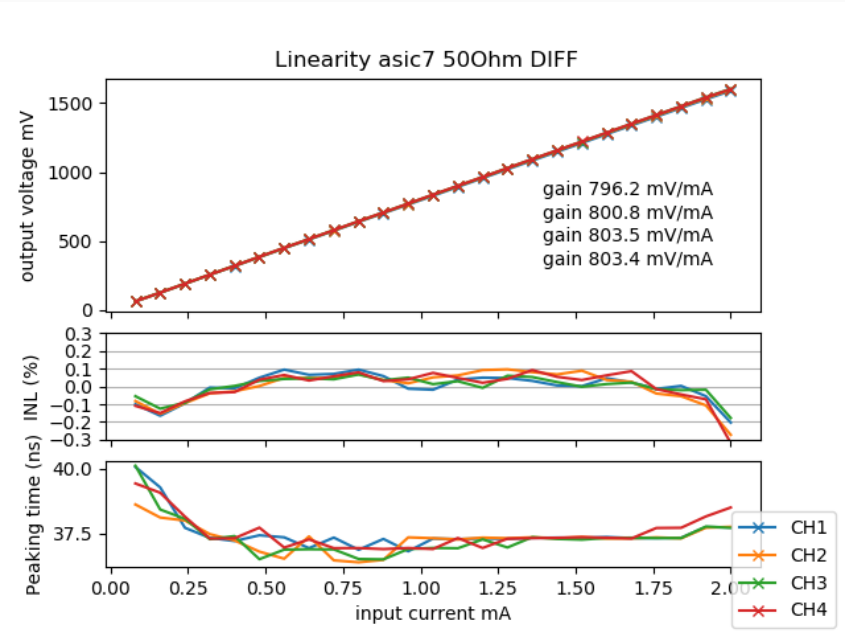
## High Gain

- INL ±0.1% vs requirement ±0.2%
- Peaking time stability: ∼ 1 ns

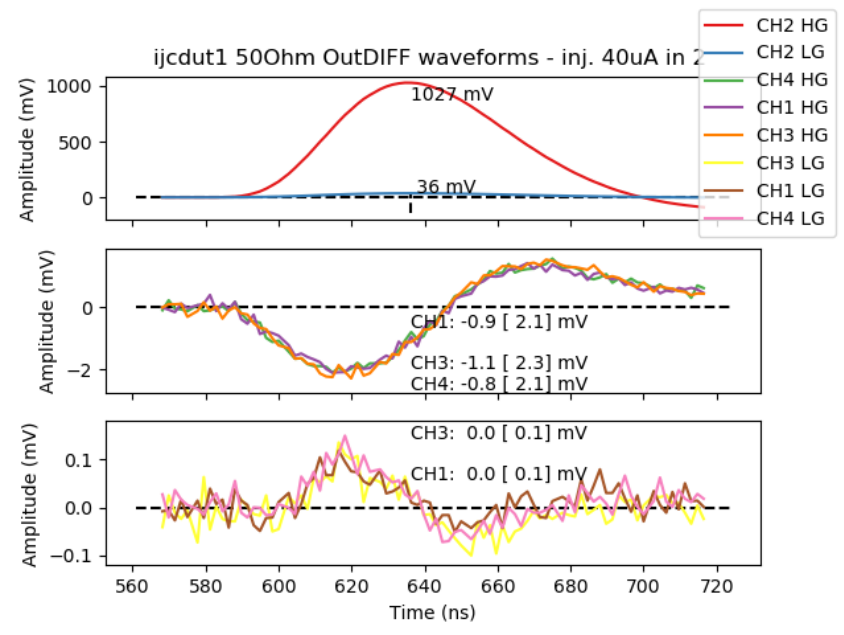


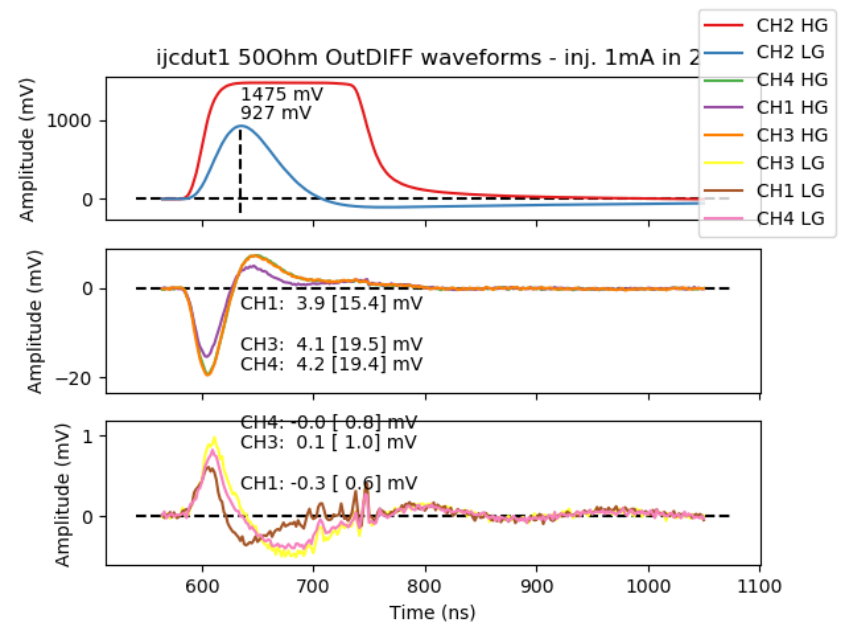

## Low Gain

- INL ±0.2% vs requirement ±0.5%
- Peaking time stability: ∼ 1 ns
- Gain ratio HG/LG: ∼ 35 vs requirement 23 ± 5



# 3.G.1-4 Cross-talk 50Ω




| inj CH2 | HG vs HG at peak | HG vs HG pk-to-pk | LG vs HG at peak | LG vs HG pk-to-pk | LG vs LG at peak | LG vs LG pk-to-pk |
|---|---|---|---|---|---|---|
| CH1 | 0.08% | 0.20% | 0.42% | 1.66% | 0.01% | 0.09% |
| CH3 | 0.11% | 0.22% | 0.44% | 2.10% | 0.01% | 0.10% |
| CH4 | 0.08% | 0.20% | 0.45% | 2.09% | 0.03% | 0.06% |

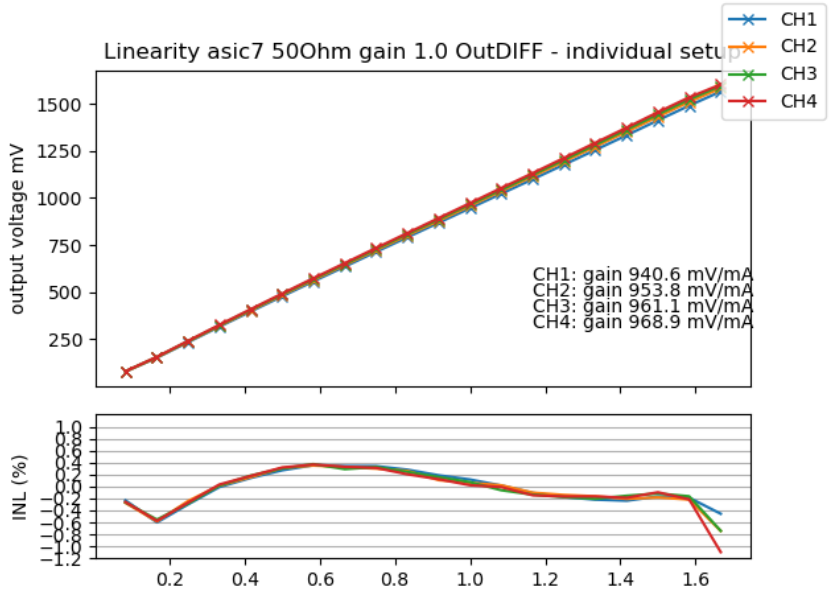
## Cross-talk

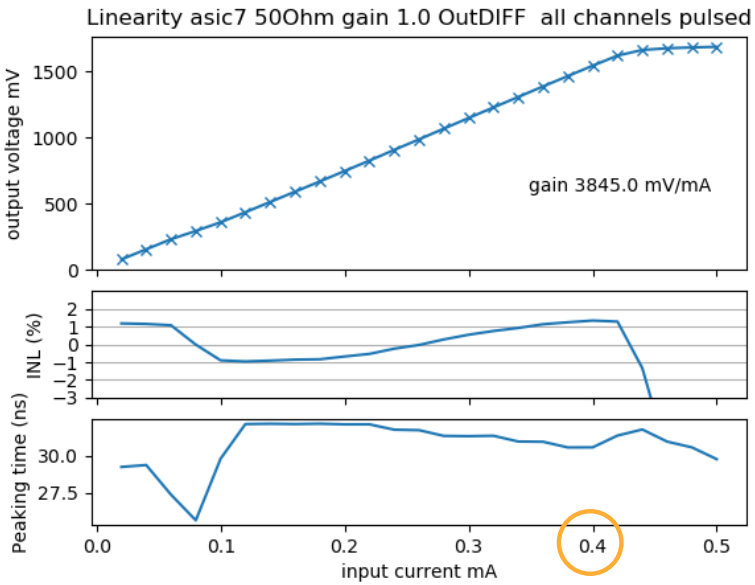
- Evaluated at peak of injected pulse
- All good vs requirement 0.5%
- Peak-to-peak cross-talk shown as well

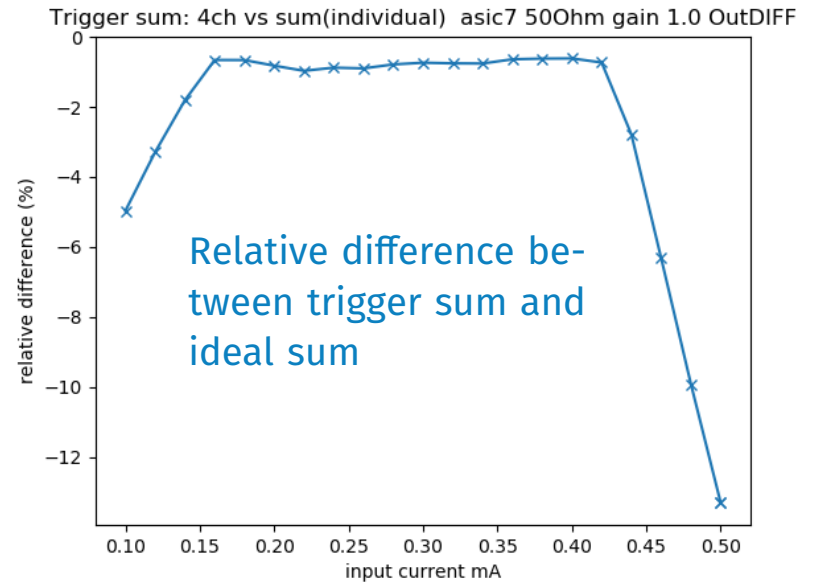
# 4.2-4 L0 Trigger Sum 50Ω

## Trigger sum

- LAUROC2 designed with gains x1 / x1.5 / x2.5 / x3.5 before requirements were fixed with x1 / x3
- Gain uniformity: $< 3\%$ vs requirement $< 5\%$
- INL $< \pm 2\%$
- Peaking time tuning and stability ok
- Shaper switches working ok



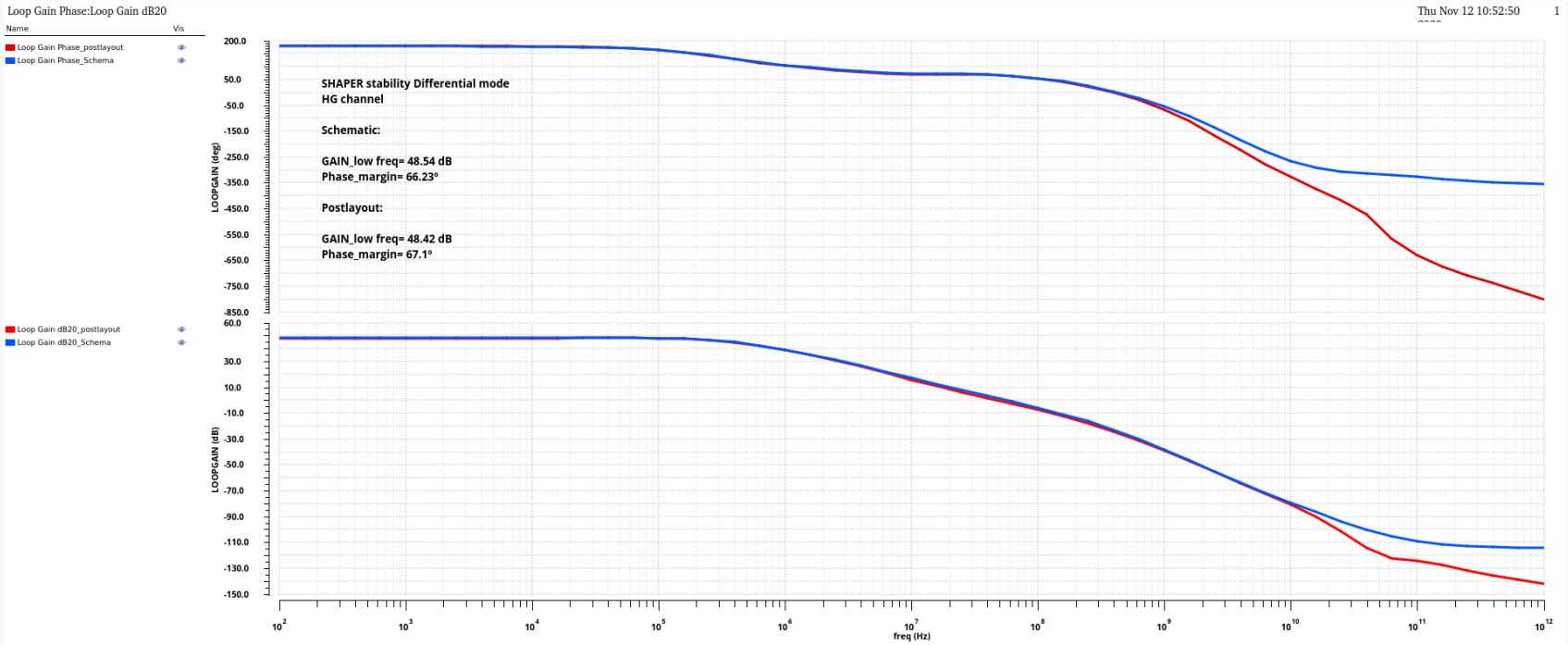



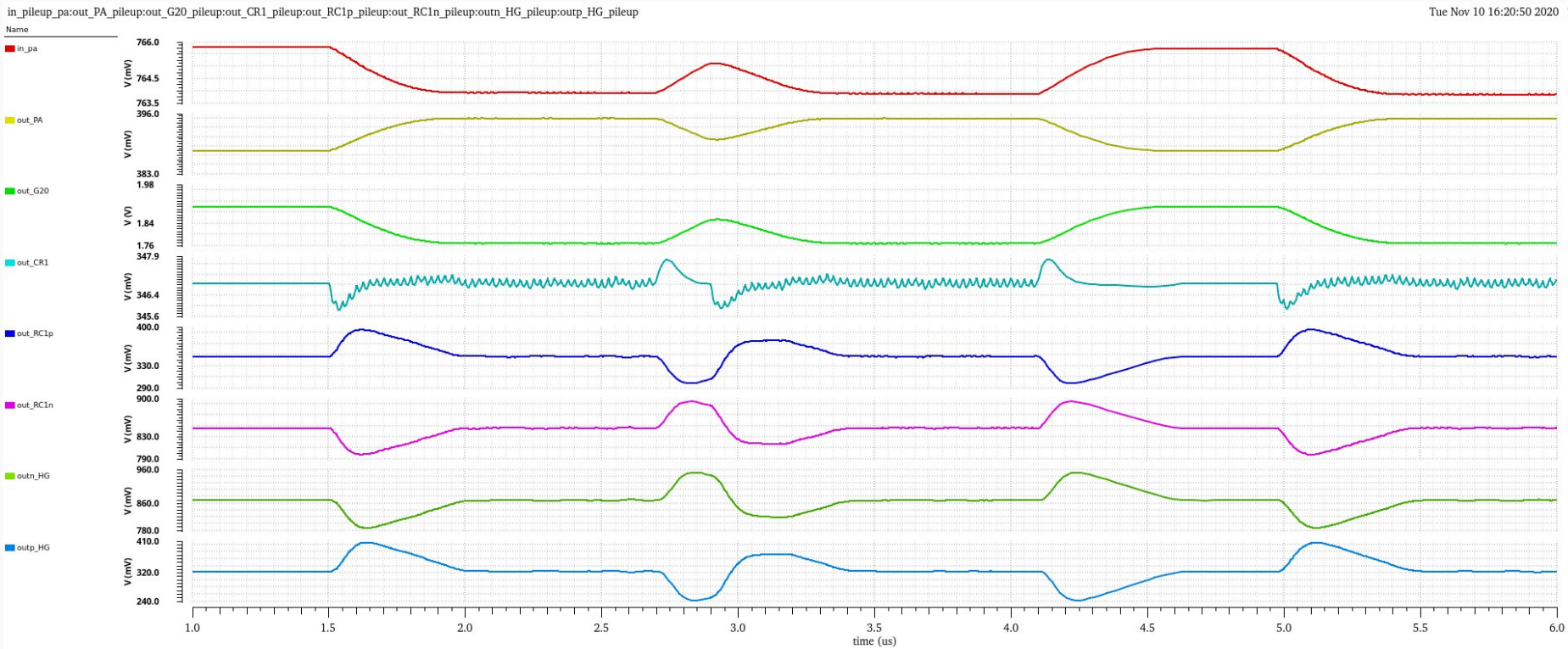

0.45 mA/channel $\Rightarrow$ 1.8 mA total

# 3.E.1 Phase Margin

- Good agreement schematic/postlayout
- Phase: $66.2^0$
- Gain: 48.4 dB

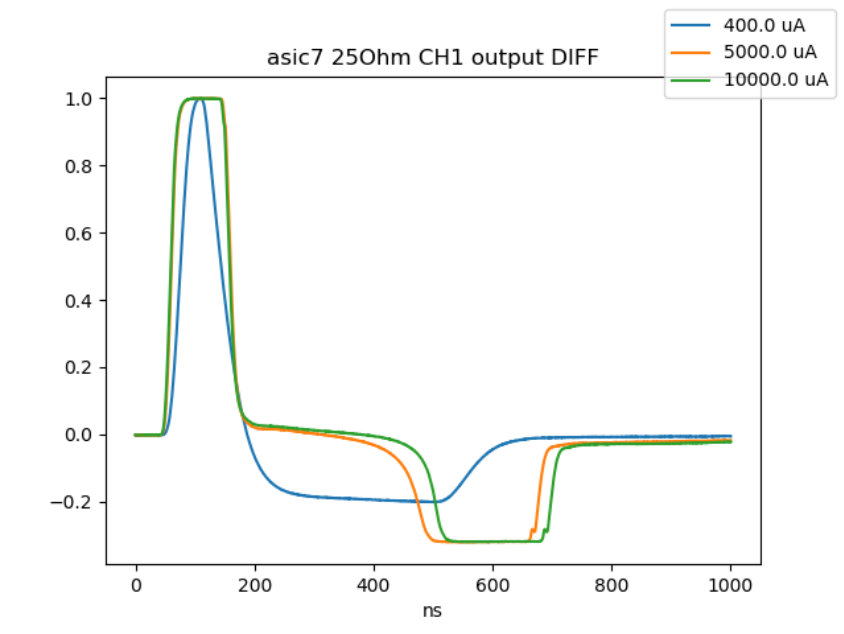


# 3.H.1 Behaviour Under High Pileup

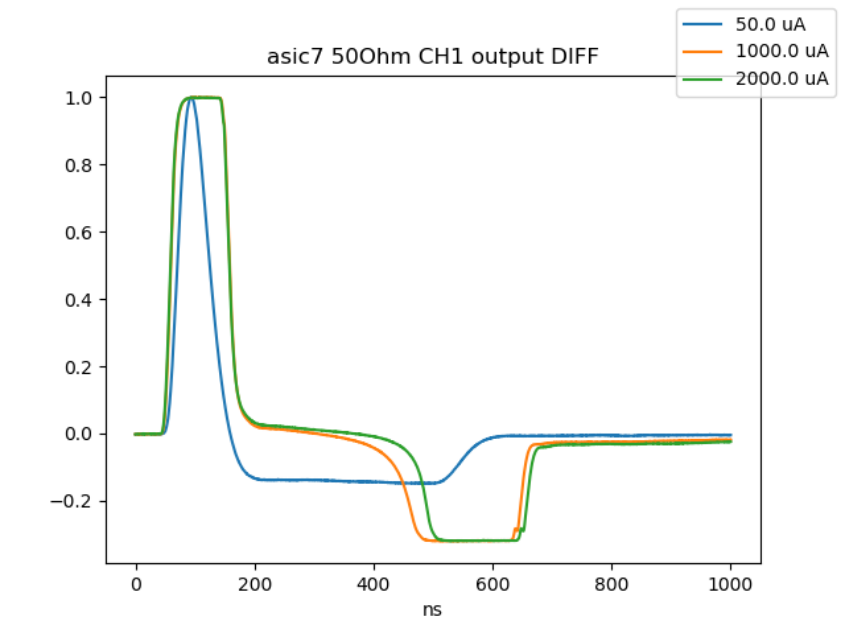



No internal saturation

# 3.B.1 Recovery Time




25 Ω




50 Ω