FEB2 block diagrams

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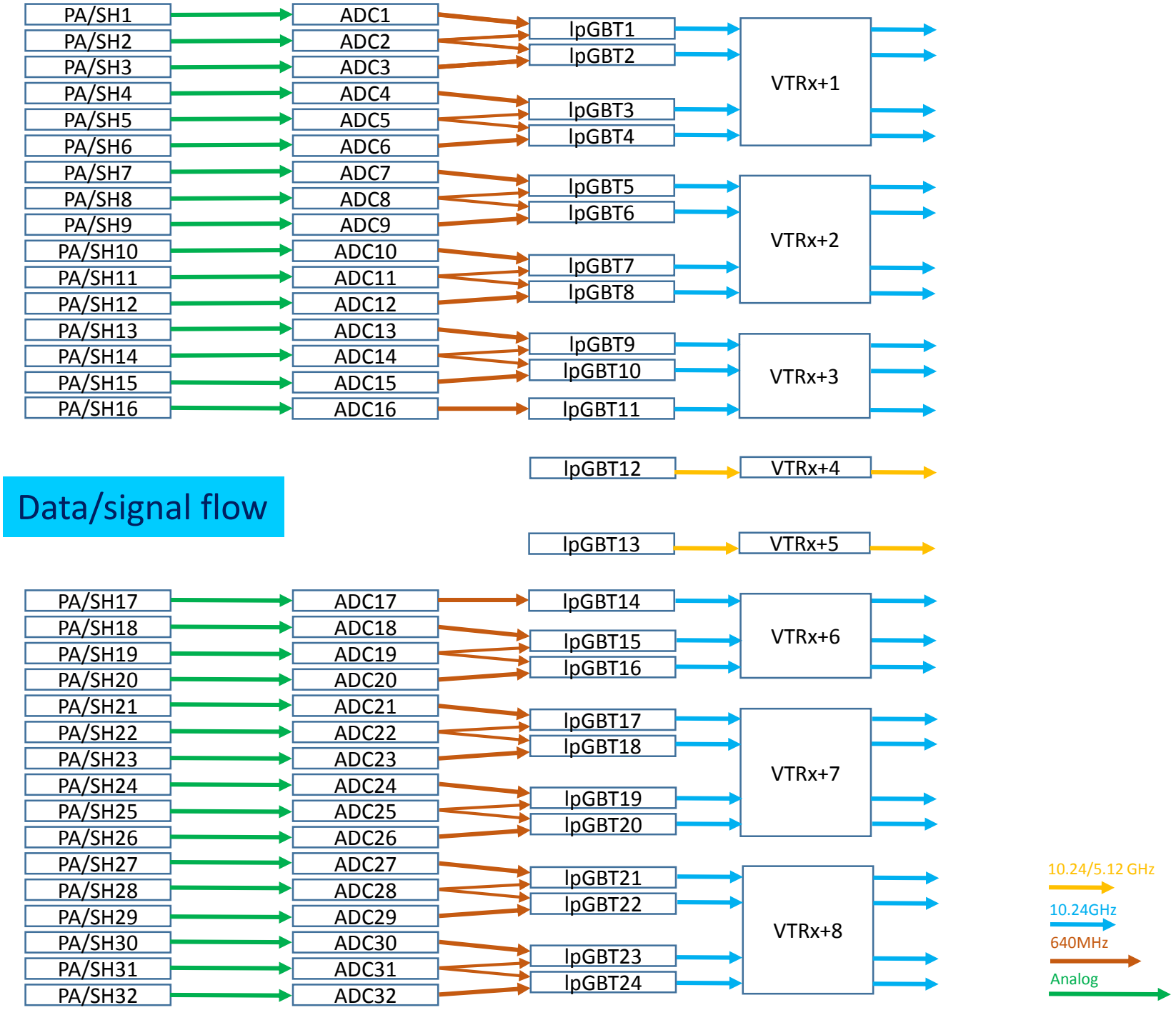
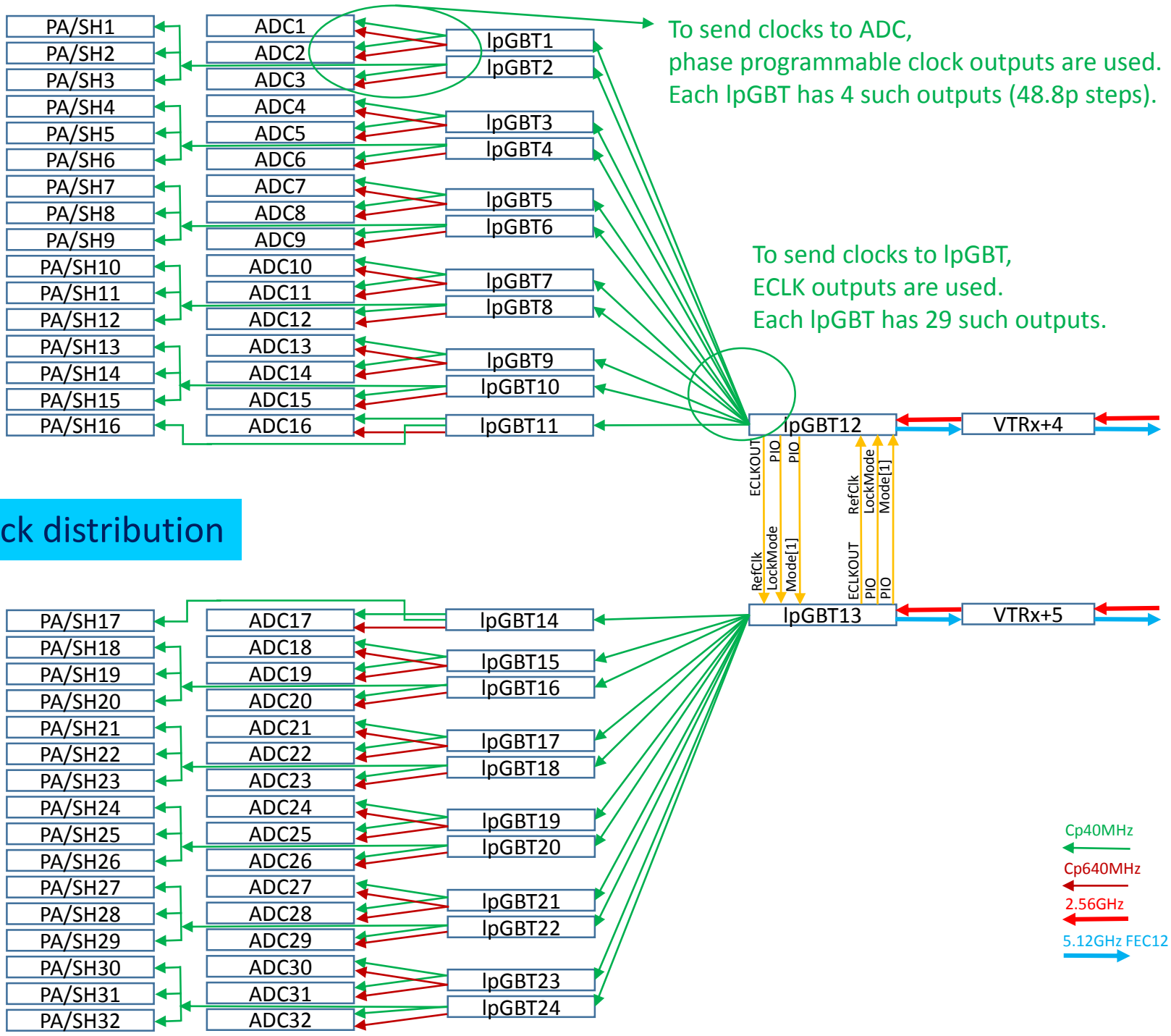
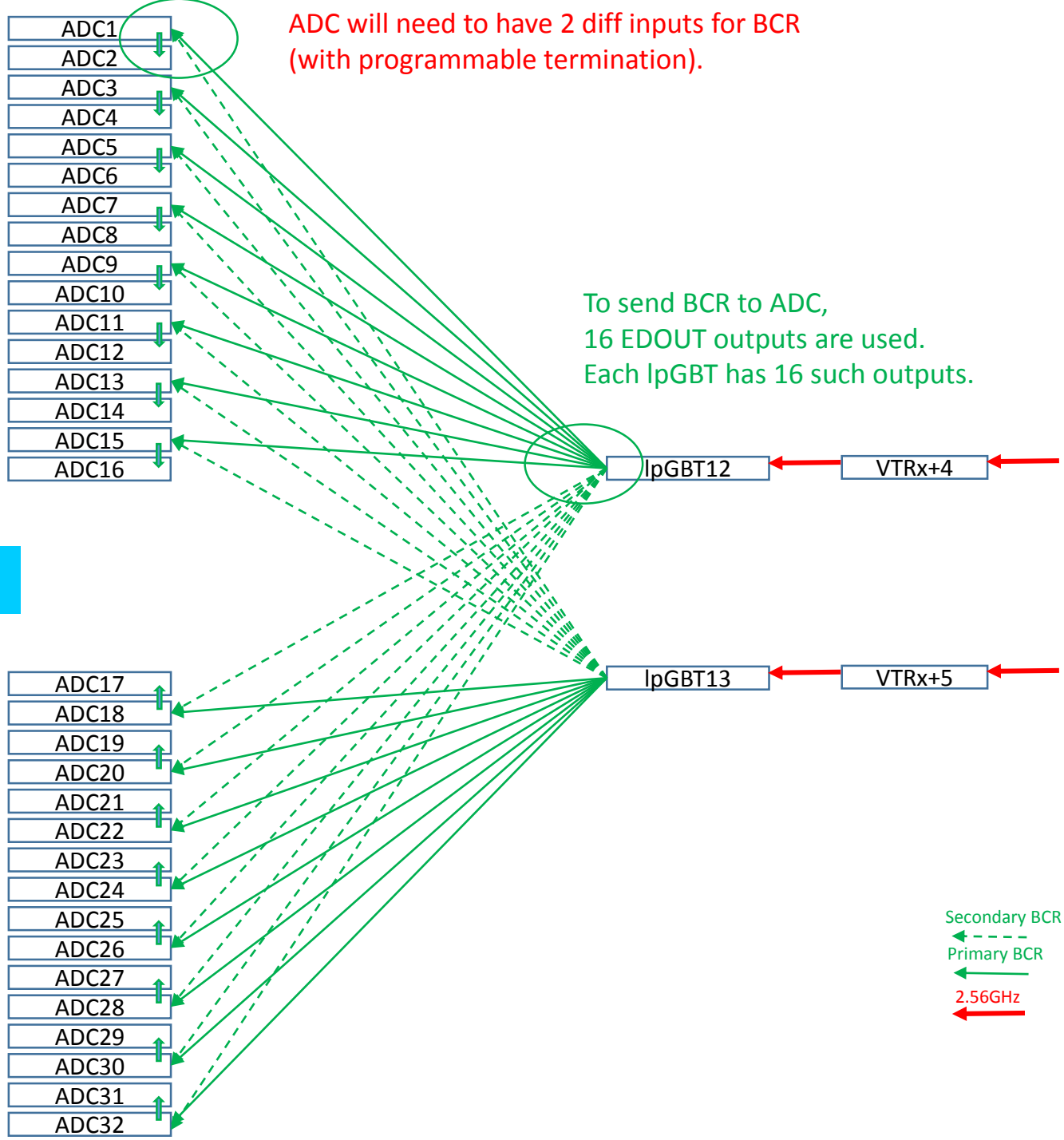
Data/signal flow



Clock distribution



BCR distribution



.BCR is generated for whole 25ns period

.BCR is strobed inside the ADC on leading edge of clk40 and BC is reset the next 25ns period

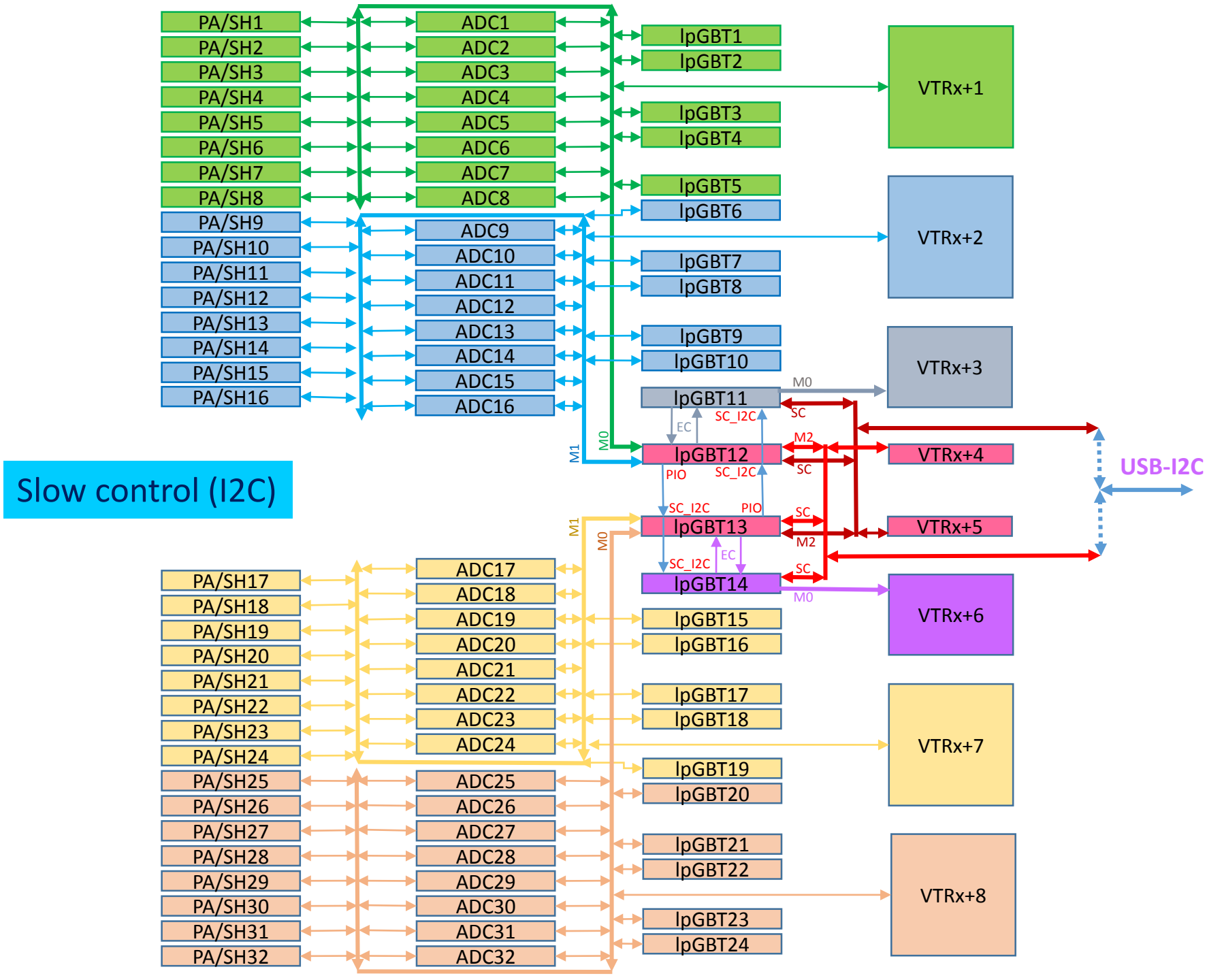
.3 BCR phases are possible with step of 12.5ns

.ADC will form a shift register containing data LpGBT clk40 during the active BCR

.This information will be available to the user to adjust the phase of the BCR for each data LpGBT

BCR hardware inside the ADC

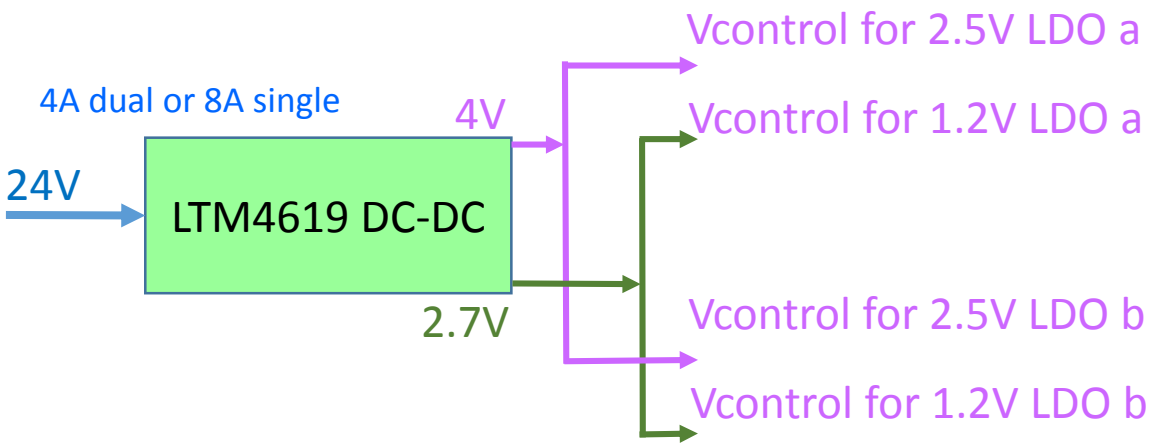
```
module BC_logic
   (input              resetB,
//clocks
    input              dL_clk40,       //40MHz clock  from local data LpGBT
    input              dL_clk640,      //640MHz clock from local data LpGBT
//Bunch crossing reset
    input              BCR,            //BCR form control LpGBT
//output registers
    output reg [15:0] BCR_cp40_reg ); //data LpGBT clk40 strobed with dL_clk640
                                      //during BCR
//registers
reg        BCR_strobed, dL_clk40_del1;

//BCR strobed with data LpGBT clk640MHz
always @(posedge dL_clk640)
  begin
   BCR_strobed <= BCR;
  end
//delay the clk40 by 1 640MHz tick  of the data LpGBT
always @(posedge dL_clk640)
  begin
   dL_clk40_del1 <= dL_clk40;
  end
//form the shift register containing data LpGBT clk40
//during the active BCR
always @(posedge dL_clk640 or negedge resetB)
  begin
   if (resetB==1'b0)     BCR_cp40_reg <= 16'b0000000000000000;
   else if (BCR_strobed) BCR_cp40_reg <= {BCR_cp40_reg[14:0], dL_clk40_del1};
  end

endmodule
```

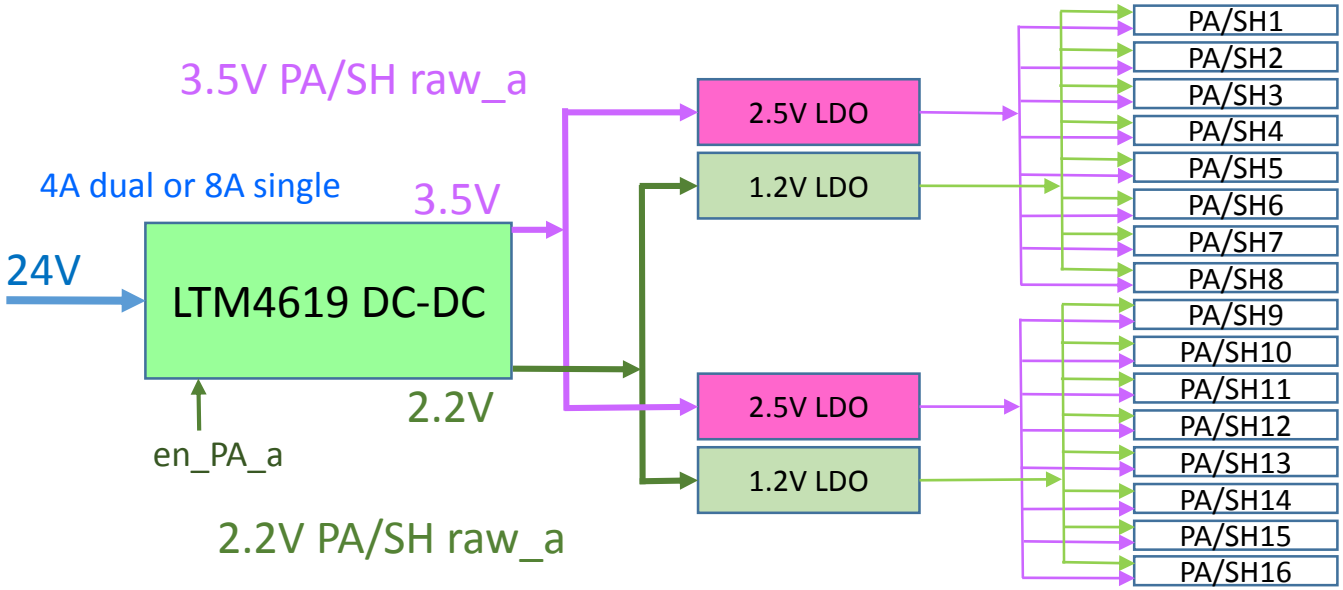

Slow control (I2C)
PA/SH1
PA/SH2
PA/SH3
PA/SH4
PA/SH5
PA/SH6
PA/SH7
PA/SH8
PA/SH9
PA/SH10
PA/SH11
PA/SH12
PA/SH13
PA/SH14
PA/SH15
PA/SH16
PA/SH17
PA/SH18
PA/SH19
PA/SH20
PA/SH21
PA/SH22
PA/SH23
PA/SH24
PA/SH25
PA/SH26
PA/SH27
PA/SH28
PA/SH29
PA/SH30
PA/SH31
PA/SH32
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
ADC9
ADC10
ADC11
ADC12
ADC13
ADC14
ADC15
ADC16
ADC17
ADC18
ADC19
ADC20
ADC21
ADC22
ADC23
ADC24
ADC25
ADC26
ADC27
ADC28
ADC29
ADC30
ADC31
ADC32
lpGBT1
lpGBT2
lpGBT3
lpGBT4
lpGBT5
lpGBT6
lpGBT7
lpGBT8
lpGBT9
lpGBT10
lpGBT11
lpGBT12
lpGBT13
lpGBT14
lpGBT15
lpGBT16
lpGBT17
lpGBT18
lpGBT19
lpGBT20
lpGBT21
lpGBT22
lpGBT23
lpGBT24
VTRx+1
VTRx+2
VTRx+3
VTRx+4
VTRx+5
VTRx+6
VTRx+7
VTRx+8
USB-I2C
M0
M1
M2
EC
SC
SC_I2C
PIO

PA/SH	I2C address	ADC	I2C address	VTRx+	I2C address	LpGBT	I2C address
1	0001xxx	1	10’b000_1000000	1	1010000	1	1110001
2	0010xxx	2	10’b001_0000000	2	1010000	2	1110010
3	0011xxx	3	10'b001_1000000	3	1010000	3	1110011
4	0100xxx	4	10'b010_0000000	4	1010000	4	1110100
5	0101xxx	5	10'b010_1000000	5	1010000	5	1110101
6	0110xxx	6	10'b011_0000000	6	1010000	6	1110001
7	0111xxx	7	10'b011_1000000	7	1010000	7	1110010
8	1000xxx	8	10'b100_0000000	8	1010000	8	1110011
9	0001xxx	9	10'b000_1000000			9	1110100
10	0010xxx	10	10'b001_0000000			10	1110101
11	0011xxx	11	10'b001_1000000			11	1110001
12	0100xxx	12	10'b010_0000000			12	1110010
13	0101xxx	13	10'b010_1000000			13	1110011
14	0110xxx	14	10'b011_0000000			14	1110100
15	0111xxx	15	10'b011_1000000			15	1110001
16	1000xxx	16	10'b100_0000000			16	1110010
17	0001xxx	17	10'b000_1000000			17	1110011
18	0010xxx	18	10'b001_0000000			18	1110100
19	0011xxx	19	10'b001_1000000			19	1110101
20	0100xxx	20	10'b010_0000000			20	1110001
21	0101xxx	21	10'b010_1000000			21	1110010
22	0110xxx	22	10'b011_0000000			22	1110011
23	0111xxx	23	10'b011_1000000			23	1110100
24	1000xxx	24	10'b100_0000000			24	1110101
25	0001xxx	25	10'b000_1000000				
26	0010xxx	26	10'b001_0000000				
27	0011xxx	27	10'b001_1000000				
28	0100xxx	28	10'b010_0000000				
29	0101xxx	29	10'b010_1000000				
30	0110xxx	30	10'b011_0000000				
31	0111xxx	31	10'b011_1000000				
32	1000xxx	32	10'b100_0000000				

I2C address assignment

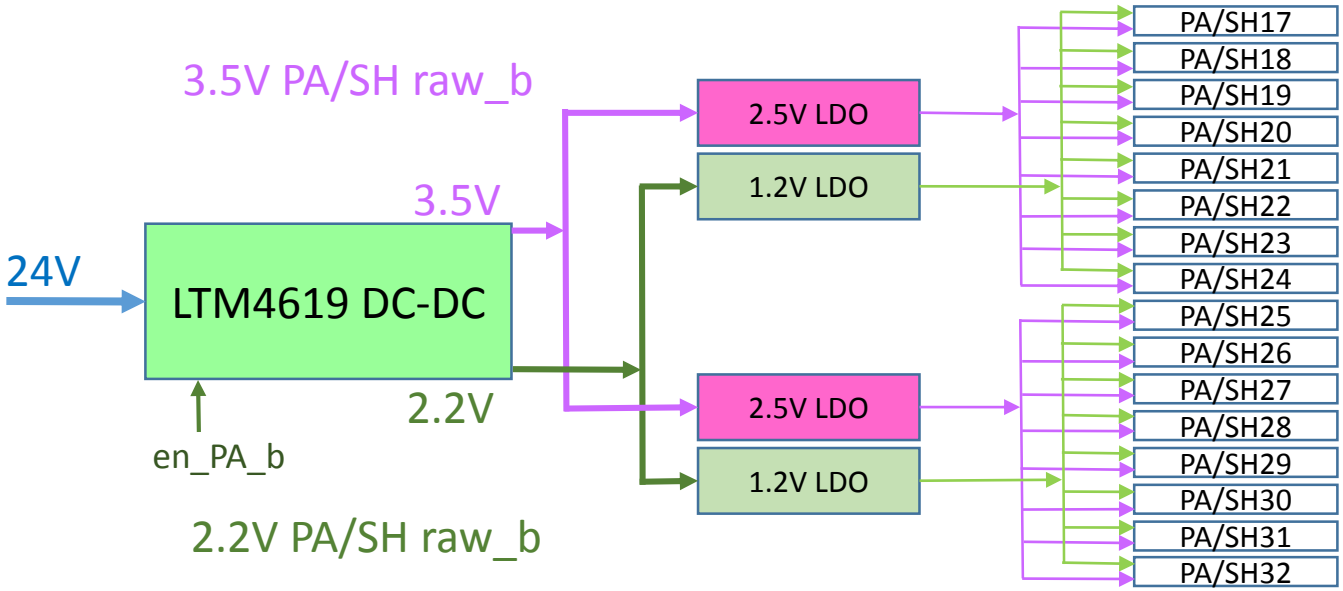
Option for LT3080 LDO Control Voltages



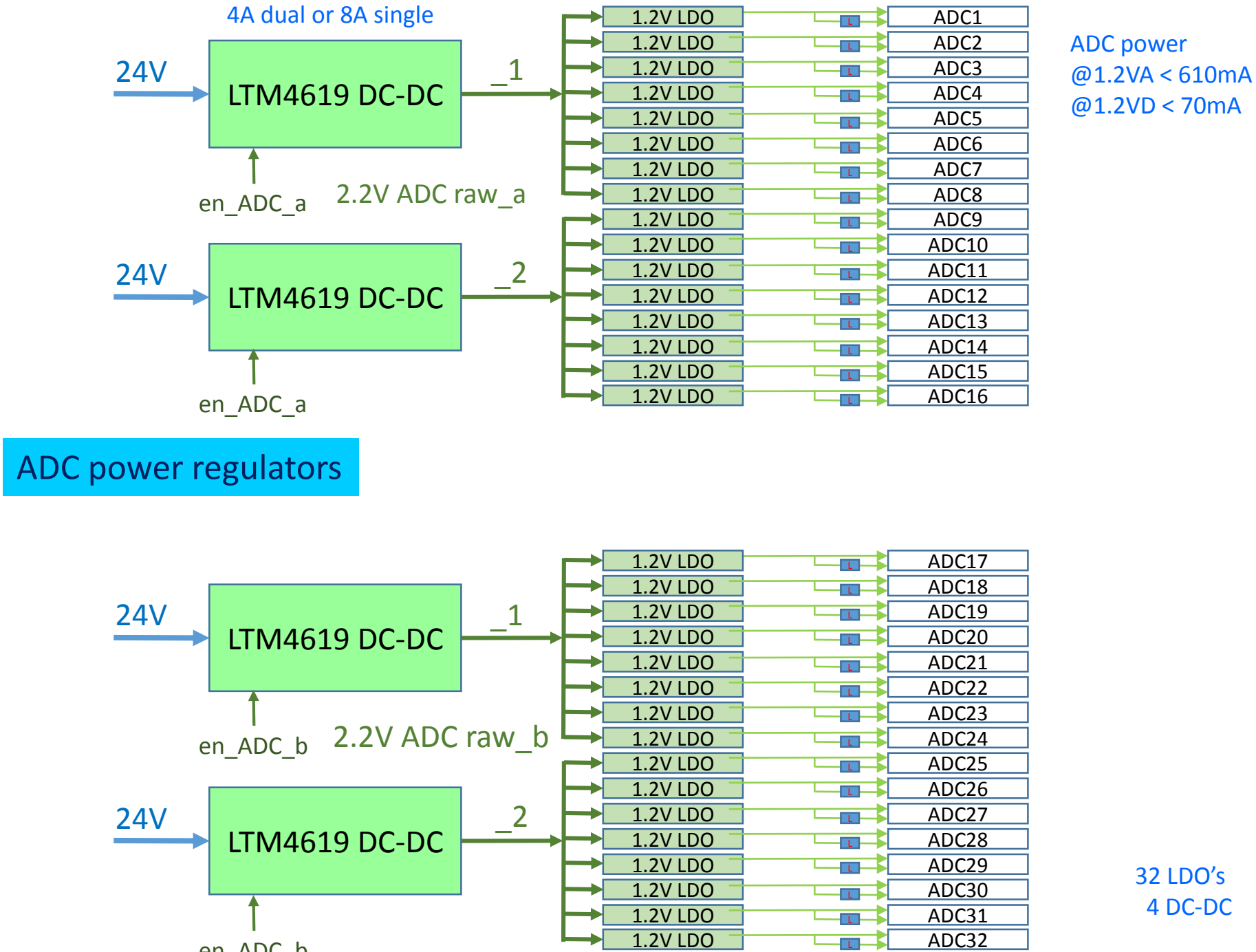


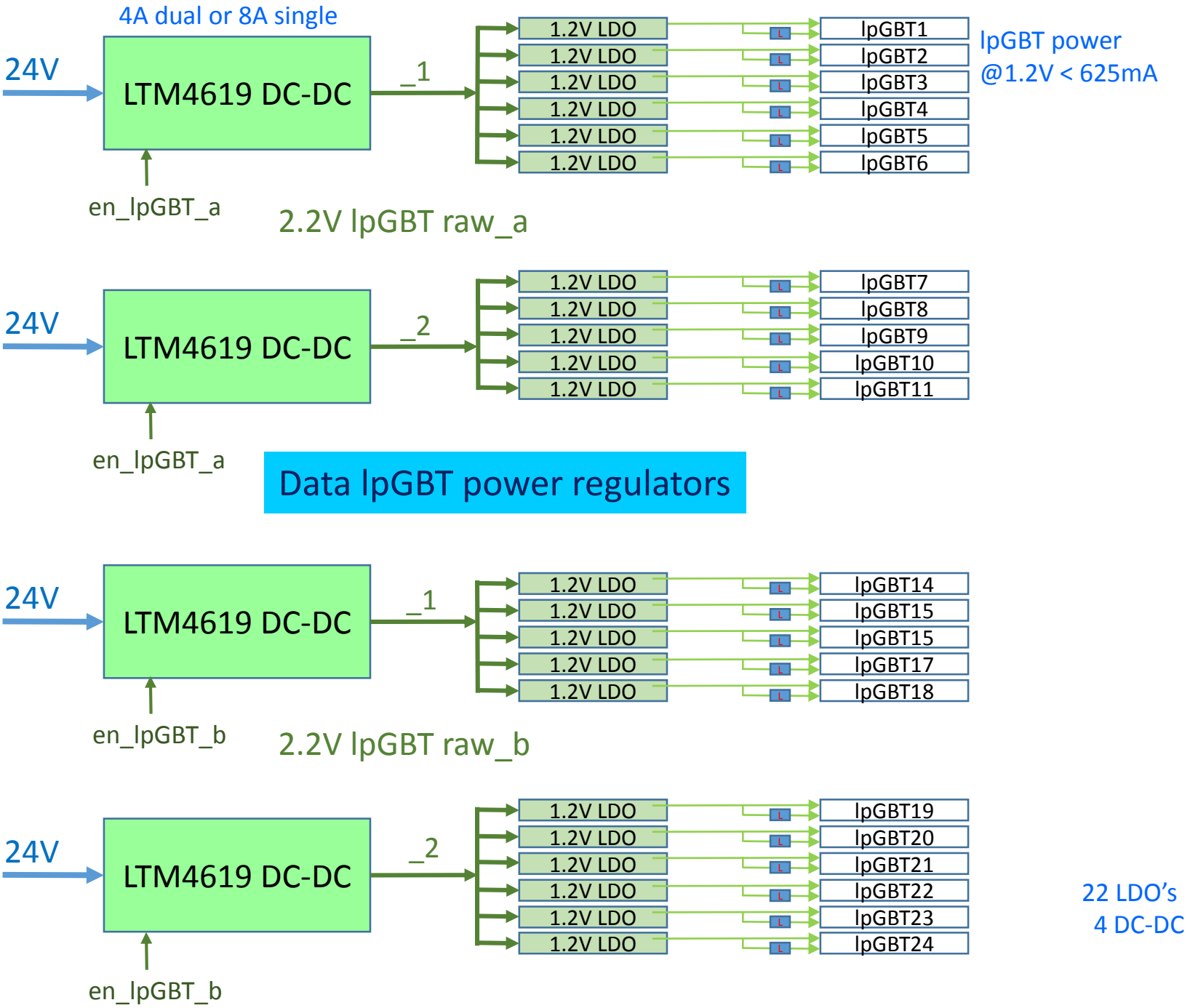
PA power
@2.5V < 100mA
@1.2V < 100mA

PA/SH power regulators

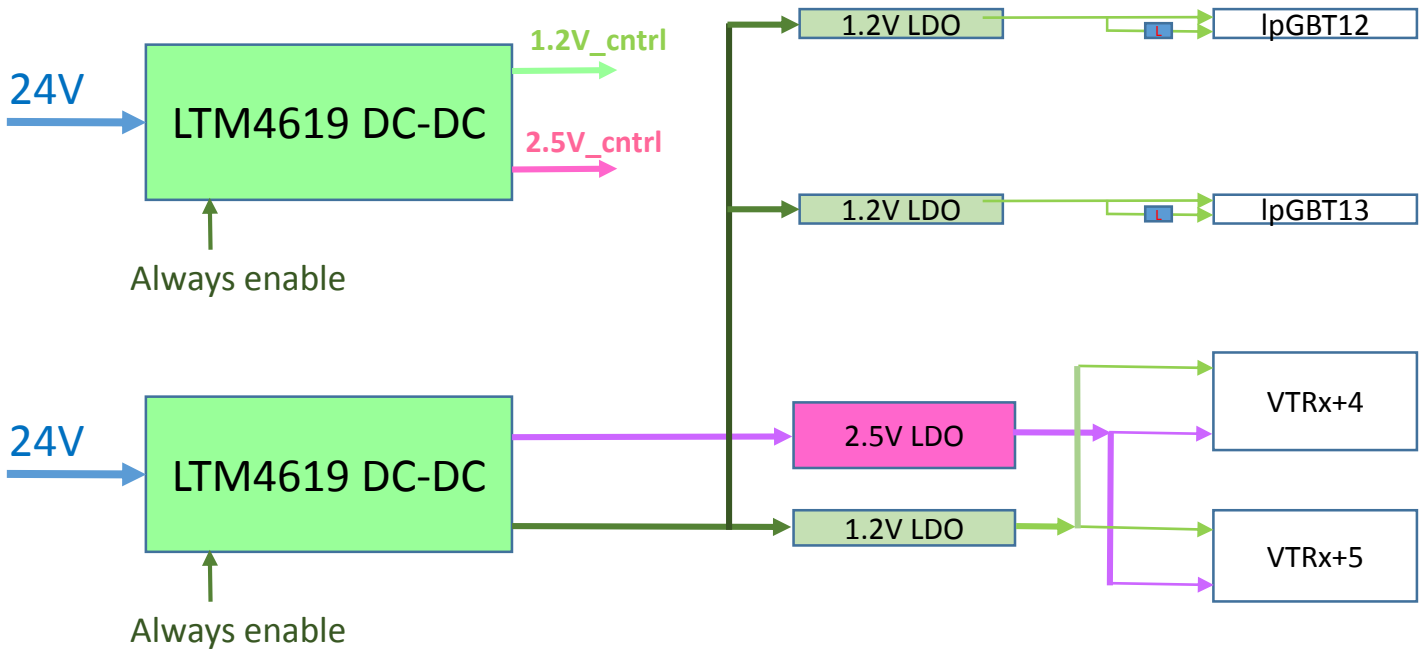


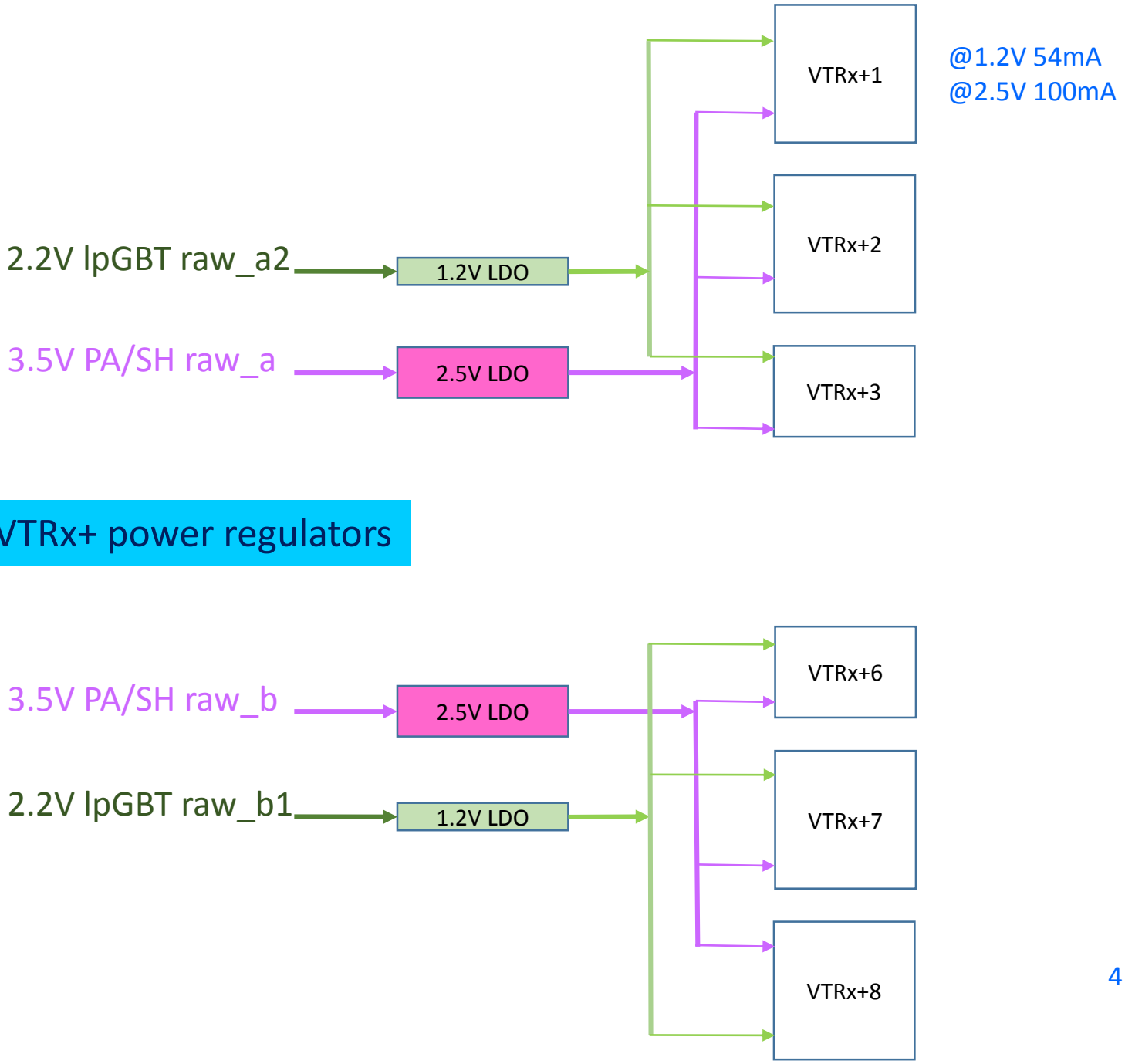
8 LDO's
2 DC-DC


4A dual or 8A single
24V
LTM4619 DC-DC
_1
en_ADC_a
2.2V ADC raw_a
24V
LTM4619 DC-DC
_2
en_ADC_a
1.2V LDO
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
ADC8
ADC9
ADC10
ADC11
ADC12
ADC13
ADC14
ADC15
ADC16
ADC power
@1.2VA < 610mA
@1.2VD < 70mA
ADC power regulators
24V
LTM4619 DC-DC
_1
en_ADC_b
2.2V ADC raw_b
24V
LTM4619 DC-DC
_2
en_ADC_b
1.2V LDO
ADC17
ADC18
ADC19
ADC20
ADC21
ADC22
ADC23
ADC24
ADC25
ADC26
ADC27
ADC28
ADC29
ADC30
ADC31
ADC32
32 LDO's
4 DC-DC


4A dual or 8A single
24V
LTM4619 DC-DC
_1
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
lpGBT1
lpGBT2
lpGBT3
lpGBT4
lpGBT5
lpGBT6
lpGBT power
@1.2V < 625mA
en_lpGBT_a
2.2V lpGBT raw_a
24V
LTM4619 DC-DC
_2
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
lpGBT7
lpGBT8
lpGBT9
lpGBT10
lpGBT11
en_lpGBT_a
Data lpGBT power regulators
24V
LTM4619 DC-DC
_1
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
lpGBT14
lpGBT15
lpGBT15
lpGBT17
lpGBT18
en_lpGBT_b
2.2V lpGBT raw_b
24V
LTM4619 DC-DC
_2
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
1.2V LDO
lpGBT19
lpGBT20
lpGBT21
lpGBT22
lpGBT23
lpGBT24
en_lpGBT_b
22 LDO's
4 DC-DC

Control lpGBT and VTRx+ power regulators



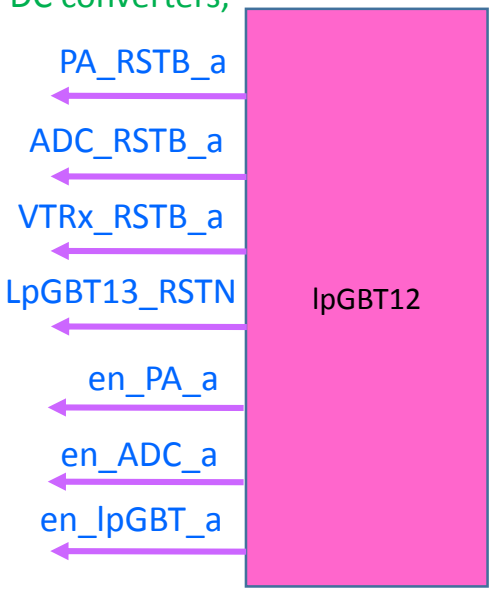


VTRx+ power regulators

Slow control & monitoring overview

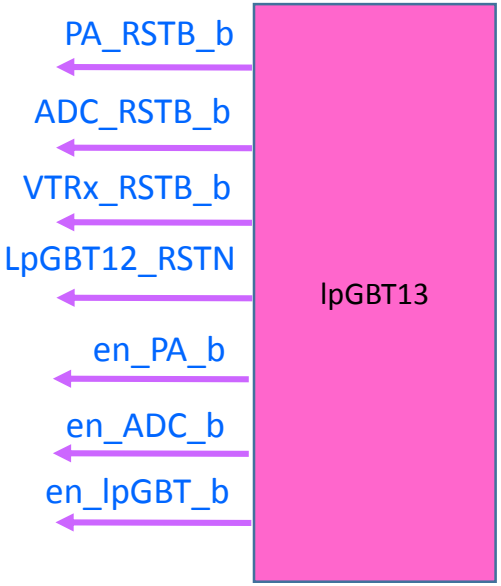
LpGBT9	PA9-16_+2.5V	PA9-16_+1.2V						
LpGBT10	ADC13_VDD	ADC14_VDD	ADC15_VDD	VTRX3_1P2				
LpGBT11	ADC16_VDD	REF_VDD	VTRX3_TEMP	VTRX3_RSSI	VTRX4_1P2			
LpGBT12	VTRX4_TEMP	V2P5_MON_A	VTRX4_RSSI	TEMP_T1	TEMP_T2	TEMP_T3	TEMP_B1	TEMP_B2
LpGBT13	VTRX5_TEMP	V2P5_MON_B	VTRX5_RSSI	TEMP_T4	TEMP_T5	TEMP_T6	TEMP_B3	TEMP_B4
LpGBT14	ADC17_VDD	VTRX5_1P2	VTRX6_1P2					
LpGBT15	PA17-24_+2.5V	PA17-24_+1.2V	VTRX6_TEMP	VTRX6_RSSI				
LpGBT16	ADC18_VDD	ADC19_VDD	ADC20_VDD	MAIN_PS				

To generate resets and enable DC-DC converters,
PIO pins are used.
Each lpGBT has 16 such outputs.



Power control		
signal	LpGBT#	GPIO pin #
DCDC_EN_PA_A	12	2
DCDC_EN_LPGBT_B	12	4
DCDC_EN_ADC_A	12	11
DCDC_EN_PA_B	13	2
DCDC_EN_ADC_B	13	3
DCDC_EN_LPGBT_A	13	4

Slow control

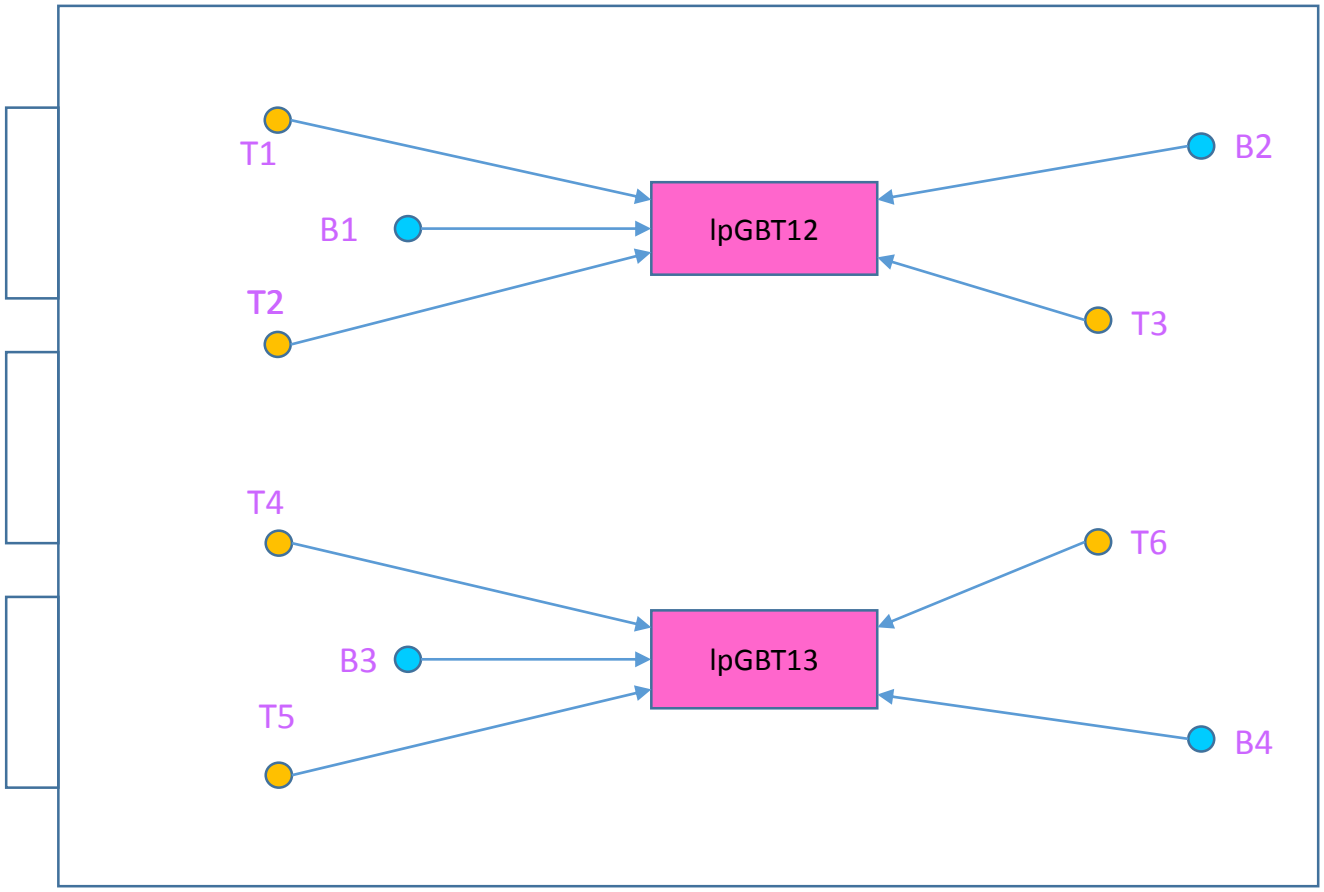


RESET control		
signal	LpGBT#	GPIO pin #
PA_RSTB_A	12	0
ADC_RSTB_A	12	1
VTRX_RSTB_A	12	3
LPGBT13_RSTN	12	10
PA_RSTB_B	13	0
ADC_RSTB_B	13	1
VTRX_RSTB_B	13	5
LPGBT12_RSTN	13	10

Tx PT1000 probe on PCB top side
Bx PT1000 probe on PCB bottom side

Temperature monitoring

Temperature monitoring		
Temperature	LpGBT#	ADC input #
T1	12	5
T2	12	2
T3	12	1
T4	13	5
T5	13	6
T6	13	1
B1	12	6
B2	12	7
B3	13	2
B4	13	7
VTRx+3	11	2
VTRx+4	12	0
VTRx+5	13	1
VTRx+6	15	2



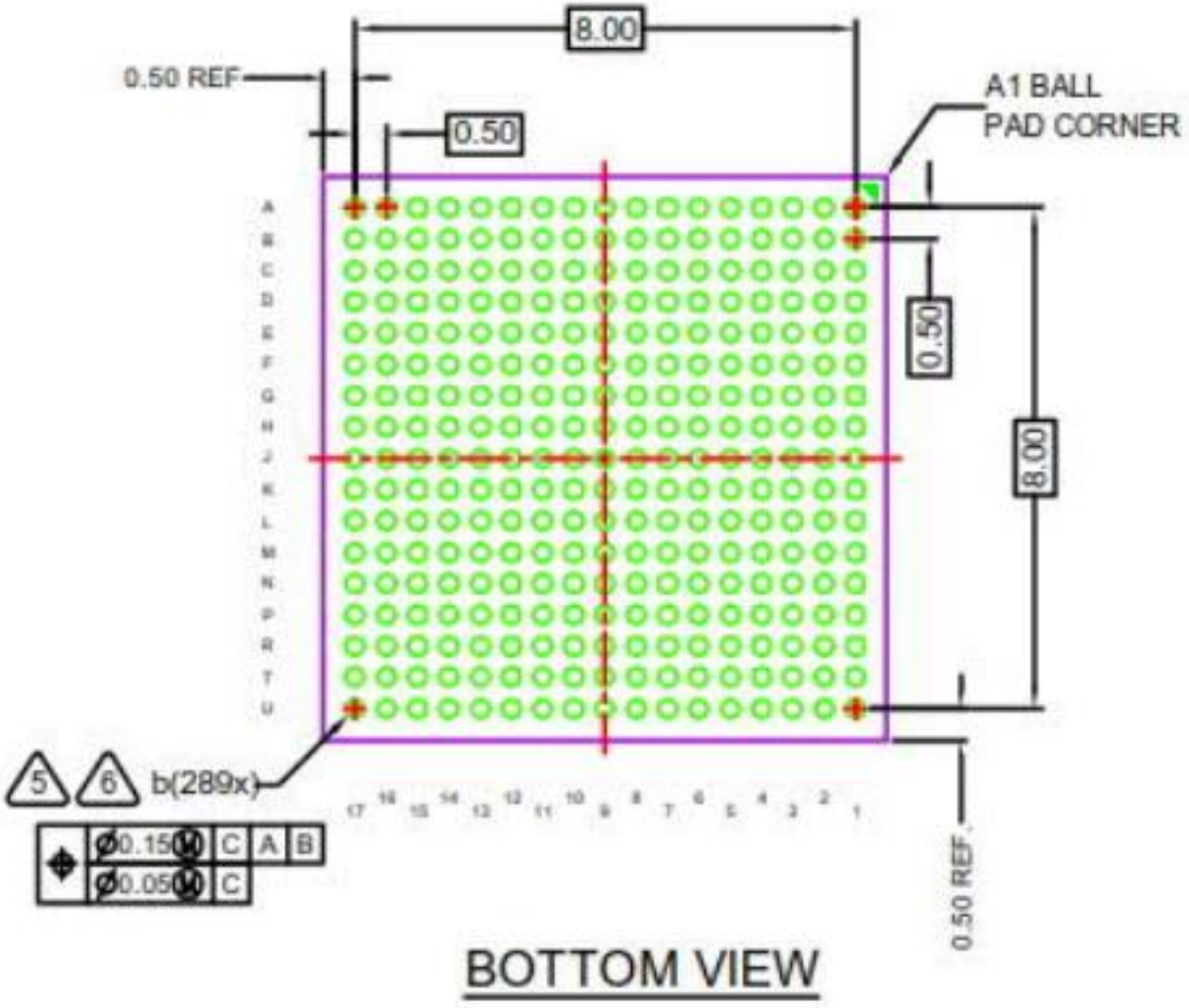
Power monitoring and control

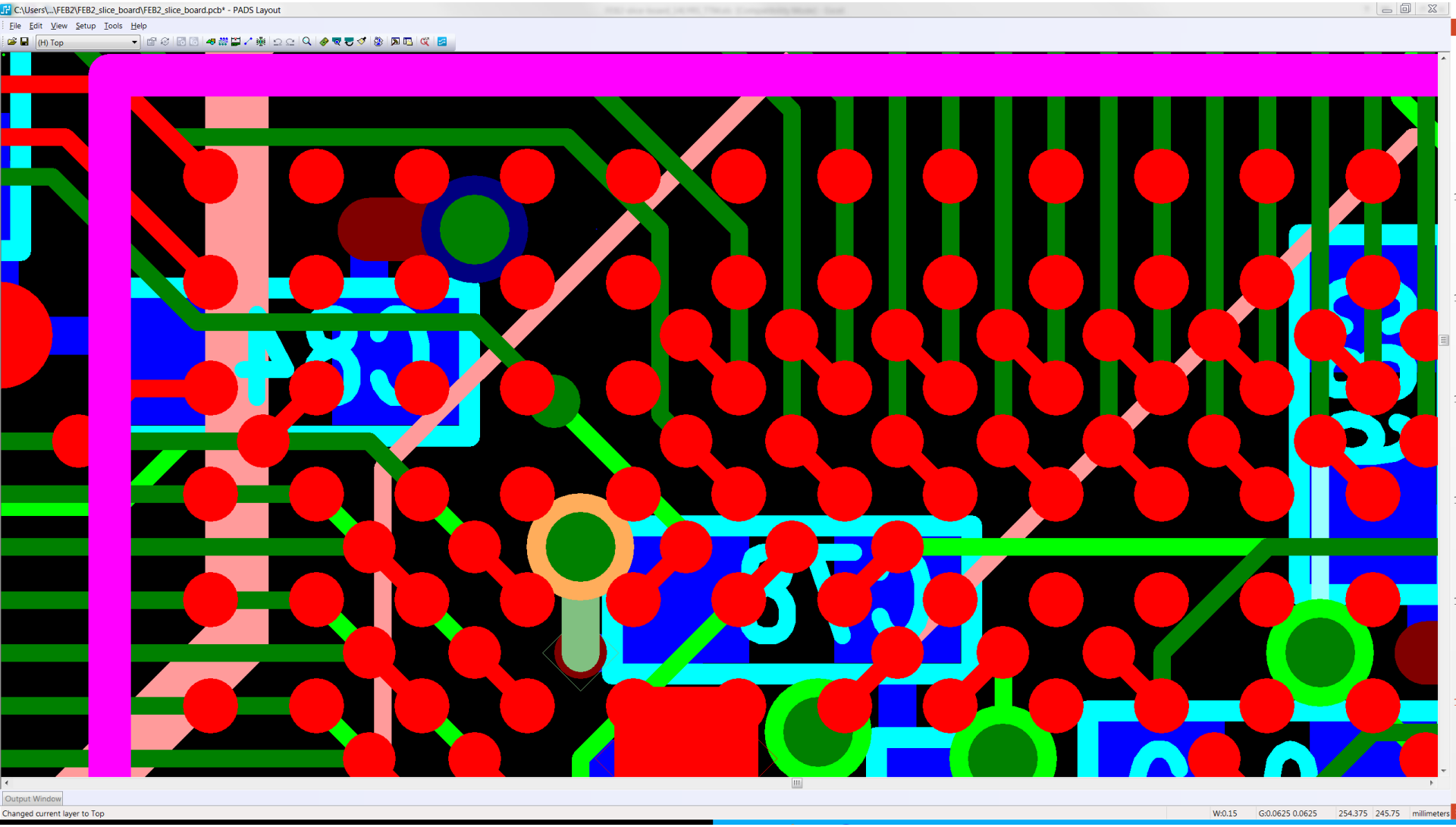
LDO/Power monitoring		
Voltage	LpGBT#	ADC input #
PA9-16_+2.5V	9	5
PA9-16_+1.2V	9	2
ADC13_VDD	10	0
ADC14_VDD	10	1
ADC15_VDD	10	2
VTRX3_1P2	10	6
ADC16_VDD	11	6
REF_VDD	11	7
VTRX4_1P2	11	2
VTRX3_RSSI	11	7
V2P5_MON_A	12	3
VTRX4_RSSI	12	4
V2P5_MON_B	13	3
VTRX5_RSSI	13	4
ADC17_VDD	14	0
VTRX6_1P2	14	6
VTRX5_1P2	14	7
PA17-24_+2.5V	15	0
PA17-24_+1.2V	15	1
VTRX6_RSSI	15	3
ADC18_VDD	16	0
ADC19_VDD	16	1
ADC20_VDD	16	2
MAIN_PS	16	6

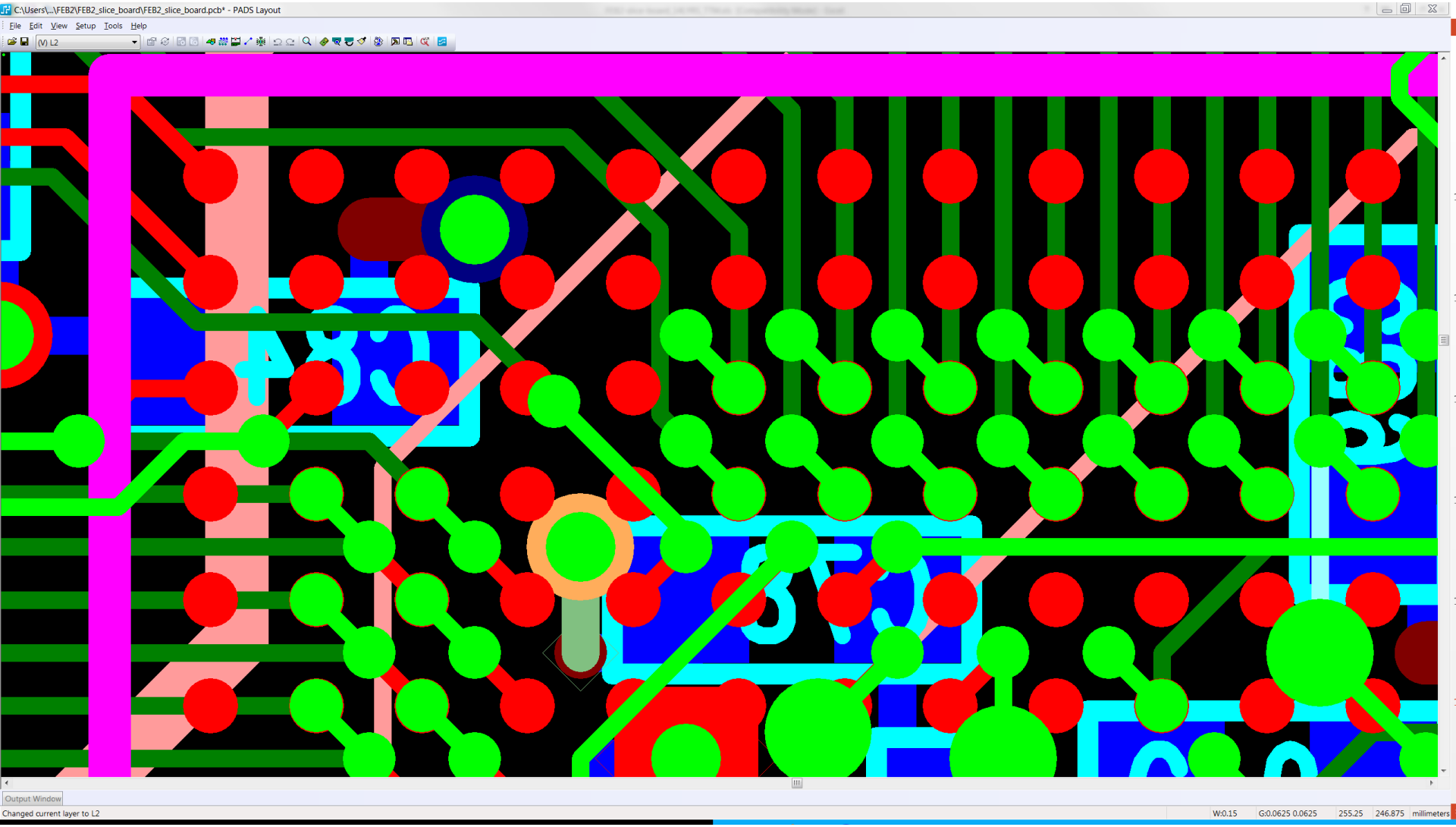
Digital signal status bits		
signal	LpGBT#	GPIO pin #
PA14_I2C_ERROR	9	0
PA13_I2C_ERROR	9	15
PA15_I2C_ERROR	10	15
PA16_I2C_ERROR	11	15
PA17_I2C_ERROR	14	15
PA19_I2C_ERROR	15	0
PA18_I2C_ERROR	15	15
PA20_I2C_ERROR	16	15

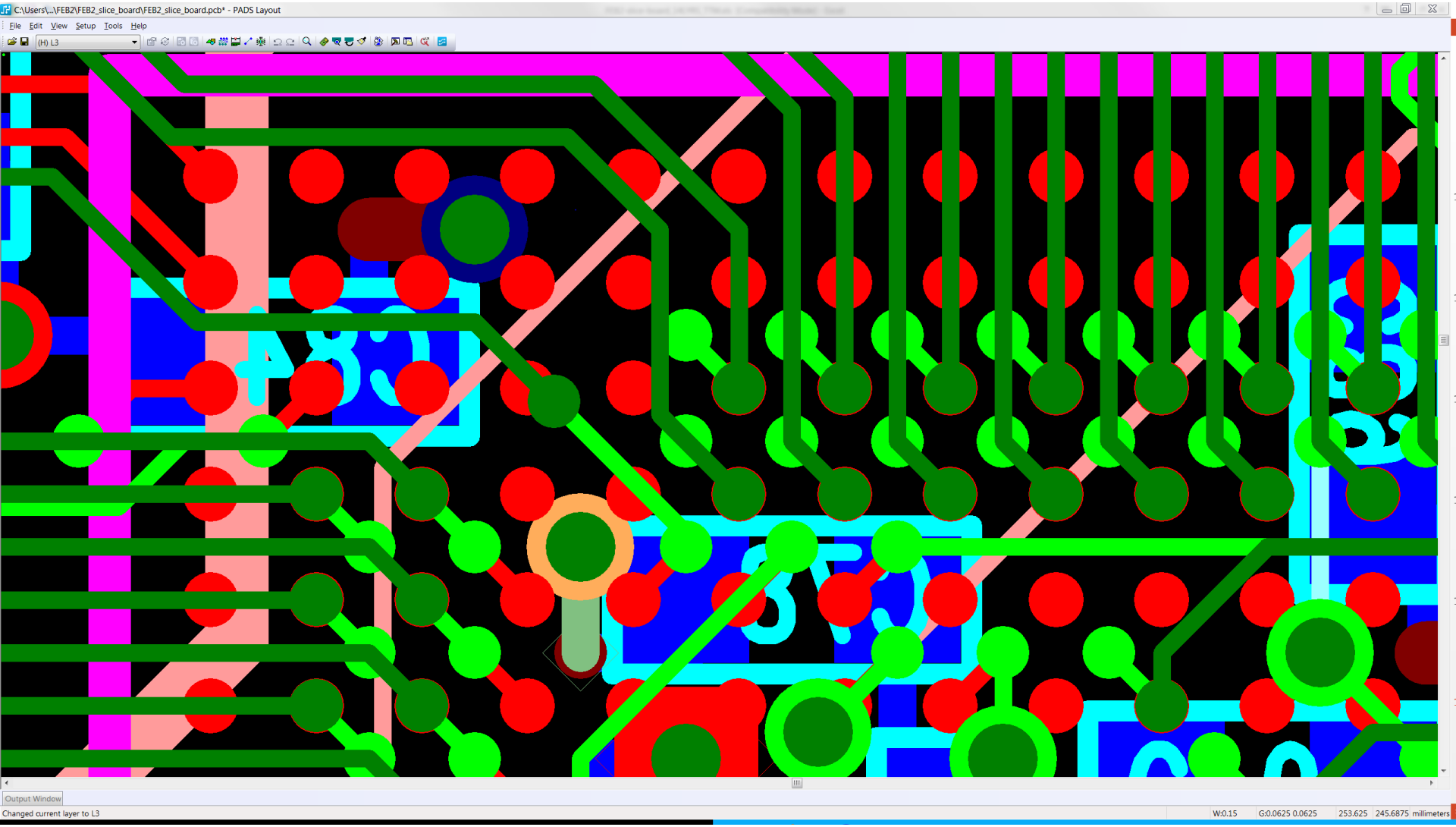
LpGBT12/13 cross control		
signal	LpGBT#	GPIO pin #
LPGBT13_MOD1	12	8
LPGBT13_LOCKMODE	12	12
LPGBT13_SC_I2C	12	14
LPGBT12_MOD1	13	8
LPGBT12_LOCKMODE	13	12
LPGBT12_SC_I2C	13	14

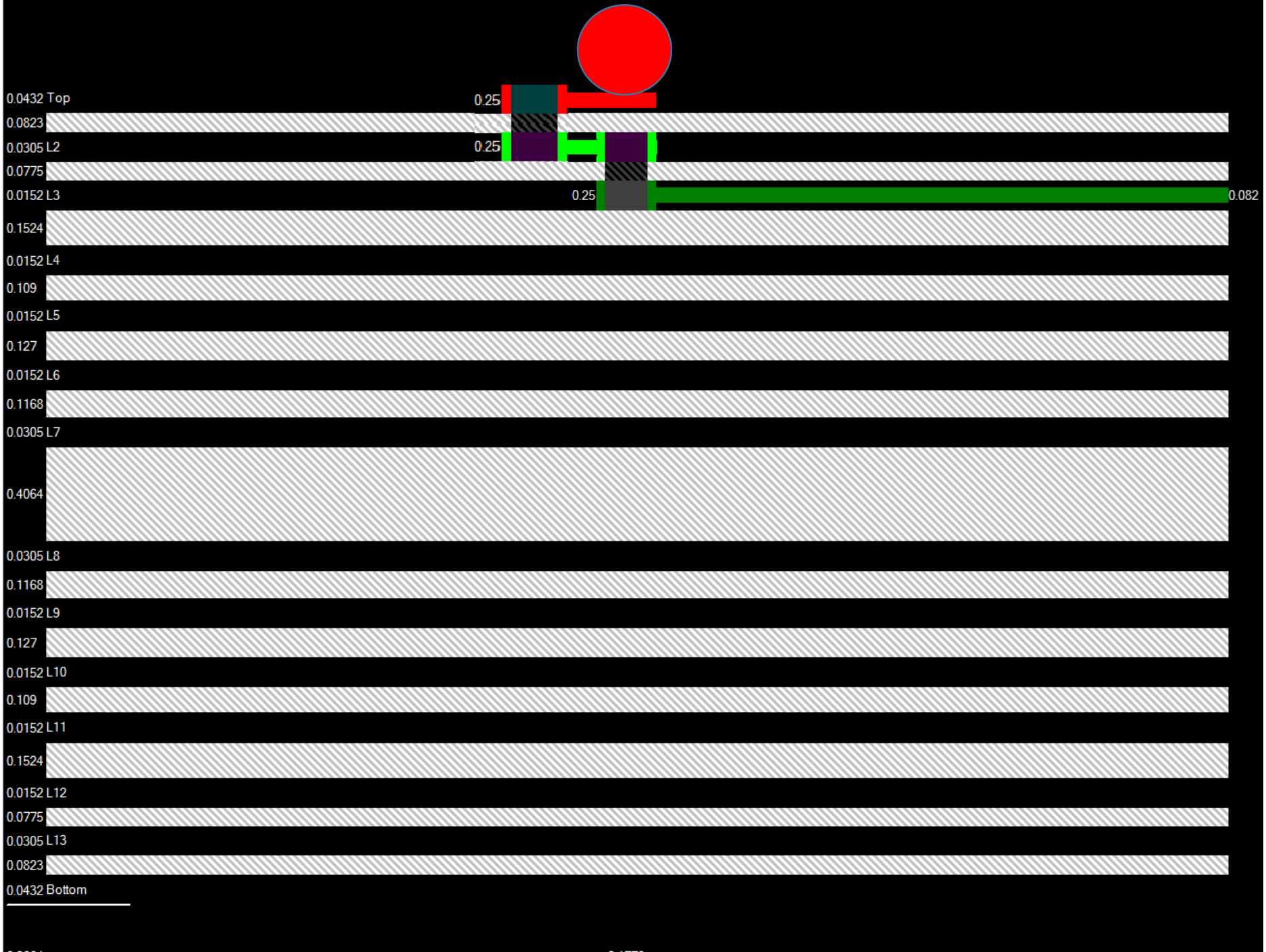
LpGBT package

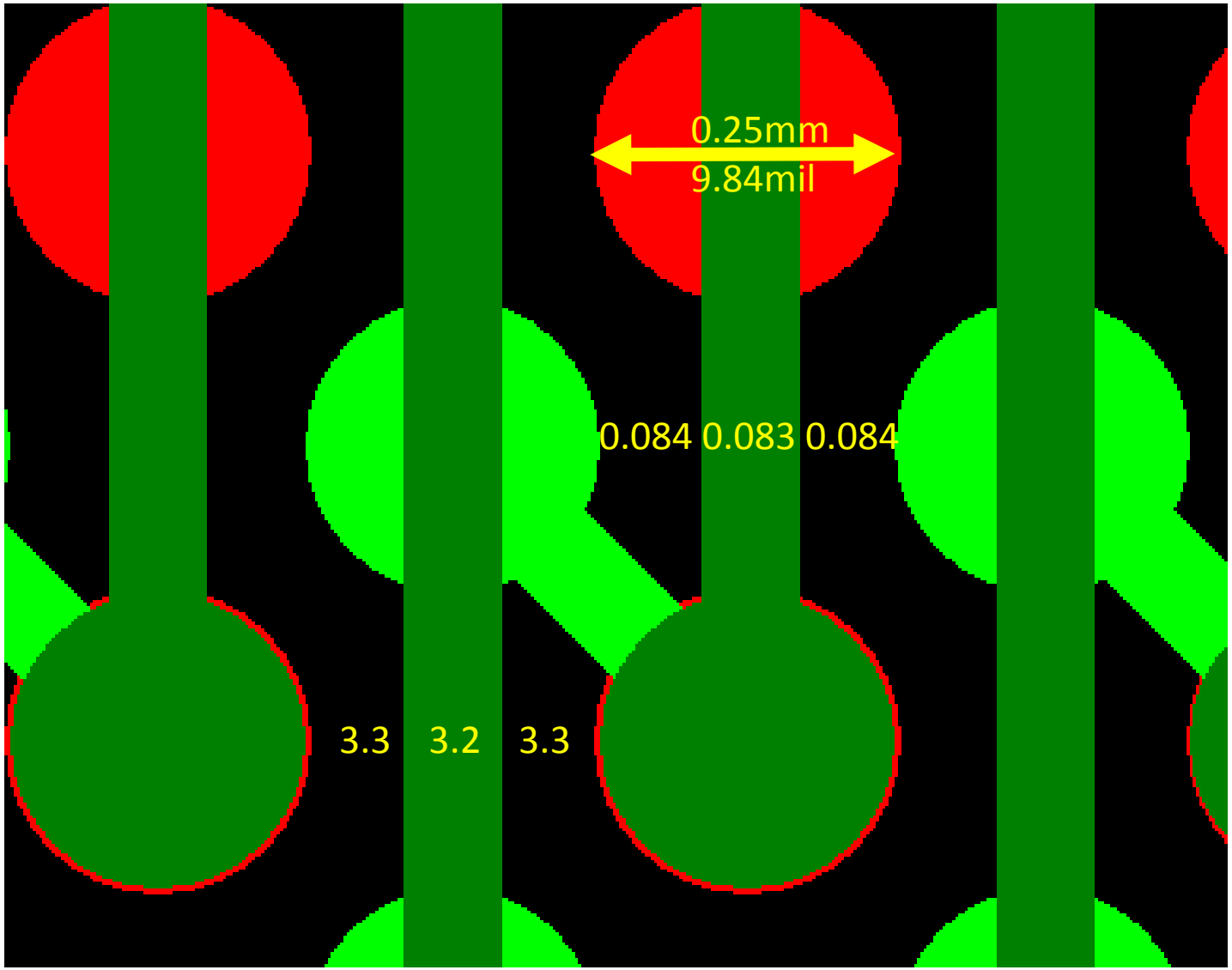



C:\Users\...\FEB2\FEB2_slice_board\FEB2_slice_board.pcb* - PADS Layout
File Edit View Setup Tools Help
(H) Top
Output Window
Changed current layer to Top
W:0.15
G:0.0625 0.0625
254.375
245.75
millimeters


C:\Users\...\FEB2\FEB2_slice_board\FEB2_slice_board.pcb* - PADS Layout
File Edit View Setup Tools Help
(V) L2
Output Window
Changed current layer to L2
W:0.15
G:0.0625 0.0625
255.25
246.875
millimeters


C:\Users\...\FEB2\FEB2_slice_board\FEB2_slice_board.pcb* - PADS Layout
File Edit View Setup Tools Help
(H) L3
Output Window
Changed current layer to L3
W:0.15
G:0.0625 0.0625
253.625
245.6875 millimeters


0.0432 Top
0.25
0.0823
0.0305 L2
0.25
0.0775
0.0152 L3
0.25
0.082
0.1524
0.0152 L4
0.109
0.0152 L5
0.127
0.0152 L6
0.1168
0.0305 L7
0.4064
0.0305 L8
0.1168
0.0152 L9
0.127
0.0152 L10
0.109
0.0152 L11
0.1524
0.0152 L12
0.0775
0.0305 L13
0.0823
0.0432 Bottom
2.0664
0.1778


0.25mm
9.84mil
0.084 0.083 0.084
3.3 3.2 3.3

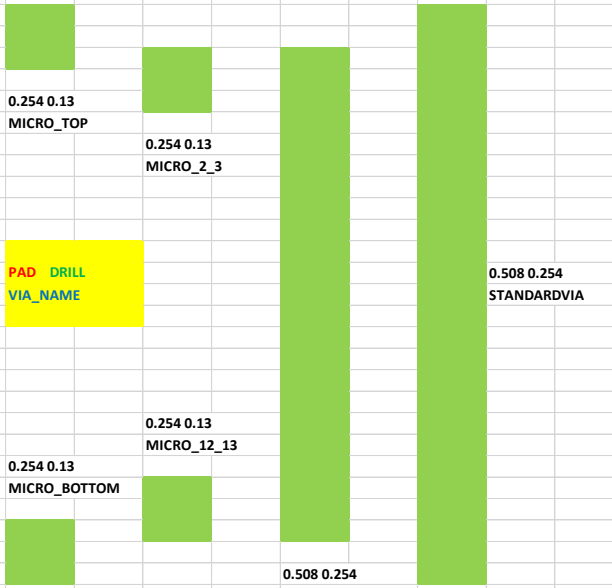
PCB Design Guidelines

Internal & External Trace Widths

		Standard	Advanced	Engineering	
	External Trace	.004"	0.003"	0.0025"	
Trace & Space	External Space	.004"	0.003"	0.0025"	
	Internal Trace	.004"	0.003"	0.0025"	
	Internal Space	.004"	0.003"	0.0025"	
Cu Weight		Trace & Space	Trace & Space	Trace & Space	Finished Weight
Plated Layer starting	External 1/4 oz		0.003"	0.0025"	average 0.0016"
Plated Layer starting	External 3/8 oz		0.003"	0.00275"	average 0.0018"
Plated Layer starting	External 1/2 oz	0.004"	0.0035"		average 0.0021"
Plated Layer starting	External 1 oz	0.005"	0.0045"		average 0.0026"
Plated Layer starting	External 2 oz	0.008"	0.0075"		average 0.0038"
Plated Layer starting	External 3 oz	0.011"	0.0105"		average 0.005"
Plated Layer starting	External 4 oz	0.014"	0.0135"		average 0.0062
Plated Layer starting	External 5 oz	0.017"	0.0165"		
non-plated Layer starting	Internal 1/4 oz		0.003"	0.0025"	
non-plated Layer starting	Internal 3/8 oz		0.003"	0.00275"	0.0004"
non-plated Layer starting	Internal 1/2 oz	0.004"	0.0035"		0.0006"
non-plated Layer starting	Internal 1 oz	0.005"	0.004"		0.0012"
non-plated Layer starting	Internal 2 oz	0.007"	0.006"		0.0026"
non-plated Layer starting	Internal 3 oz	0.009"	0.008"		0.004"
non-plated Layer starting	Internal 4 oz	0.011"	0.010"		0.0054"
non-plated Layer starting	Internal 5 oz	0.013"	0.012		0.0068"

FEB2 stack-up

Layer №	LAYER DESCRIPTION	Segment	Cu WT(OZ PER SQ FT)	EST THK mils	EST THK mm	Differential (100 Ohms+/-10%) FINISHED LW/SP(MILS)	Calculated Zdiff	Dk	LW/Sp mm
	SOLDERMASK			0.60	0.0152				
1	PRIMARY SIDE	Cu	0.33oz + plating	1.70	0.0432	4.0/5.0	100.16		0.1016/0.127
		Prepreg		3.24	0.0823			3.08	
2	PLANE	Cu	0.33oz + plating	1.20	0.0305	REF	REF		
		Prepreg		3.05	0.0775			3.08	
3	SIGNAL	Cu	0.5	0.60	0.0152	3.2/3.6	100.27		0.082/0.0914
		Core		6.00	0.1524			3.22	
4	PLANE	Cu	0.5	0.60	0.0152	REF	REF		
		Prepreg		4.29	0.1090			3.00	
5	SIGNAL	Cu	0.5	0.60	0.0152	3.2/3.0	100.56		0.082/0.0762
		Core		5.00	0.1270			3.36	
6	PLANE	Cu	0.5	0.60	0.0152	REF	REF		
		Prepreg		4.60	0.1168			3.00	
7	PLANE	Cu	1	1.20	0.0305	REF	REF		
		Core		16.00	0.4064			3.52	
8	PLANE	Cu	1	1.20	0.0305	REF	REF		
		Prepreg		4.60	0.1168			3.00	
9	PLANE	Cu	0.5	0.60	0.0152	REF	REF		
		Core		5.00	0.1270			3.36	
10	SIGNAL	Cu	0.5	0.60	0.0152	3.2/3.0	100.56		0.082/0.0762
		Prepreg		4.29	0.1090			3.00	
11	PLANE	Cu	0.5	0.60	0.0152	REF	REF		
		Core		6.00	0.1524			3.22	
12	SIGNAL	Cu	0.5	0.60	0.0152	3.2/3.6	100.27		0.082/0.0914
		Prepreg		3.05	0.0775			3.08	
13	PLANE	Cu	0.33oz + plating	1.20	0.0305	REF	REF		
		Prepreg		3.24	0.0823			3.08	
14	SECONDARY SIDE	Cu	0.33oz + plating	1.70	0.0432	4.0/5.0	100.16		0.1016/0.127
	SOLDERMASK			0.60	0.0152				
Est Board thickness over plating (mils and mm)				81.36	2.0665				
		Total		82.5600	2.0970				



PCB Design Guidelines

Laser Drilled Blind & Buried Microvias

Attritube	Standard	Advanced	Engineering	DpMV™	
Pad diameter	0.012"	0.010"	0.0086"	0.012"	
Laser drill diameter	0.006"	0.005"	0.005"	0.006"	
Dielectric thickness	0.0025" - 0.003"	0.0025" - 0.004"	0.0025 - 0.004"	0.006"	
Aspect Ratio	0.4:1 - 0.5:1	0.5:1 - 0.8:1	0.5:1 - 0.8:1	one-to-one	
Anti Pad	0.005"/side	0.004"/side	0.004"/side	0.004"/side	
Dog Bone Offset	0.005" space Pad-Pad	Pads Tangent	0.001" Pad overlap	0.005"Space	

Proposed Laser vias

MICRO vias	Pad	Laser drill	Dielectric
MICRO_TOP	10	5	3.24
MICRO_2_3	10	5	3.05
MICRO_2_3	10	5	3.05
MICRO_BOTTOM	10	5	3.24

PCB Design Guidelines

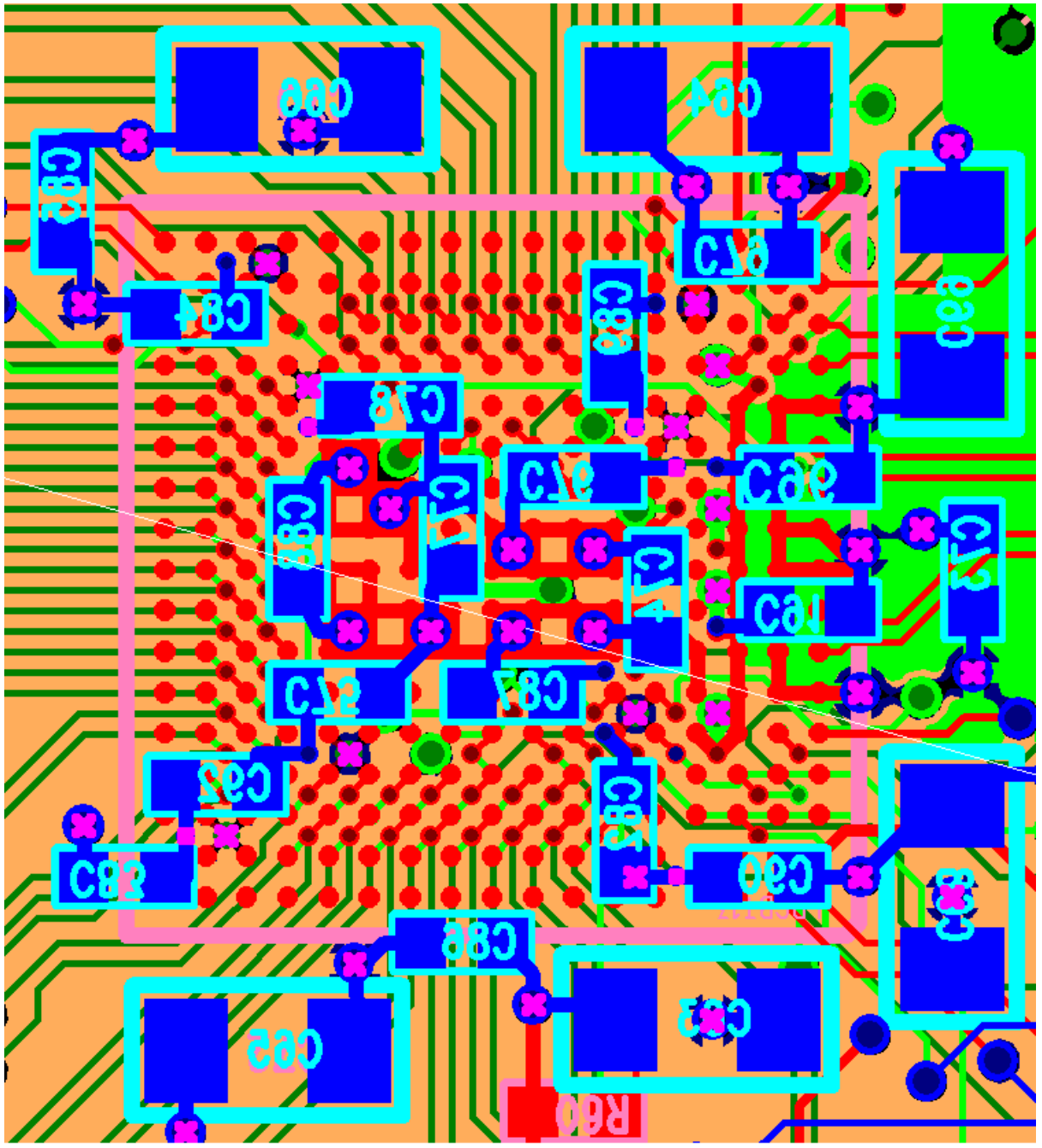
Mechanical Drilled Blind, Buried, and Through Holes

	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
	0.006"	0.016"	0.026"	up to 0.039"	6.5:1
Drill & Pad Diameter	0.008"	0.018"	0.028"	up to 0.062"	7.75:1
IPC Class 2	0.010"	0.020"	0.030"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.022"	0.032"	up to 0.120"	10:01

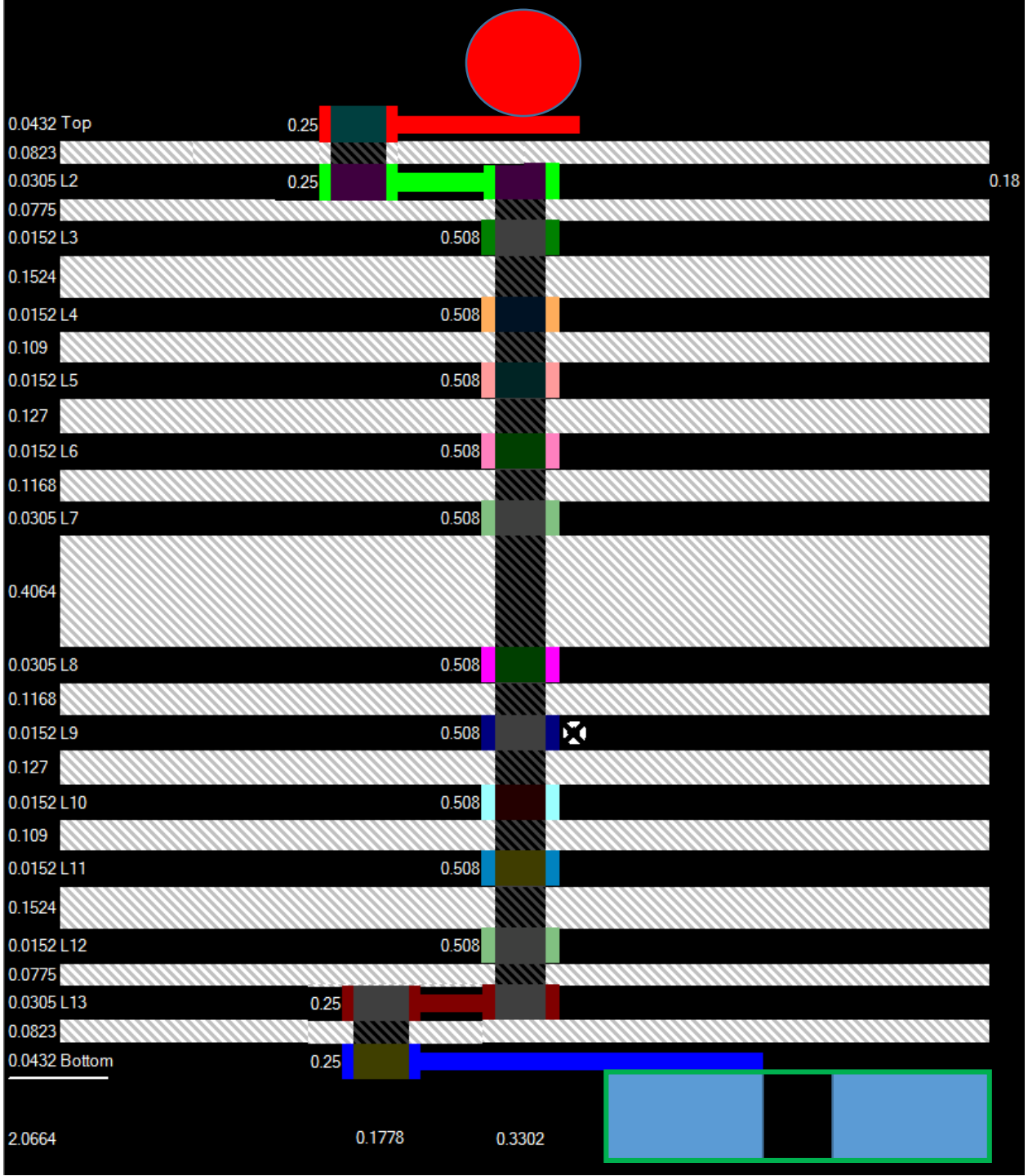
	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
Drill & Pad Diameter	0.008"	0.023"	0.033"	up to 0.062"	7.75:1
IPC Class 3	0.010"	0.025"	0.035"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.027"	0.037"	up to 0.120"	10:01
	0.0135"	0.028"	0.038"	up to 0.135"	10:01

Mechanical vias

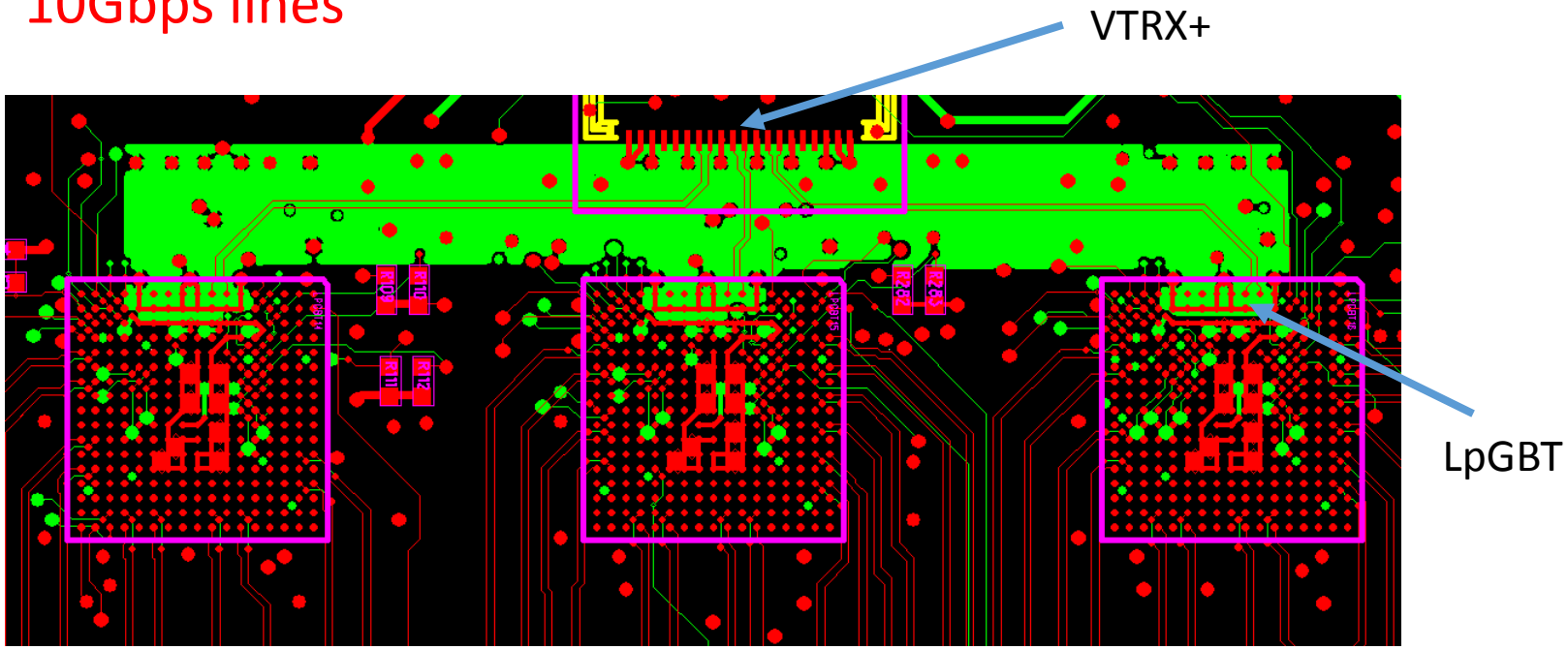
Via type	Drill	Pad	PCB Thickness	Aspect Ratio
STANDARDVIA	10	20	0.082”	8.2
BURRIED_2_13	10	20	0.071”	7.1


C89
C88
C87
C86
C85
C84
C83
C82
C81
C80
C79
C78
C77
C76
C75
C74
C73
C72
C71
C70
C69
C68
C67
C66
C65
C64
R60

Power Connections & Filters



10Gbps lines

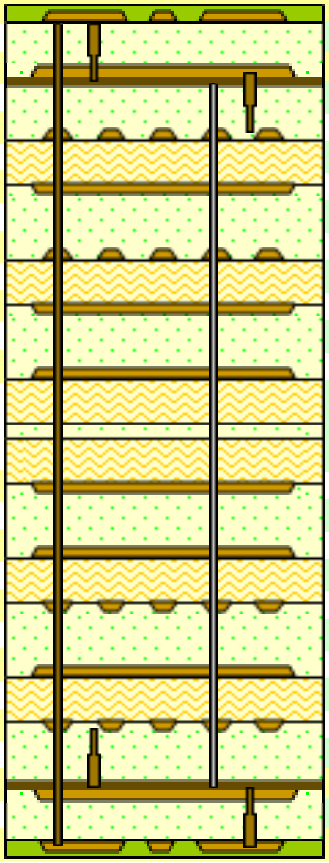


Printed on Top layer

Target diff line impedance 100 Ohm

Line width	4mils
Line space	5mils

Dielectric_type	signal loss [per inch@10G]
TU872SLK	1.65dB
TU883	1.35dB
Megtron6	1.35dB

Layer	Cu Thick. (mils)	Cu Foil wt (oz)		DK	Lam. Thick. (mils)	Description
1	1.75	.375 oz				Foil .375 oz
				3.24	3.83	Prepreg Megtron6 1078(72) 185 18Gx24
2	1.05	.375 oz				Foil .375 oz
				3.24	3.64	Prepreg Megtron6 1078(72) 185 18Gx24
3	0.60	0.5 oz				
				3.42	5.90	Core Megtron6 5.90mils 2x1080 0.5 oz / 0.5 oz 185 HVLP 18.25Gx24.25
4	0.60	0.5 oz				
				3.25	4.12	Prepreg Megtron6 1035(70)/1035(70) 185 18Gx24
5	0.60	0.5 oz				
				3.64	4.90	Core Megtron6 4.90mils 2116 0.5 oz / 0.5 oz 185 HVLP 18.25Gx24.25
6	0.60	0.5 oz				
				3.25	4.27	Prepreg Megtron6 1035(70)/1035(70) 185 18Gx24
7	1.20	1 oz				
				3.42	5.90	Core Megtron6 5.90mils 2x1080 1 oz / 0 185 RTF 18.25Gx24.25
				3.24	4.09	Prepreg Megtron6 1078(72) 185 18Gx24
				3.42	5.90	Core Megtron6 5.90mils 2x1080 0 / 1 oz 185 RTF 18.25Gx24.25
8	1.20	1 oz				
				3.25	4.27	Prepreg Megtron6 1035(70)/1035(70) 185 18Gx24
9	0.60	0.5 oz				
				3.64	4.90	Core Megtron6 4.90mils 2116 0.5 oz / 0.5 oz 185 HVLP 18.25Gx24.25
10	0.60	0.5 oz				
				3.25	4.12	Prepreg Megtron6 1035(70)/1035(70) 185 18Gx24
11	0.60	0.5 oz				
				3.42	5.90	Core Megtron6 5.90mils 2x1080 0.5 oz / 0.5 oz 185 HVLP 18.25Gx24.25
12	0.60	0.5 oz				
				3.24	3.64	Prepreg Megtron6 1078(72) 185 18Gx24
13	1.05	.375 oz				Foil .375 oz
				3.24	3.83	Prepreg Megtron6 1078(72) 185 18Gx24
14	1.75	.375 oz				Foil .375 oz

78.51	Thickness over Laminate
82.01	Thickness over Copper
83.01	Thickness over Soldermask

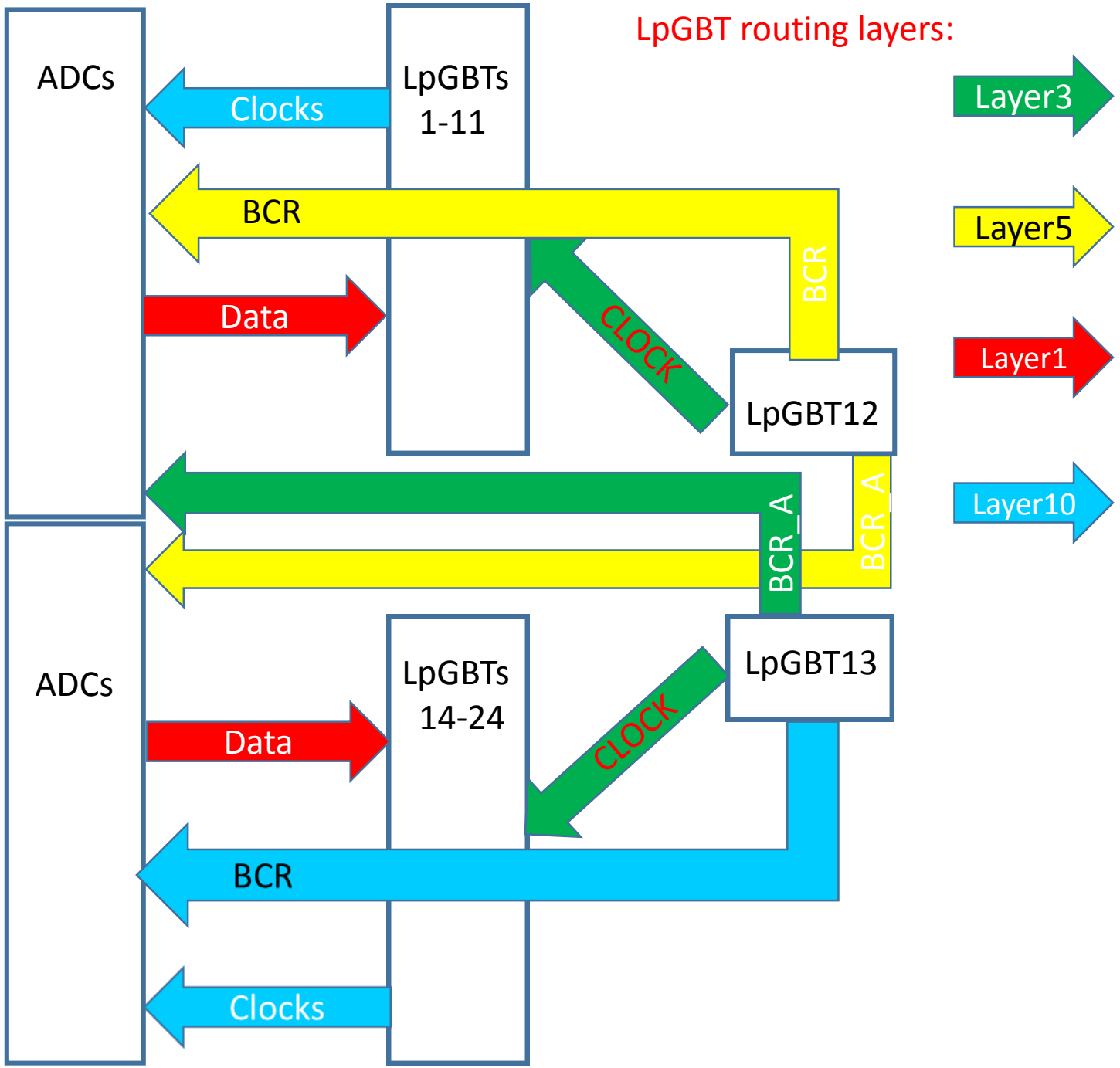
Drill Table								
Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Drill Size (min)	Drill Depth	Pad Size(min)	Stacked Vias
1	14	Mech	PTH	--		79.41		
2	13	Mech	Via	Non-Conductive Via Fill (Flat)		69.65		
13	12	Laser	Micro Via	CuVF_Button Pattern		4.09		
14	13	Laser	Micro Via	CuVF_Button Pattern		4.28		
1	2	Laser	Micro Via	CuVF_Button Pattern		4.28		
2	3	Laser	Micro Via	CuVF_Button Pattern		4.09		

Impedance Table										
Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Edge Coupled Differential	Yes	100.00	+/-10	4.00	9.00	(2)	4.25	99.47	
3	Edge Coupled Differential	---	100.00	+/-10	3.20	6.80	(2, 4)	3.50	99.63	
5	Edge Coupled Differential	---	100.00	+/-10	3.20	6.20	(4, 6)	3.25	98.99	
10	Edge Coupled Differential	---	100.00	+/-10	3.20	6.20	(11, 9)	3.25	98.99	
12	Edge Coupled Differential	---	100.00	+/-10	3.20	6.80	(13, 11)	3.50	99.63	
14	Edge Coupled Differential	Yes	100.00	+/-10	4.00	9.00	(13)	4.25	100.50	

* Edge Coupled Pitch is measured from the center line of one differential trace to the center line of the other.

* This stack-up was created using estimated copper area percentages. (25% signal, 50% mix, 75% plane) Once data is received minor adjustments of traces and pre-preg thickness may occur.

Process Plating Info
Final Assembly - 1/14 = Pattern Plate
Sub Assembly - 2/13 = Pattern Plate


LpGBT routing layers:
ADCs
Clocks
LpGBTs
1-11
Layer3
BCR
Layer5
Data
CLOCK
BCR
Layer1
LpGBT12
BCR_A
BCR_A
Layer10
ADCs
LpGBTs
14-24
LpGBT13
Data
CLOCK
BCR
Clocks