FEB2 Slice Testboard Startup

24-09-2021 (v1.1)

Permanent documentation for slice testboard at:

https://twiki.nevis.columbia.edu/twiki/bin/view/ATLAS/SliceTestboard

Git Repository for GUI software:

https://gitlab.cern.ch/dawillia/slice-testboard

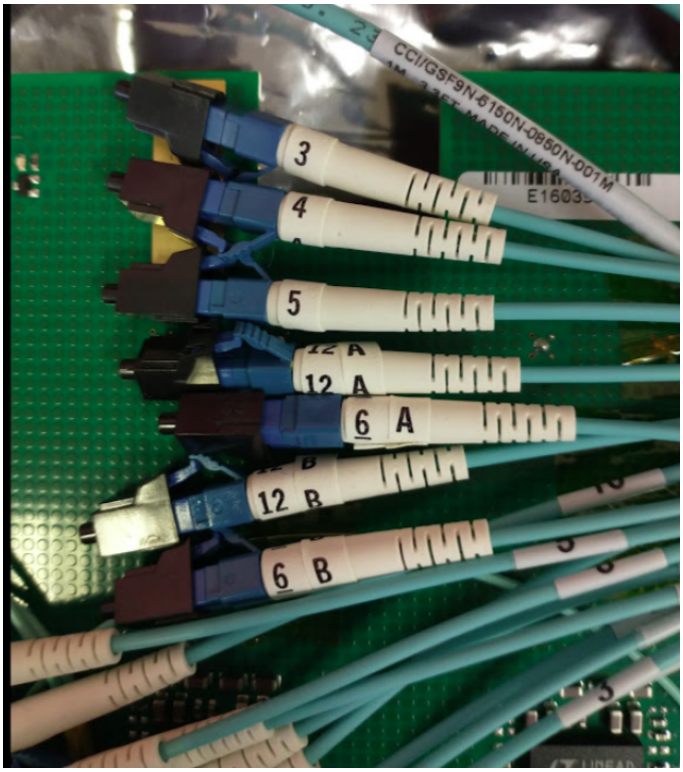
Required Setup Components

The startup instructions here are assuming the following items are present in the setup:

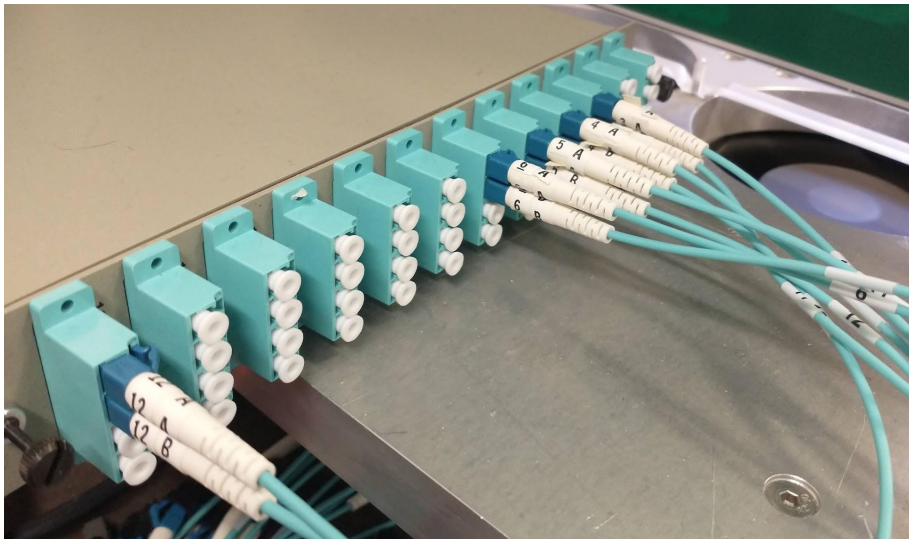
- v1.1 slice testboard
- Power connector and cable
- Power supply capable of >3A current output at 18V
- 3 MPO fanout cables
- Fiber patch box
- 1 MPO to MPO fiber cable
- PC running CentOS 7 Linux (tested with CentOS 7.8.2003)
- FELIX card FLX-712 installed in PC PCIe slot

Fiber Mapping - Based on Board E163634

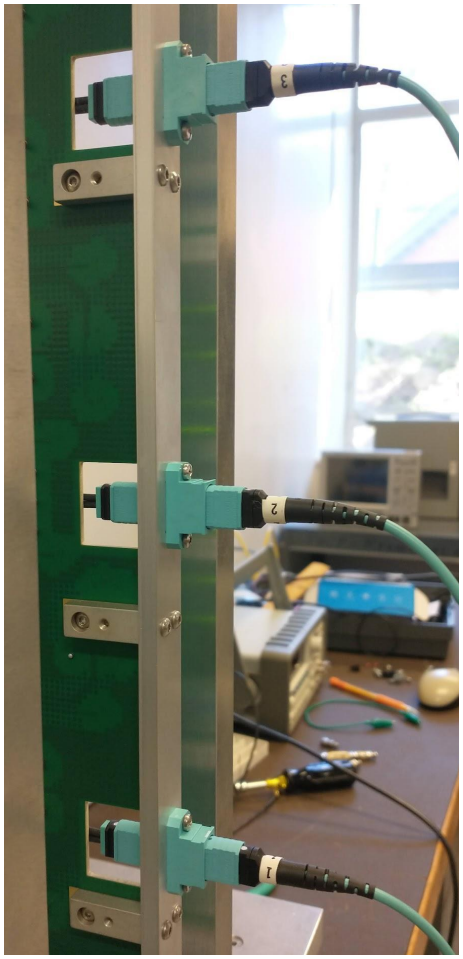
Board E163634 MPO fanout fibers connected to key lpGBTs were labeled as shown below:



The single fiber connections were connected to the fiber patch box as shown here:

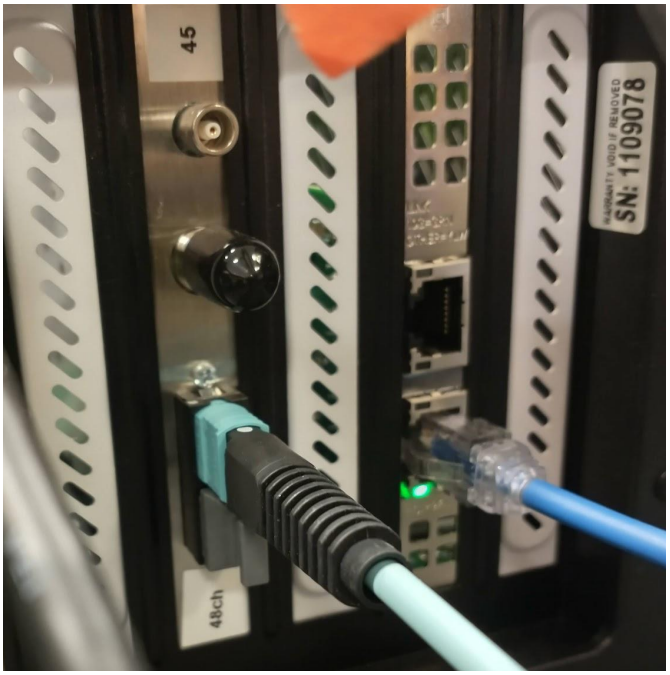


The fiber MPO fanout cable MPOs were connected to the slice testboard as shown here:



The fiber MPO-MPO cable is connected to the back of the fiber patch box as shown here:

The fiber MPO-MPO cable is connected to the FELIX card as shown here:



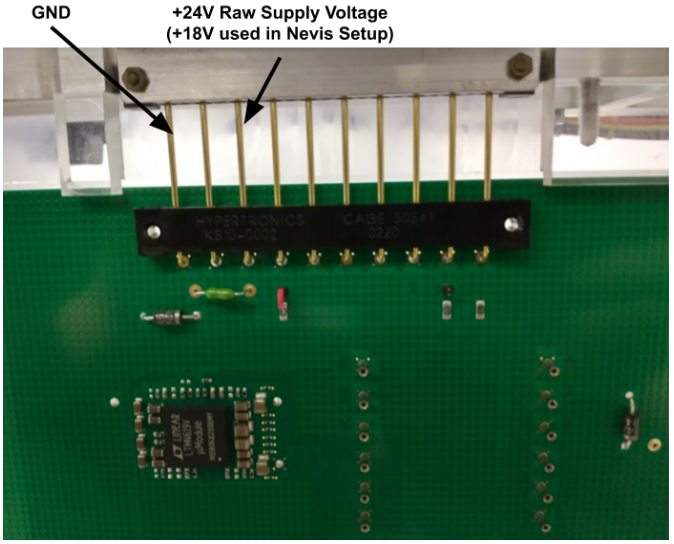
The fiber connection information is summarized in this table

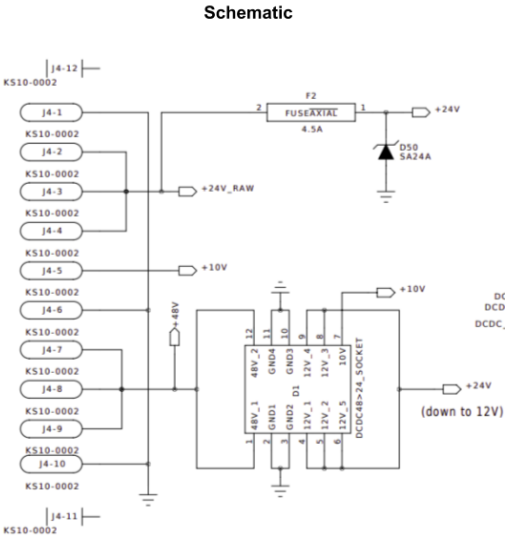
ID	Box Slot	MPO #	Fiber #	FELIX ch	Role
3A	3 left	3, top	10	1st RX 7	lpGBT16 to FELIX uplink, ch74-79 COLUTA19 (ch5-8), COLUTA20
3B	3 right	3, top	11	1st RX 6	lpGBT15 to FELIX uplink, ch68-73 COLUTA18, COLUTA19 (ch1-4)
4A	4 left	3, top	12	1st RX 5	lpGBT14 to FELIX uplink, ch64-67 COLUTA17
4B	4 right	1, bottom	10	1st RX 4	lpGBT11 to FELIX uplink, ch60-63 COLUTA16
5A	5 left	1, bottom	11	1st RX 3	lpGBT10 to FELIX uplink, ch54-59 COLUTA14 (ch5-8), COLUTA15
5B	5 right	1,	12	1st RX 2	lpGBT9 to FELIX uplink, ch48-53

		bottom			COLUTA13, COLUTA14(ch1-4)
6A	6 left	2, middle	6	1st RX 1	lpGBT13 to FELIX uplink
6B	6 right	2, middle	12	1st RX 0	lpGBT12 to FELIX uplink
12A	12 left	2, middle	5	1st TX 1	FELIX to lpGBT13 downlink
12B	12 right	2, middle	11	1st TX 0	FELIX to lpGBT12 downlink

Note that here COLUTA ADC and lpGBT numbers start from “1”, matching the labels in the board layout and block diagrams (see slide 2): https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2_block_diagrams.pdf

Power Connector

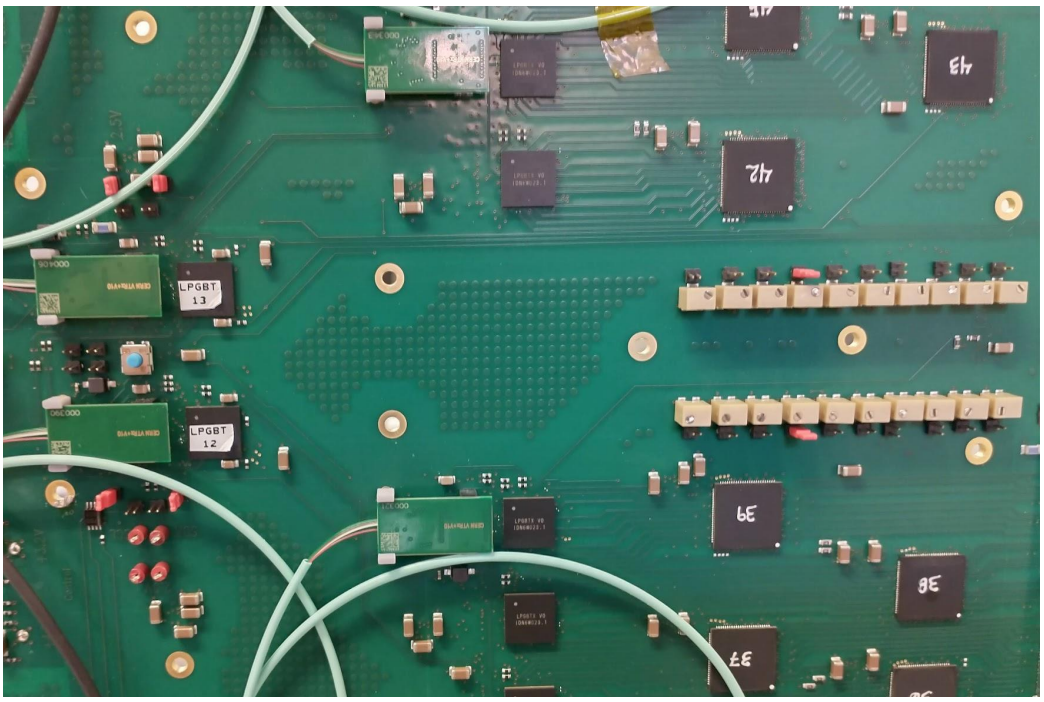




For reference the voltage supply connection to the slice testboard as used in the Nevis test setup is shown here. The raw supply voltage was set to 18V, resulting in roughly 2.2A of current draw for a fully configured slice-testboard.

Board Header Configuration and POT Adjustment

The set of headers corresponding to default operation of the board are shown here:



The required header numbers are H4, H57, H20, H21, H22, H23.

Additionally the outputs of potentiometers P9 and P13 should both be set to 0.6V when the board is fully configured. This sets an appropriate common mode reference voltage for the COLTUAs.

GUI Software and Board Configuration

The most up-to-date instructions for using the GUI are posted in the git repository page. A few notes for using this software with board E163634 specifically are provided here.

lpGBTs 12 and 13 on this board have had a minimal set of e-fuses burned to allow configuration over IC on powerup. The LED beside either of these lpGBTs should immediately turn on when their corresponding fiber (listed above) is connected to gigabit link. When this is the case the GUI software should be able to fully configure these lpGBTs, after which it can configure other chips on their respective I2C buses.

Instructions to connect and operate the USB interface as well as perform the e-fusing process are provided here:
https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/20210923_sliceBoard_usbInterface_eFusing_instructions.pdf

The first time running the GUI after checking out the software there will be series of questions on the command line used to set up the “metadata.txt” file, which contains persistent information about the test setup. Additionally the first time GUI records data it will create a directory to store the output files in “../Runs” ie above the GUI source directory.

Basic Startup Procedure

(from slice-testboard repo README)

1. If starting completely from scratch, begin by downloading and compiling the FLX software package from here: https://gitlab.cern.ch/atlas-tdaq-felix/software. (If needed, change flx_setup1.sh to point to the proper paths). The libflx-lpgbt package is also required, obtained from

2. Configure the FLX with the proper firmware. Following the instructions in Chapter 4 of the flx manual available at:
https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/felix-user-manual.pdf
Note that on flx-srv-atlas the Vivado suite and bitstream files are in the atlas-group account, while the GUI software is in the dawillia account:
Vivado version: software/Xilinx/Vivado/2018.1/settings64.sh
The current bitstream file is:
flx-srv-atlas:/home/atlas-group/software/bitstreams/felix_top_bnl711.bit
It can also be found here:
https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/felix_top_bnl711.bit

Once the firmware is programmed, reboot (soft reboot - a hard reboot will wipeout the firmware configuration you just did!).

3. Setup the anaconda environment as follows:

If the computer is already setup but you just (soft) rebooted, start here!
4. cd to the ~/FLX/slice-testboard/ directory on flx-srv-atlas and run `source flx_setup1.sh`. This will start the driver, start the FLX, and set up the FLX to send the clock and start to be ready to take data.

If the computer is already on and configured, start here!
5. Activate the environment with `conda activate coluta`

6. Run the GUI with `python sliceBoard.py`

7. If you want to take data, use one of the “Take Sine Data”, “Take Pedestal Data” or “Take Pulse Data” buttons in the Data tab of the GUI.

Configuring the board

1. To configure all chips on the board with their default configuration, press **Configure All** in the Control tab. Check the “Readback Configuration” to enable readbacks of chip configuration register writes, which is recommended to ensure the configuration was written correctly. The GUI and terminal printout should indicate if all the onboard chips were written correctly.

2. To configure only specific chips, choose the chip from the drop down menu on the Control tab, and press the corresponding **Configure** button.
Note: lpgbt12 must be configured before any other chips on the lpgbt12 side of the board, and likewise for lpgbt13.

3. To write and read specific lpgbt registers, use the drop down menu on the Control tab to select an lpgbt. Enter the register to write/read in hex. If writing, also enter the value to write in hex. If you want to write the same value to more than one consecutive register, or read from multiple consecutive registers, enter the number of consecutive registers as a decimal. Press **Write to LpGBT** or **Read From LpGBT**.
Note: If you are switching between data lpGBTs, you will need to do a master reset each time you switch. This can be done with the **Reset lpGBT12/13 I2C Control** buttons.

4. To update a configuration, navigate to the chip using the LAUROC/ COLUTA/ lpGBT tabs. Change the configuration settings, then return to the Control tab and press **Send Updated Configurations**.

Configurations for taking Data
5. By default, COLUTA channels 1-8 come up in normal mode. This can be changed in the COLUTA/Channel/DDPU tab. Additionally, in Channel 1 for each COLUTA there are **Turn On Serialier Mode** and **Turn Off Serializer Mode** buttons, which change serializer mode for all channels on that COLUTA.

Voltage and Temperature Monitoring

1. To start, configure at least lpGBT12 and lpgbt13 (you may also configure the whole board, but this will alter the power consumption).

2. Navigate to the Power/Voltage tab. Select the voltages you want to measure (or use **Select All Voltages** to choose all voltages) and press **Read Voltages.**
Note: Pending improvement to calibration constants in software - voltage reading may not be exact. Use calculateVREF procedure to determine calibration constants

3. To measure temperatures, navigate to the Power/Temperature tab. Select the temperature points you want to measure (or use **Select All Temperatures** to choose all temperature points) and press **Read Temperatures**. A temperature reading will appear in celsius.
Note: Pending improvement to calibration constants in software - temperature reading may not be exact.

Find board schematics with temperature and voltage points here (maybe?):
https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2_slice_board_schematic.pdf

Current Monitoring

The following table shows the expected current draw and power usage of the board given an 18V source, at various stages of chip configuration.

Chip	test 1(mA)	test 2	test 3	test 4	Avg (mA)	avg power usage (18V) (W)
nothing	285.6	285.6	285.6	285.6	285.6	5.14

lpgbt12	626.3	626.3	626.6	622.7	625.5	11.26
lpgbt13	1017	1017	1012	1015	1015.3	18.27
lpgbt11	1025	1024	1020	1024	1023.3	18.42
lpgbt14	1019	1022	1018	1018	1019.3	18.35
lpgbt9	1027	1030	1027	1026	1027.5	18.50
lpgbt10	1036	1039	1036	1035	1036.5	18.66
lpgbt15	1047	1049	1046	1046	1047.0	18.85
lpgbt16	1066	1068	1066	1065	1066.3	19.19
coluta16	1136	1139	1135	1137	1136.8	20.46
coluta17	1207	1205	1202	1208	1205.5	21.70
coluta20	1284	1284	1279	1283	1282.5	23.09
lauroc16	1284	1284	1279	1283	1282.5	23.09
lauroc20	1284	1284	1279	1283	1282.5	23.09

Running Clock Scan

To run the clock timing parameter scan open the GUI control tab and on the far right side select the COLUTAs to include in the scan by checking the corresponding boxes. Then press the **Run Clock Scan** button to run the scan. When the scan is done it will create a directory with a new set of configuration files containing the updated clock timing parameters. They can be used by copying them into the “config” directory or by modifying the files within.