LAr Slice Testboard Noise Investigation

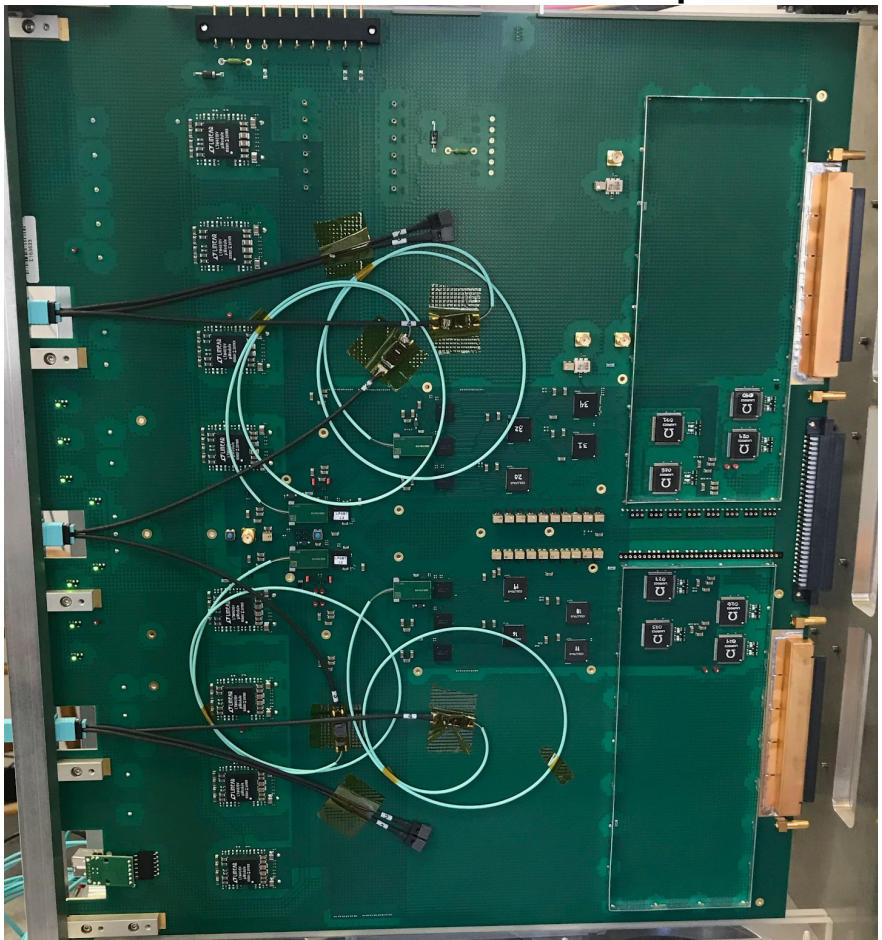
2021-04-13

Slice Testboard Noise Issues

- Pedestal noise measurements with Slice Testboard (that uses 8 LAUROC2 chips connected to 8 COLUTAv3 ADC chips) show some issues:
  - Individual channels seem significantly noisier than expected (particularly apparent for LO gain)
  - Coherent noise across channels is significantly higher than <5% specification and what was achieved previously with Analog Testboard (using LAUROC1 and COLUTAv2)
- As summarized in these slides, we have been systematically investigating these issues, trying many different configurations and making many different measurements to try shed light on what is going on
- Two main noise features observed: 250kHz line and 20kHz “bump”
  - 20kHz noise appears to be main source of correlated noise

Slice Testboard Setup, LAUROC Configuration

Slice Testboard in Test Setup



- v1.1 slice testboard in test setup
- 8 LAUROC2 + 8 COLUTAv3 chips
- Readout via lpGBTs into FELIX
- Inject signals through dedicated SMA input into LAUROC20 ch4 input
- Configuring LAUROCs with defaults in LAUROC2 datasheet
  - Using 25Ohm, 10mA settings
    - sw_R025_10mA = 1
    - sw_R025_5mA = 0

Reminder: DRE and MDAC Inputs on COLUTAv3

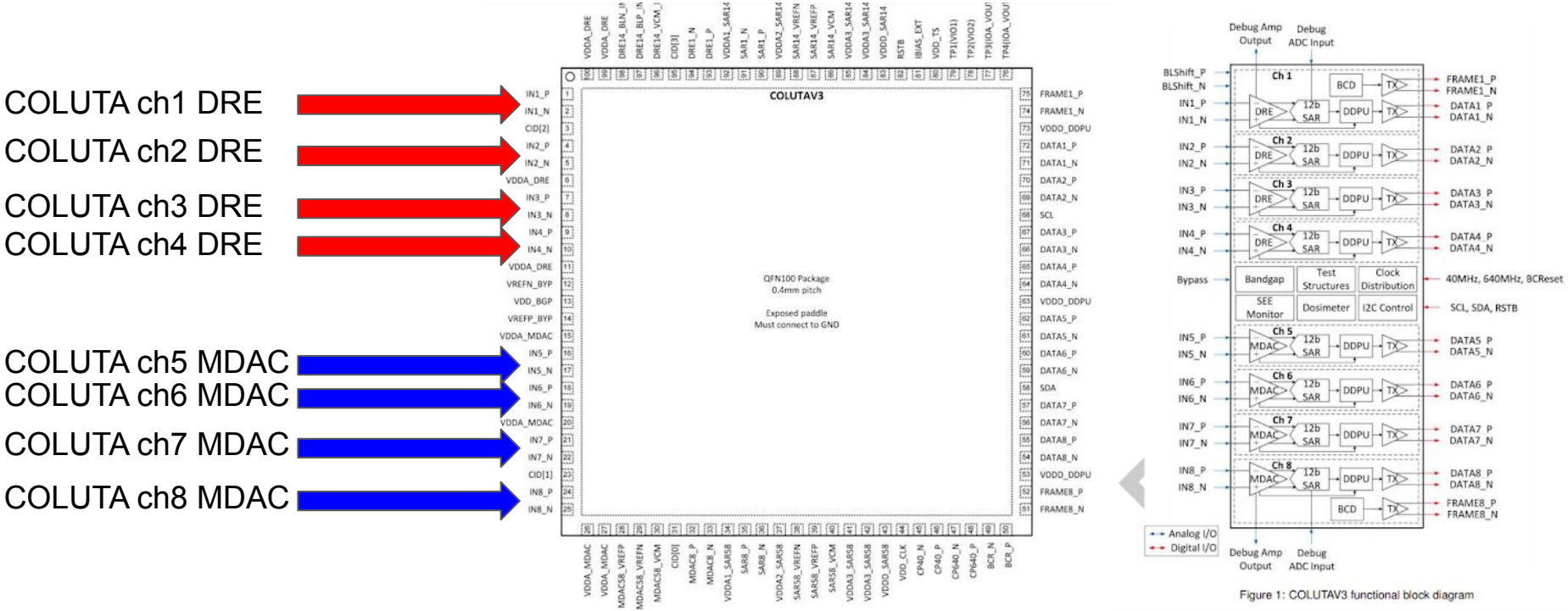


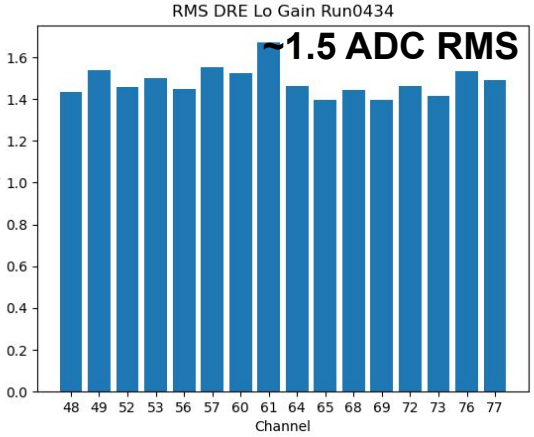
Figure 1: COLUTAV3 functional block diagram

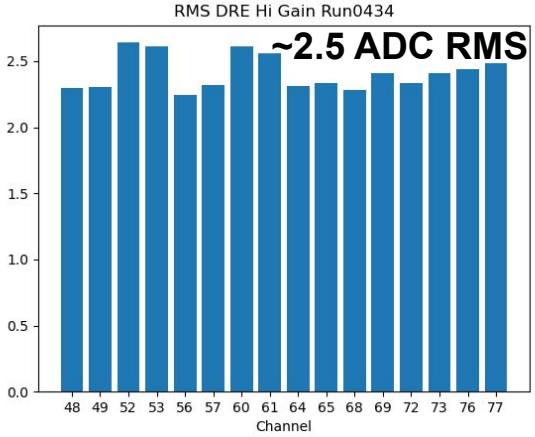
- COLUTAv3 has two different input types, ch1-4=DRE, ch5-8=MDAC
- For these studies, DRE configured to use fixed 1x gain mode, MDAC is effectively 4x gain
  - Impacts measured noise magnitudes, but channel performance is similar
- Each LAUROC outputs to 4 DRE channels, 4 MDAC
  - LAUROC ch1 LG+HG = DRE, ch2 HG+LG = DRE, ch3 LG+HG = MDAC, ch4 HG+LG = MDAC

Standard Slice Testboard Noise Measurements

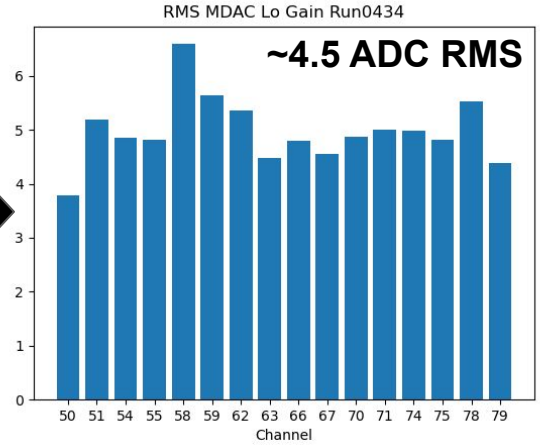
LOW GAIN | **HIGH GAIN**

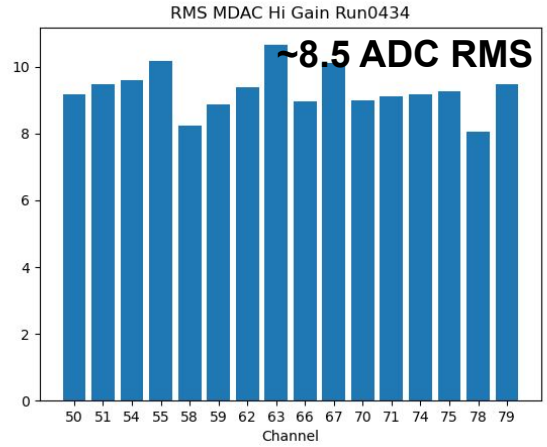
DRE Chs
(fixed 1X gain, to avoid issues of DRE with shifted baseline)





MDAC Chs





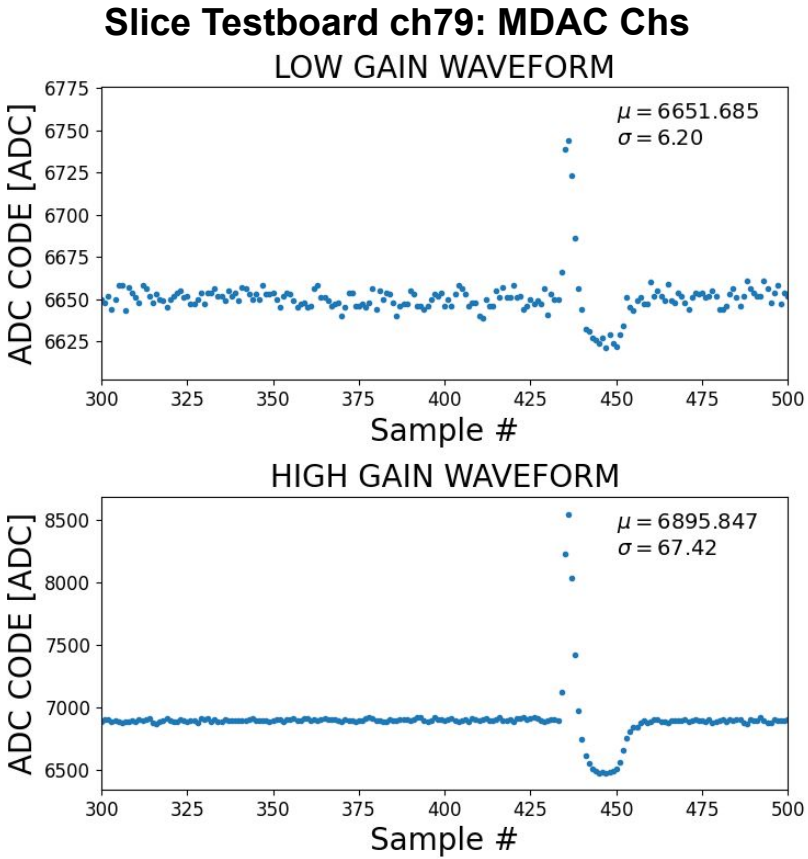
Noise measurements made with no detector load on LAUROC inputs

Expect ~4x more noise on MDAC chs vs DRE chs in 1x gain mode, by design

Sampling performance for MDAC and DRE channels similar in CV3 testboard measurements

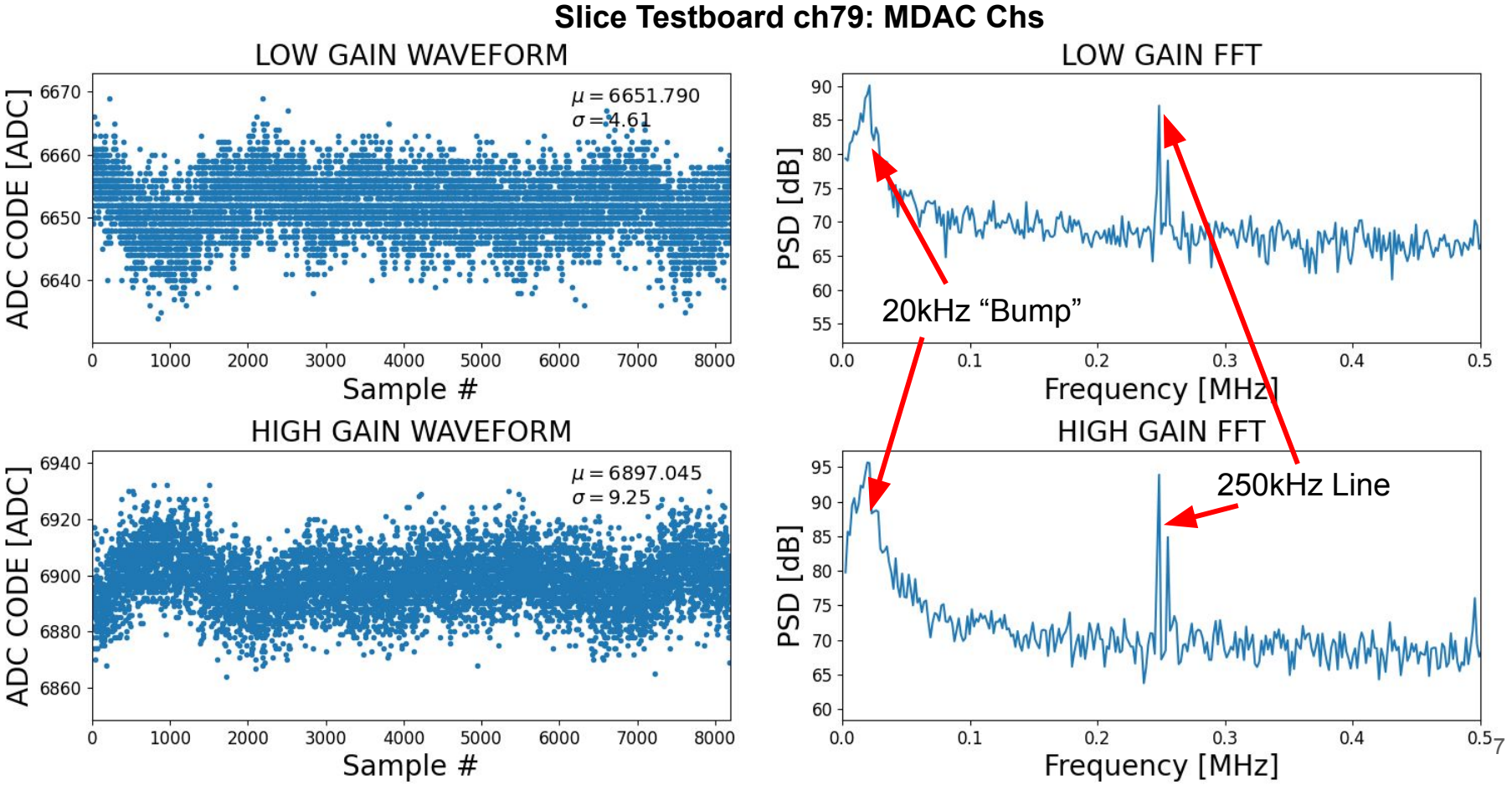
Notes: (1) HG channel noise only ~2 times LG noise
(2) COLUTA-only noise ~1.3 ADC counts

Relative Gain Measured with Injected AWG Signal



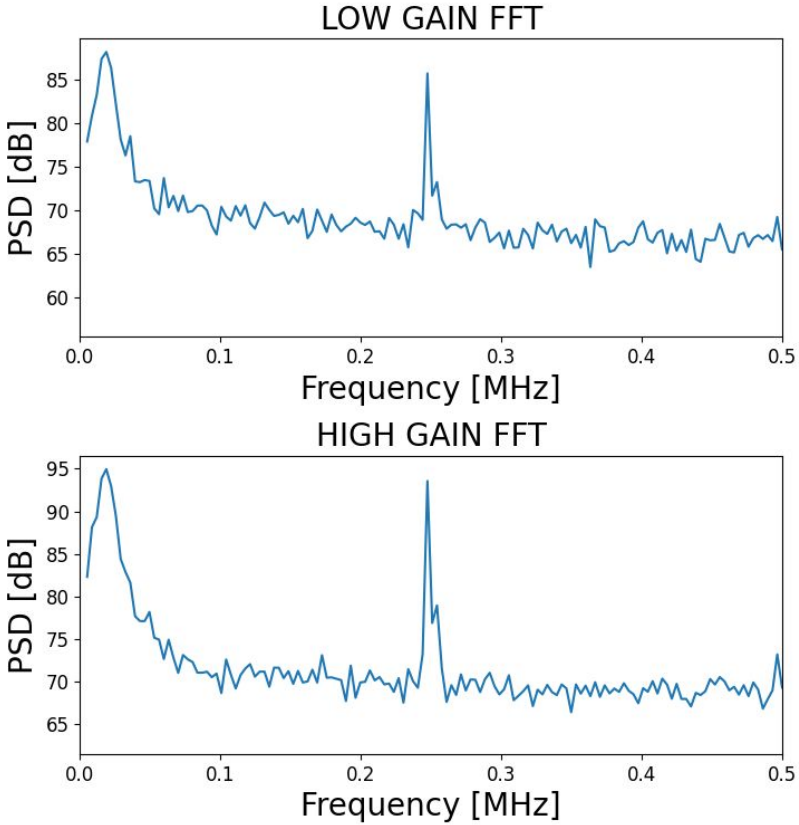
- Inject AWG signals through one of the LAUROC inputs
- Observe LAr-like signal on COLUTA, LAUROC+COLUTA signal path working on slice testboard!
- Rough estimate ~20x relative gain on pulse signals between HG and LG channel
- Reminder: observed noise on HG channels generally only 2x higher than LG channels
  - LG channels noisier than expected? (would expect to be dominated by COLUTA noise and quantization error of ~1.3 ADC counts?)
  - As will be shown, results show also “excess noise” in HG channels, but less apparent due to overall higher noise level)

Main Noise Features: 20kHz Bump+250kHz Line in FFT

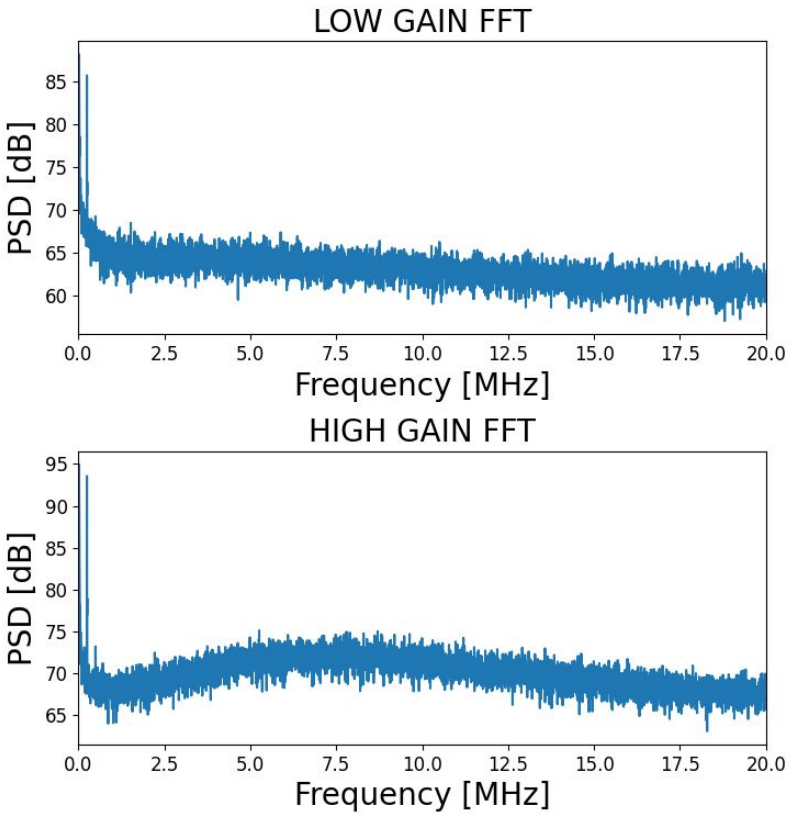


20kHz and 250kHz Noise Features are Dominant

Slice Testboard ch79 FFTs 500kHz Range

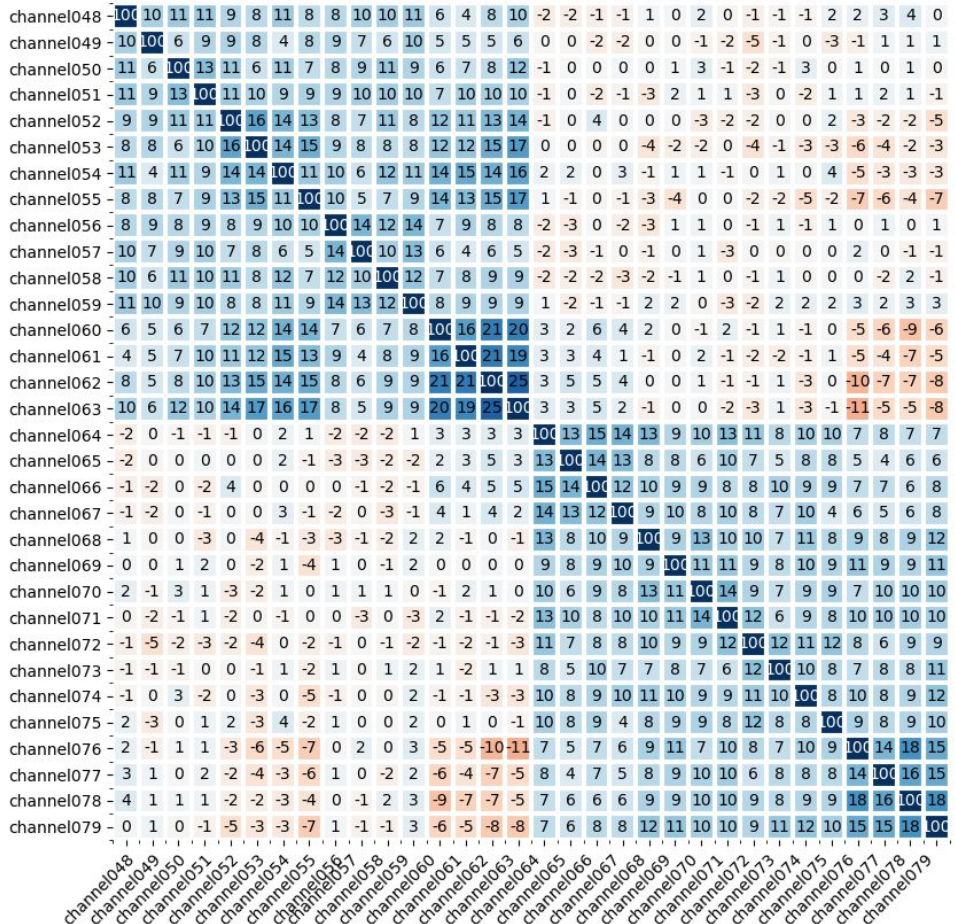


Slice Testboard ch79 FFTs 20MHz Range

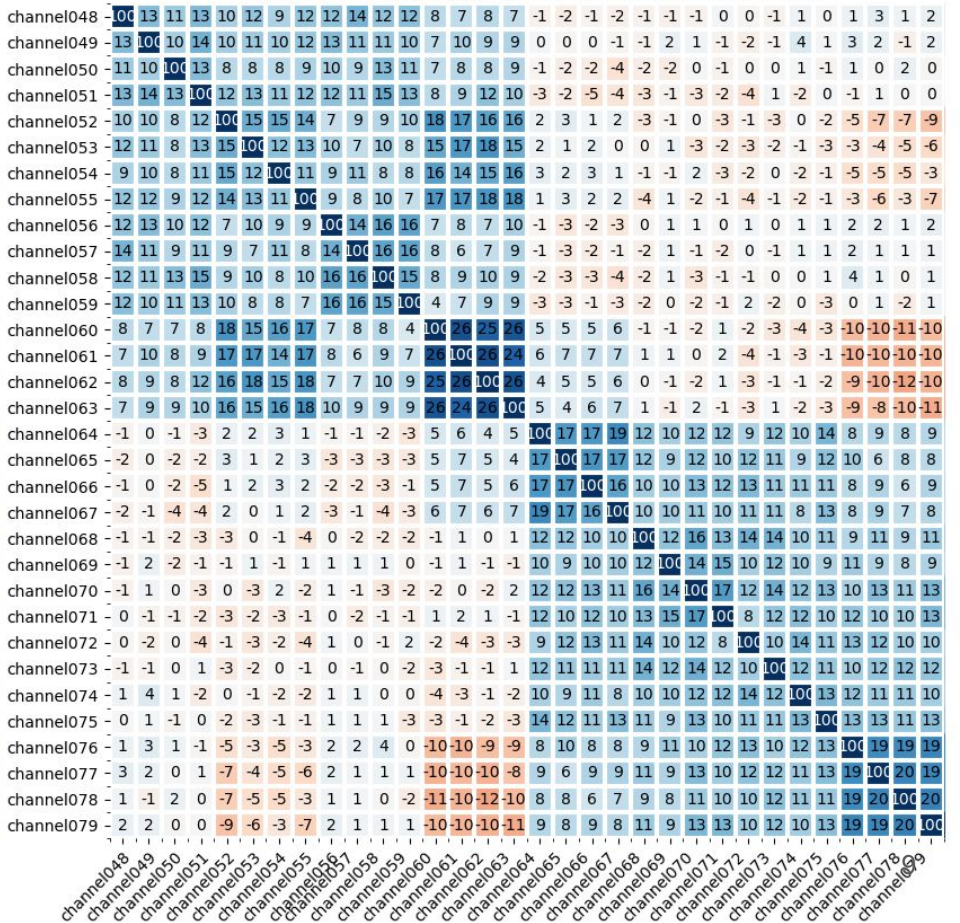


Noise is >10-20% Correlated Across Slice Testboard Halves

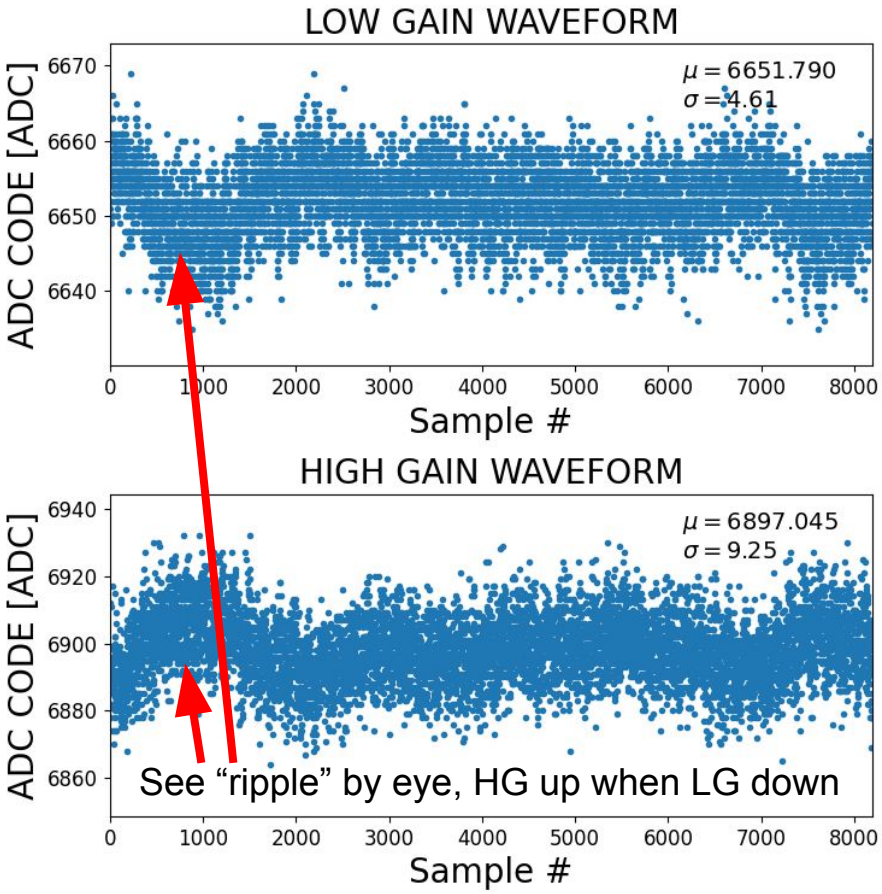
LOW GAIN Chs



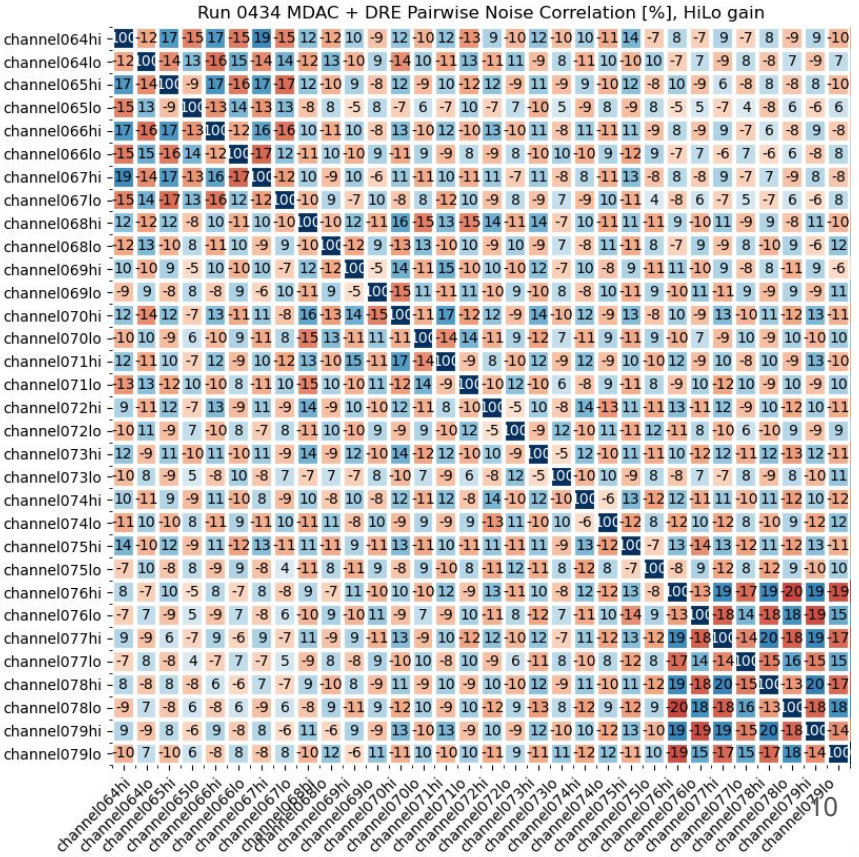
HIGH GAIN Chs



20kHz Noise Visible as ~50us “Ripple” in Waveforms, Anti-Correlated Between LG and HG Channels

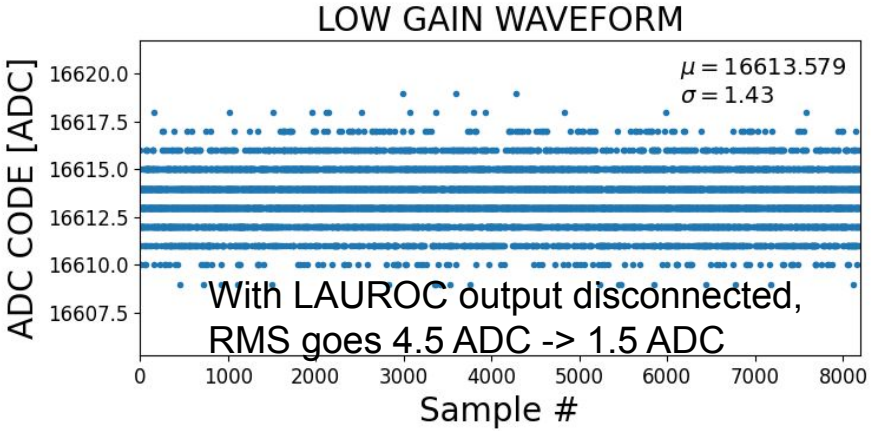


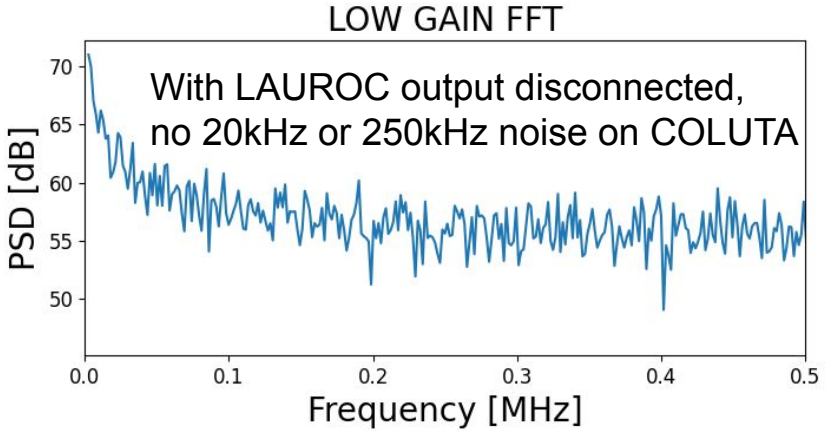
Correlation Plot, All Chs on Upper Board Half

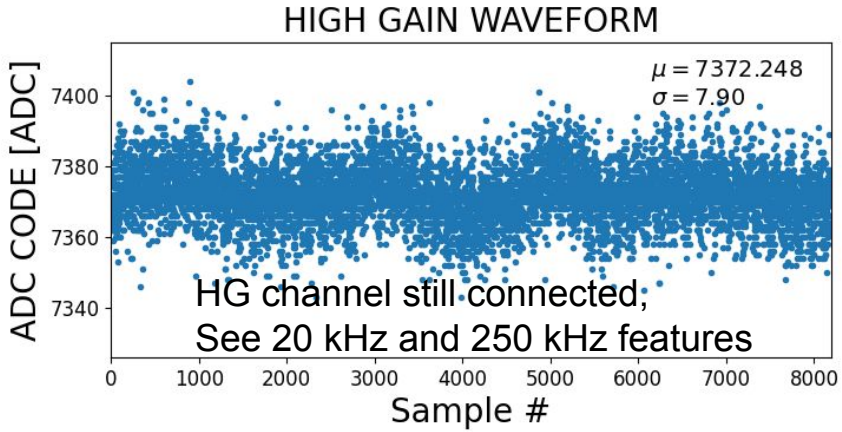


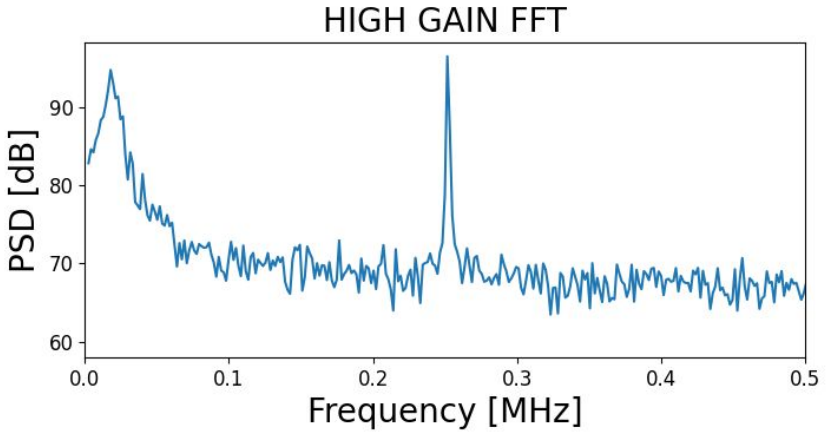
Noise Features Not Seen by COLUTA without LAUROC

Slice Testboard ch79: MDAC Chs
LG Ch Disconnected from LAUROC



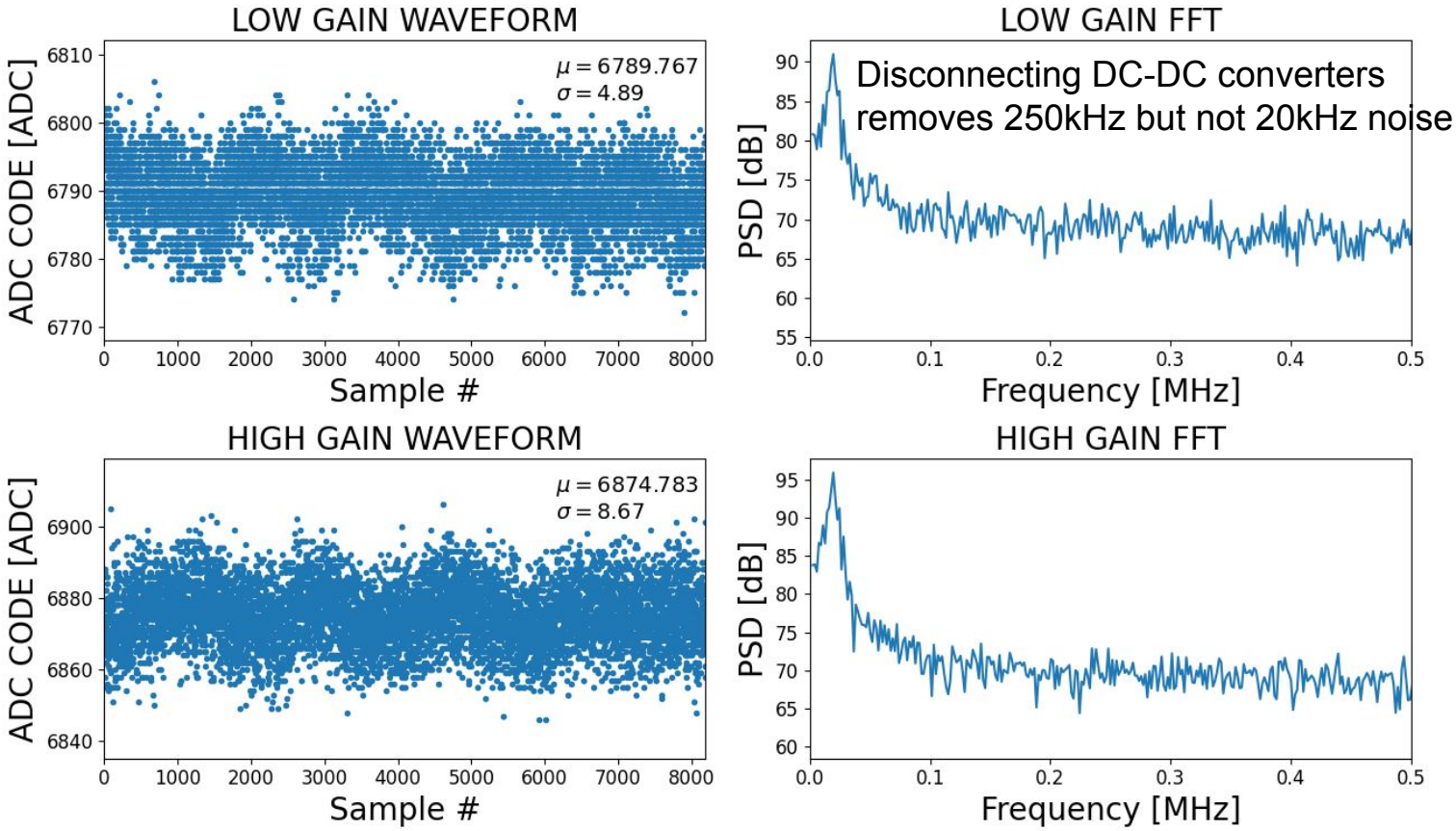






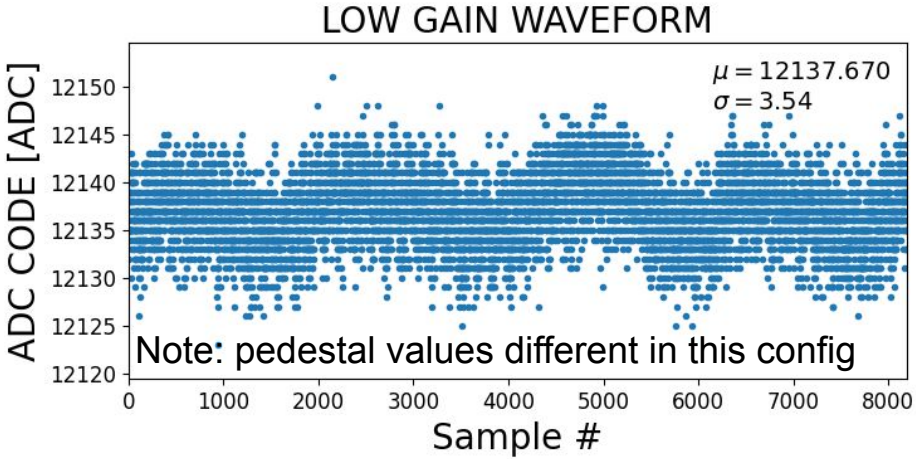
250kHz Noise Not Seen When Using External Linear PS (ie. DC-DC Converters Not Connected), but 20kHz Bump Remains

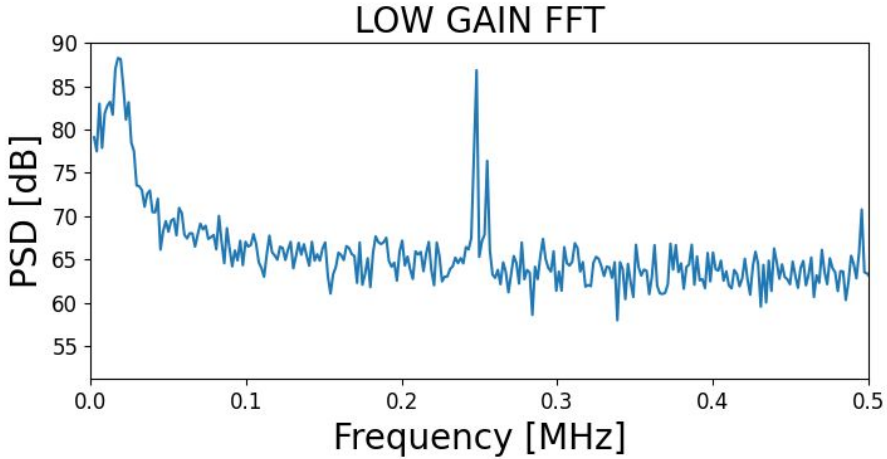
Slice Testboard ch79: MDAC Chs

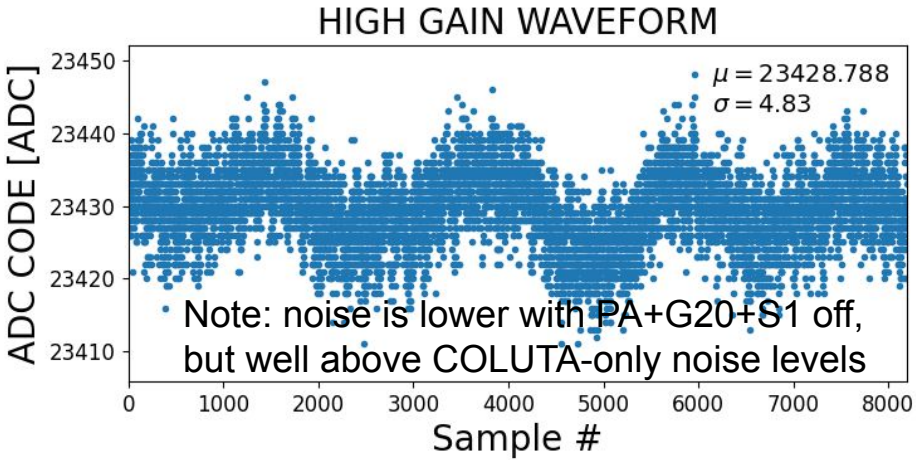


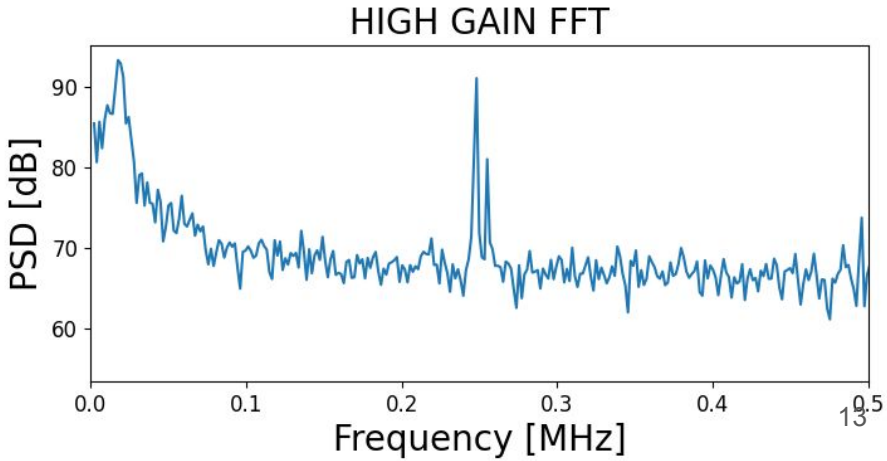
20kHz+250kHz Noise Remains with PA,G20,S1 Off

Slice Testboard ch79: MDAC Chs

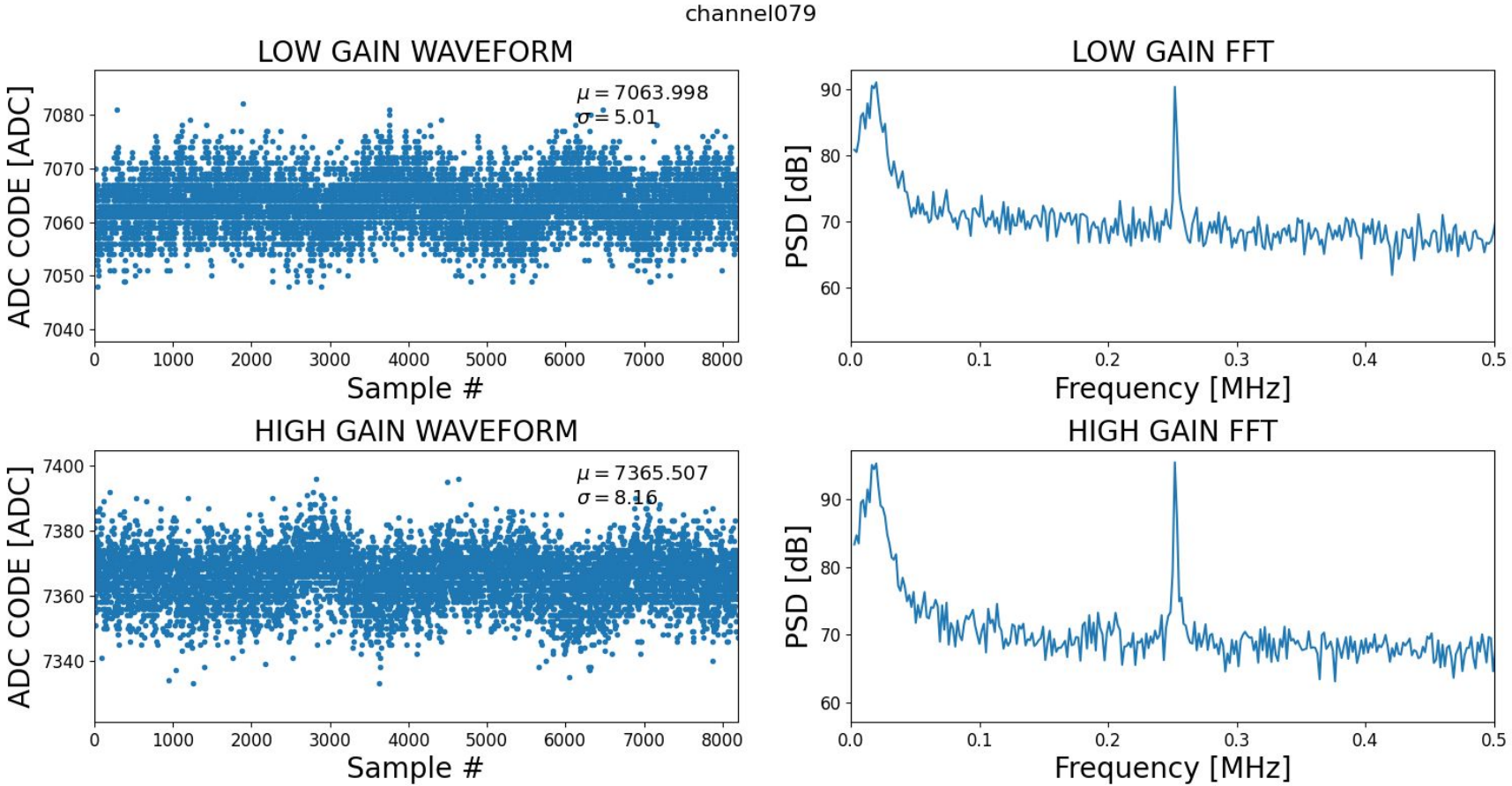






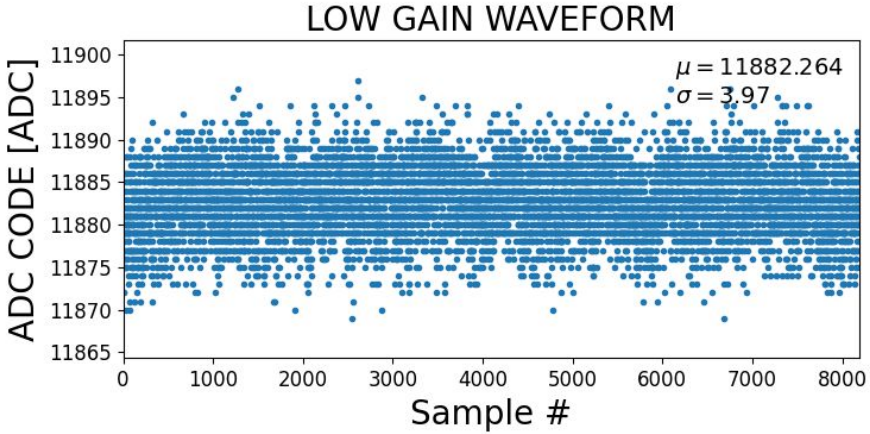


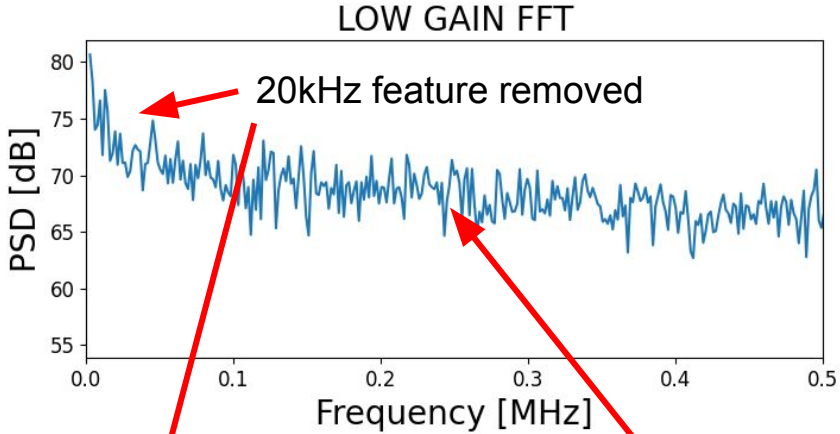
20kHz+250kHz Noise Remains with 50Ohm Resistors on LAUROC Outputs

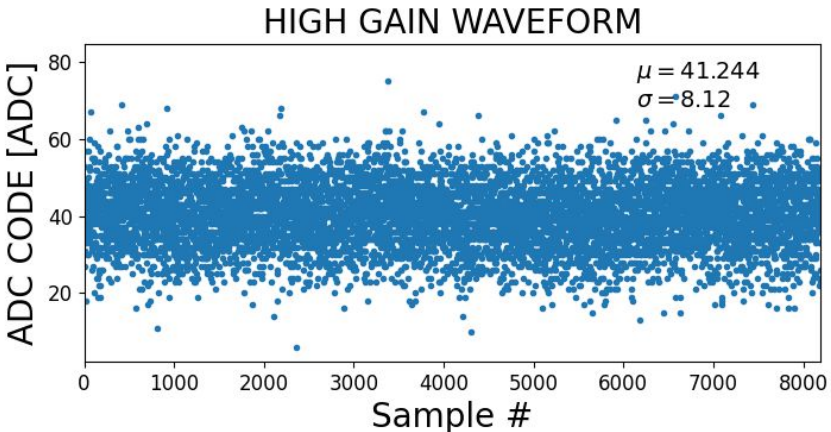


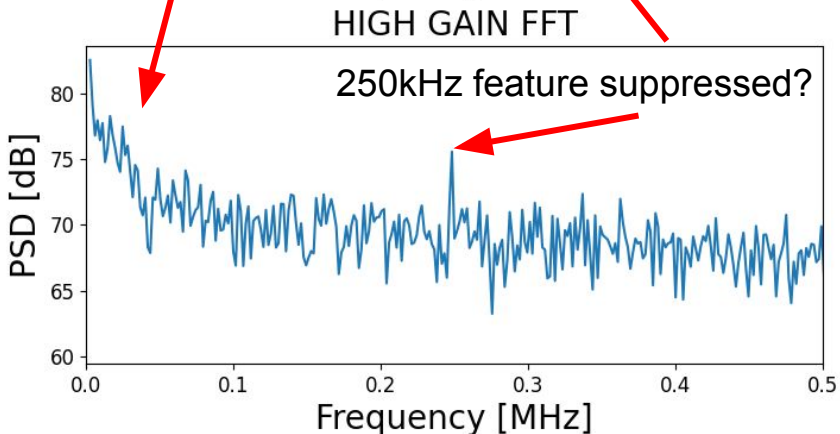
Setting DAC VDC LG/HG to Low Value Removes 20kHz Noise

Slice Testboard ch79: MDAC Chs
DAC VDC LG = 0, DAC VDC HG = 5



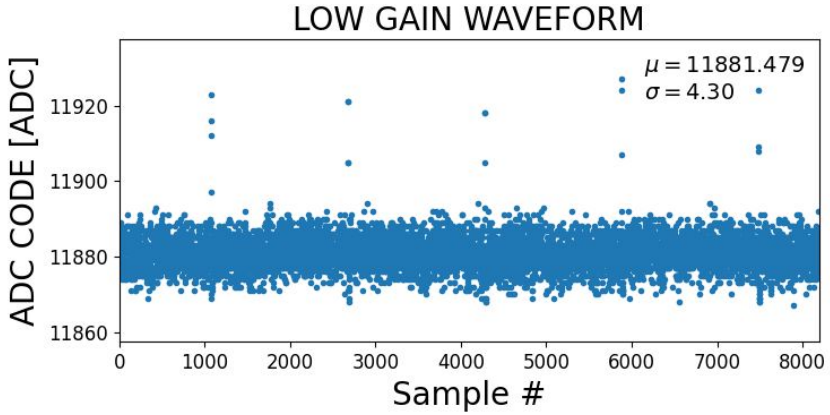


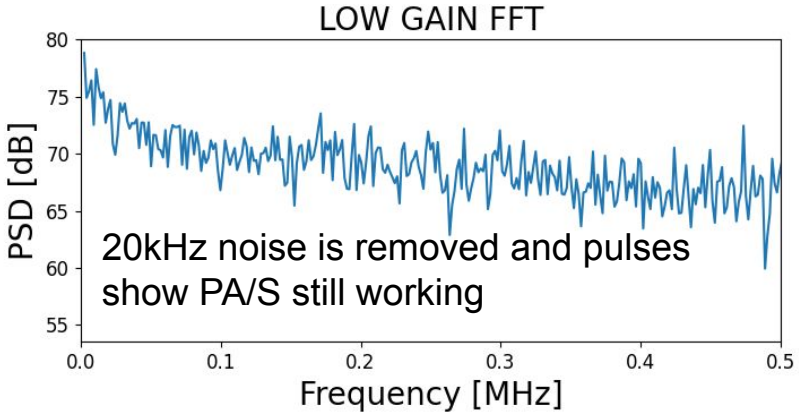


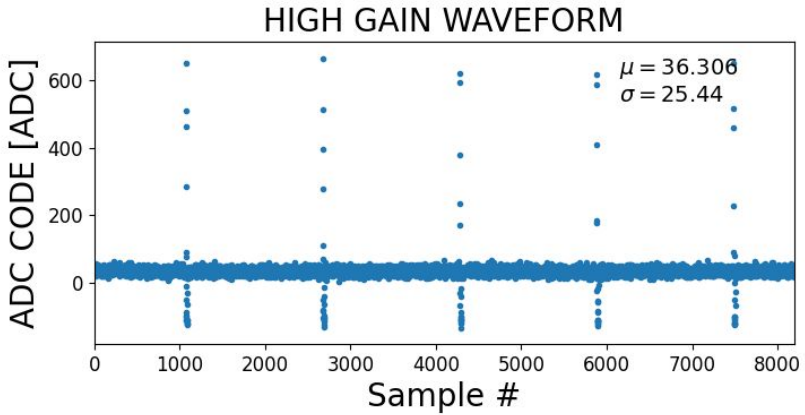


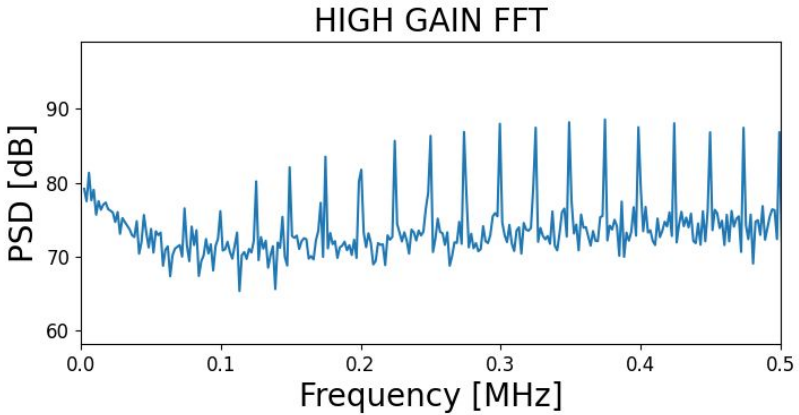
Pulse Signals Still Visible with Low DAC VDC (so PA/S still working)

Slice Testboard ch79: MDAC Chs
DAC VDC LG = 5, DAC VDC HG = 5

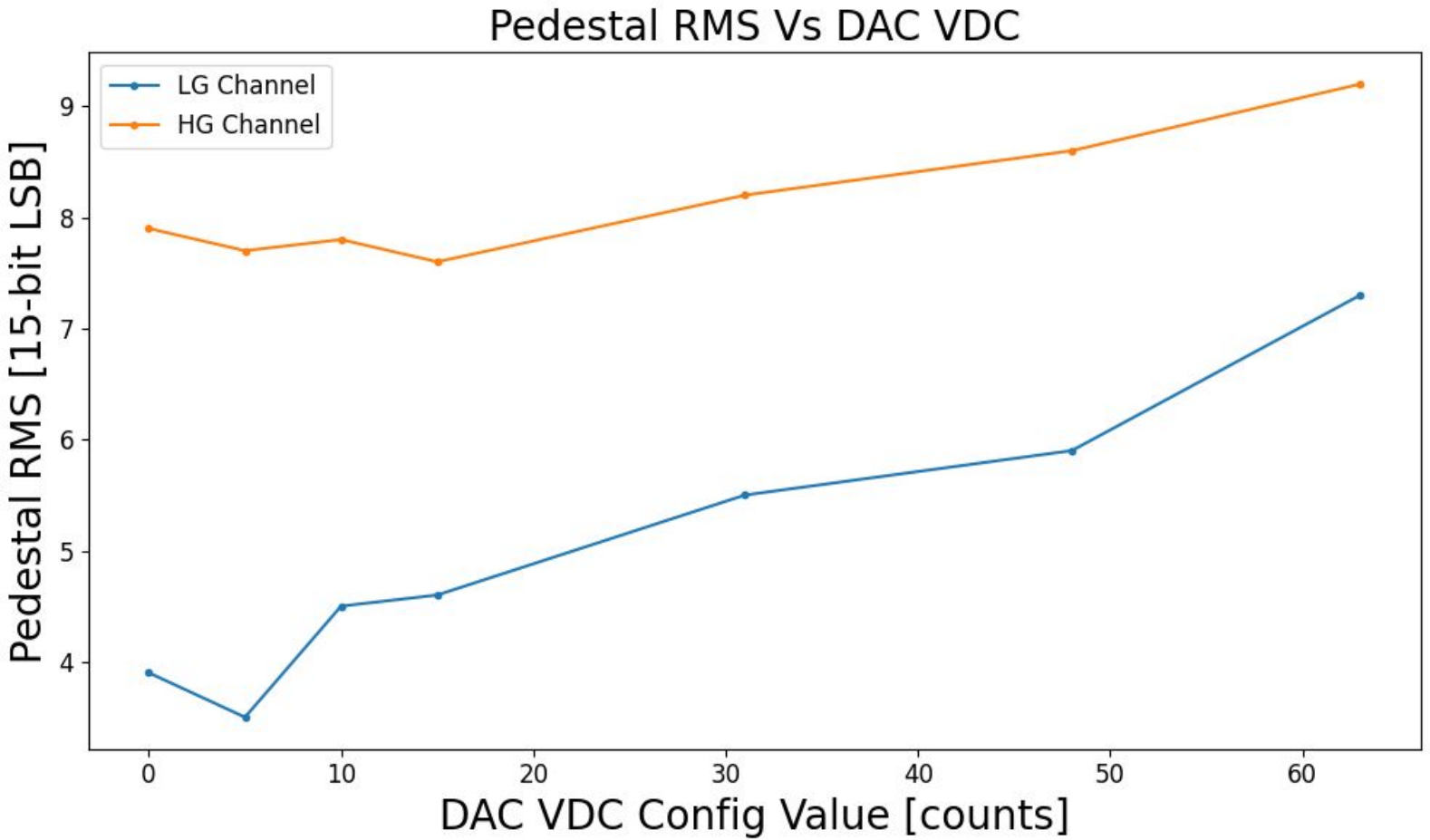






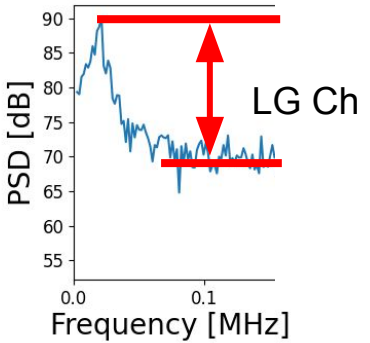


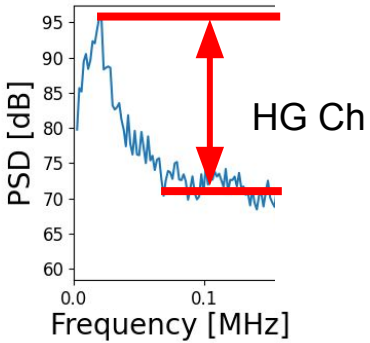
Measured Pedestal RMS Vs DAC VDC

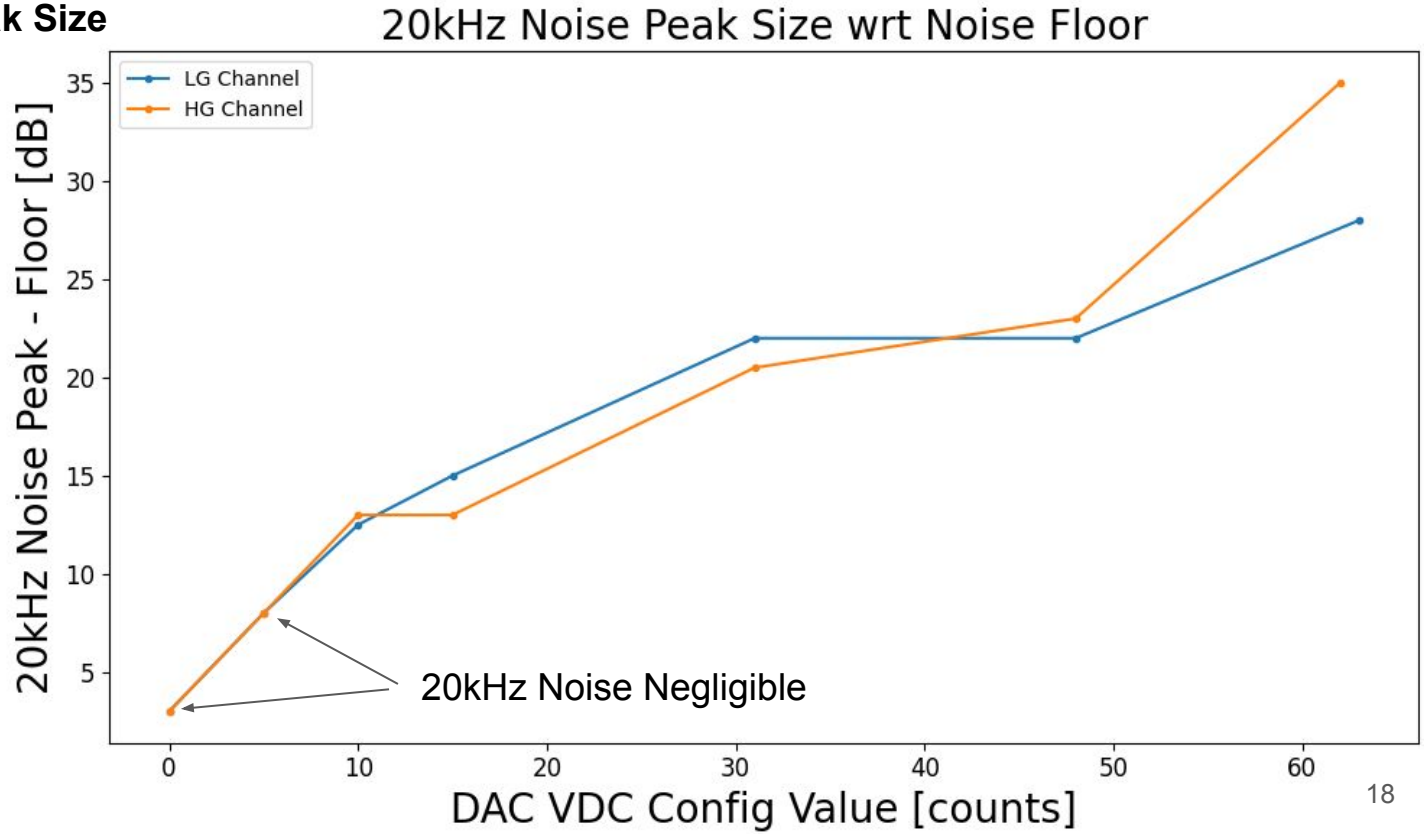


Measured 20kHz Noise Magnitude Vs DAC VDC

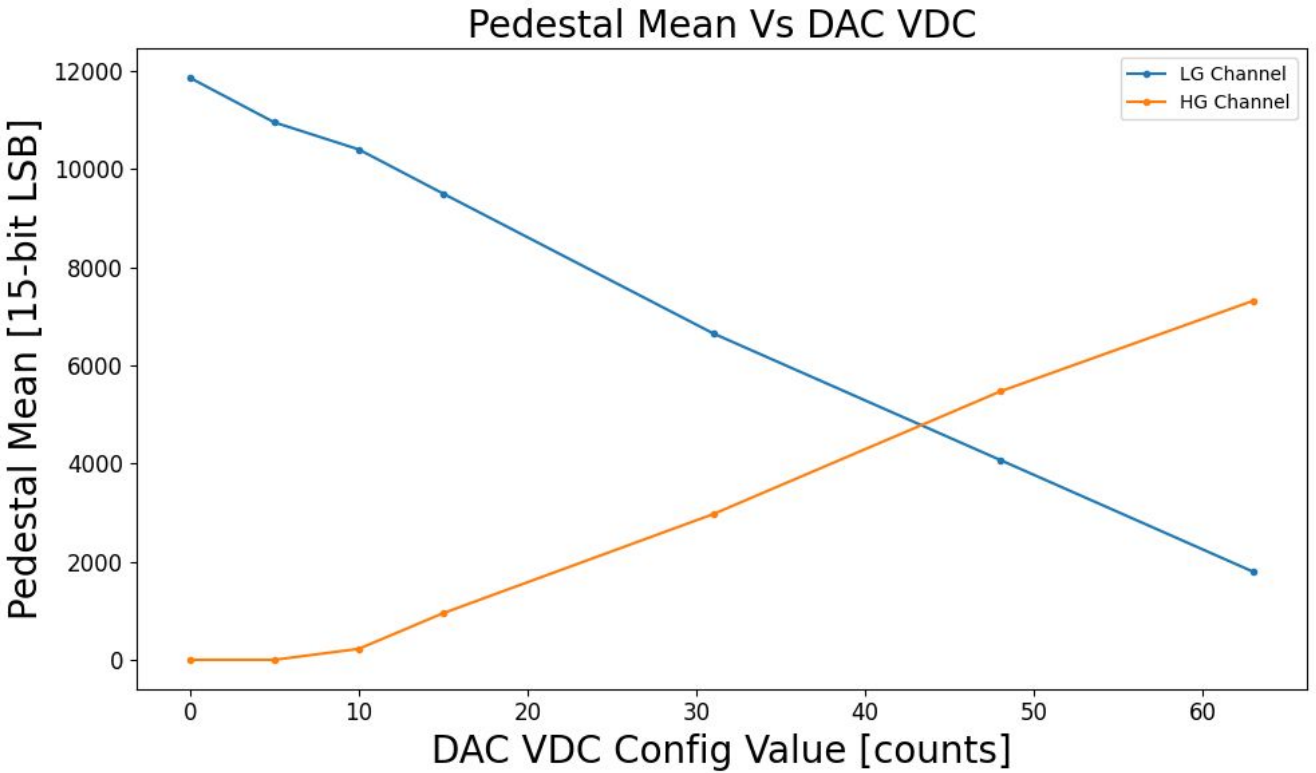
Measurement of 20kHz Peak Size wrt Noise Floor





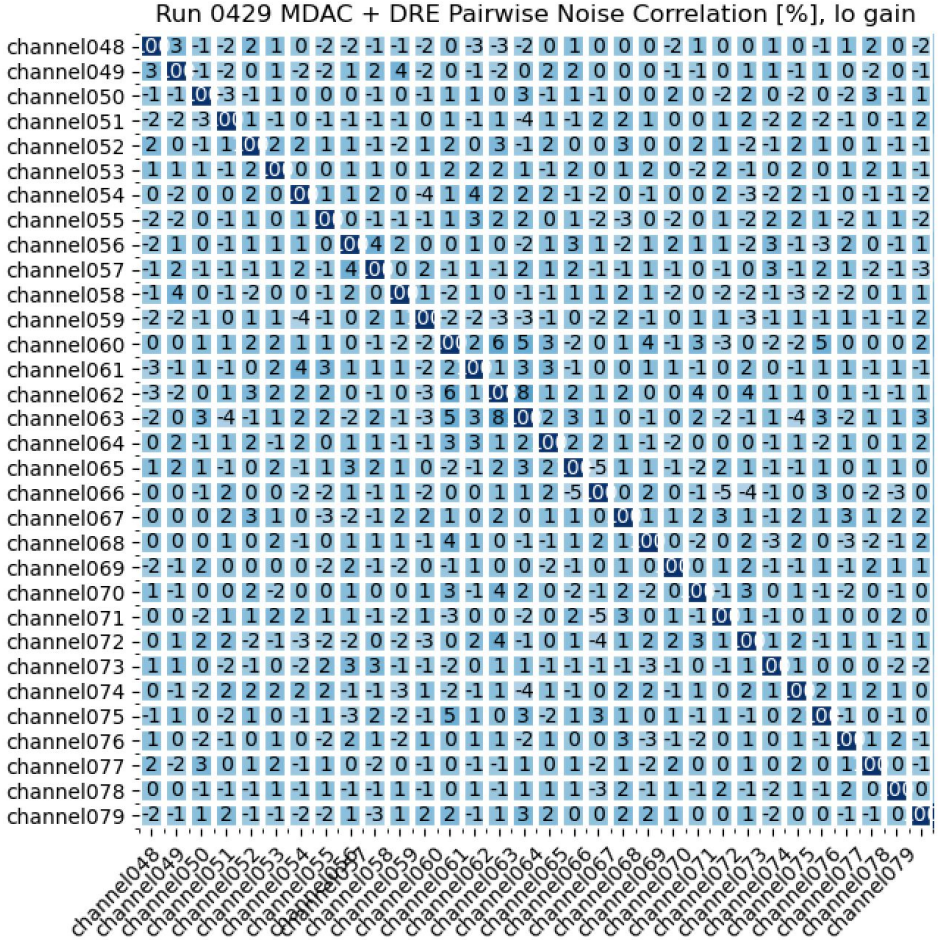


Pedestal Mean Vs DAC VDC

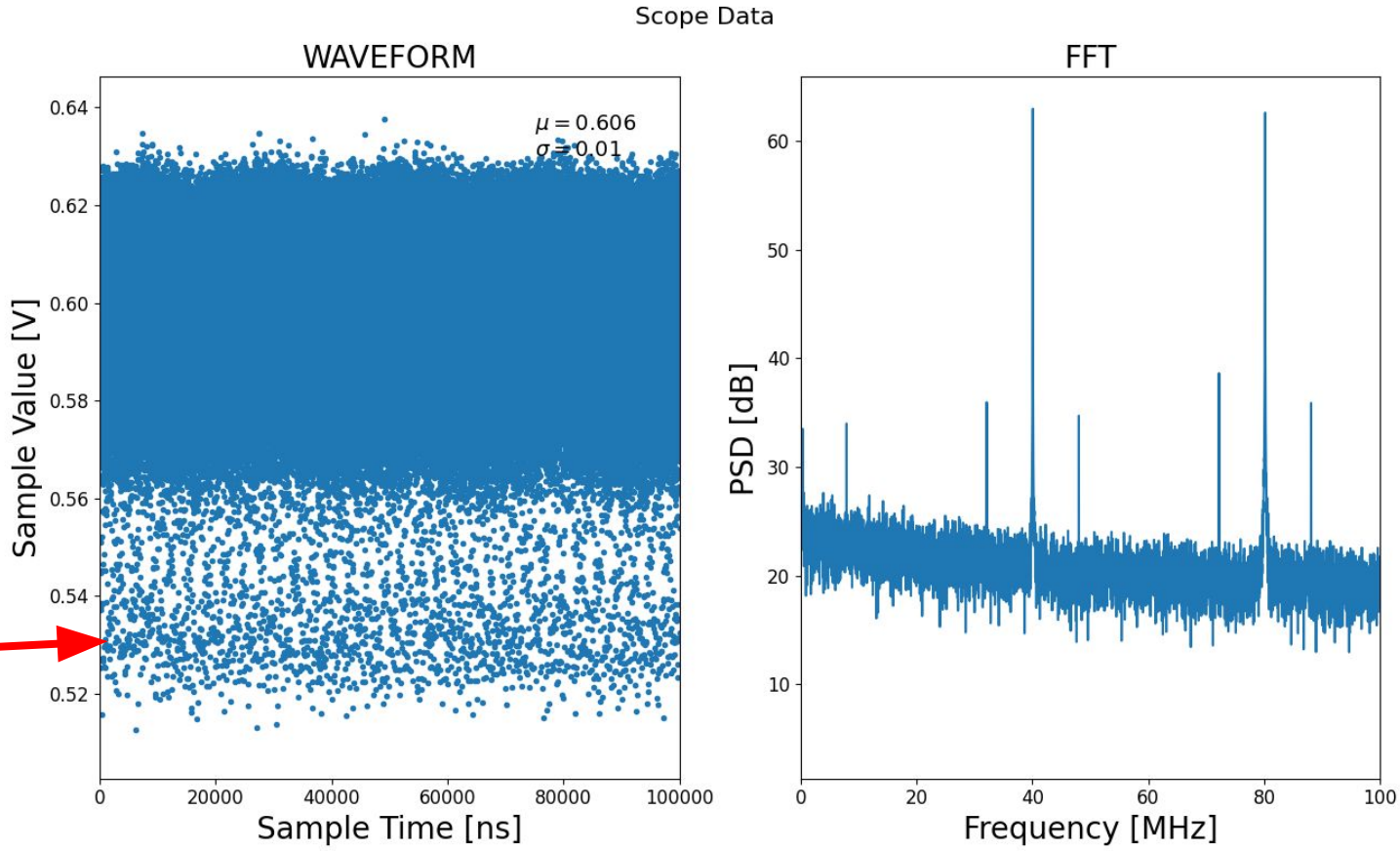


- Low gain and high gain channels vary differently wrt DAC VDC value
- Related to anti-correlated low gain and high gain 20kHz noise?

Correlated Noise <5% with Low DAC VDC

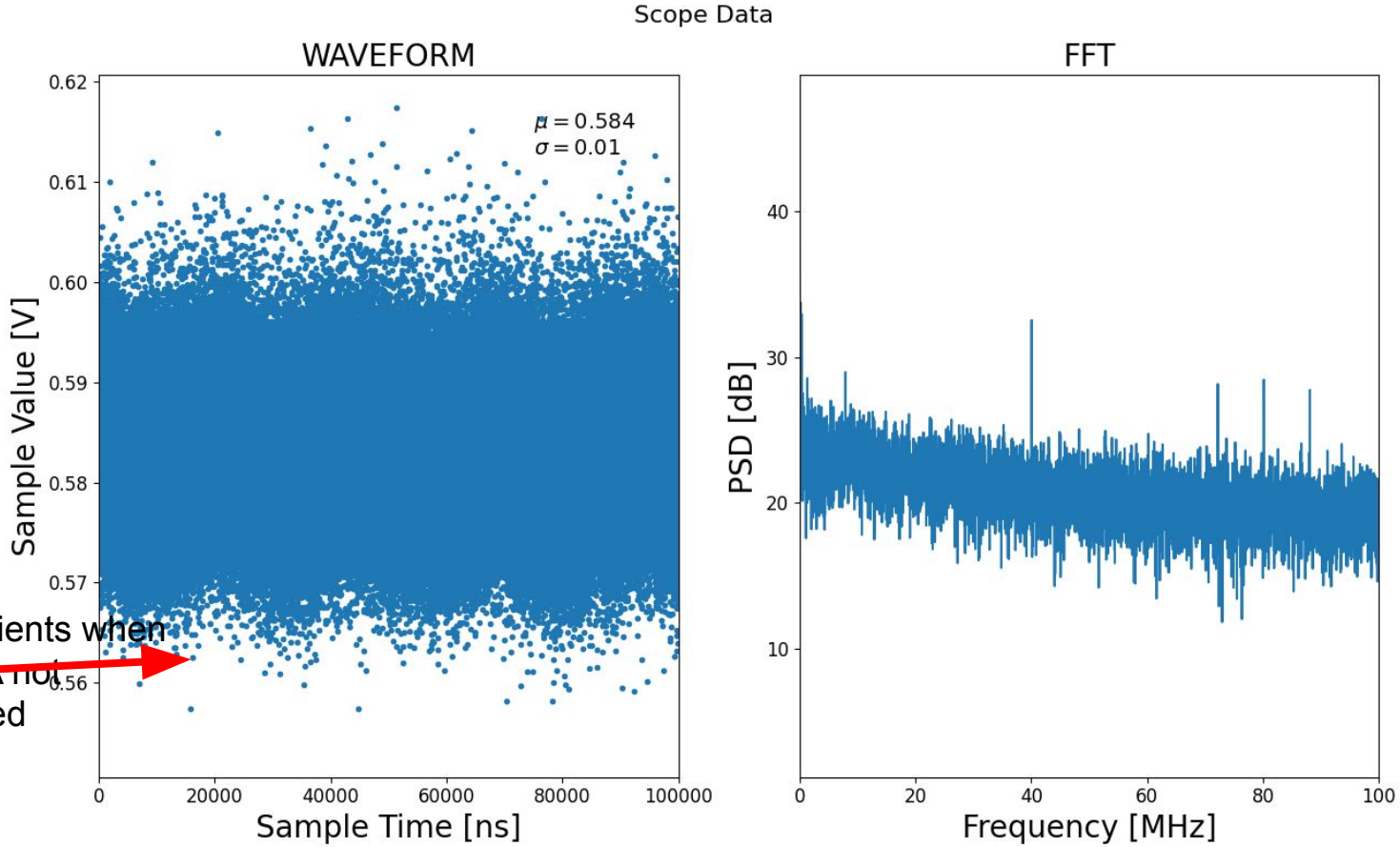


Probe LAUROC Outputs with Diff. Scope Directly, See Impact of 40MHz Sampling when COLUTA Connected



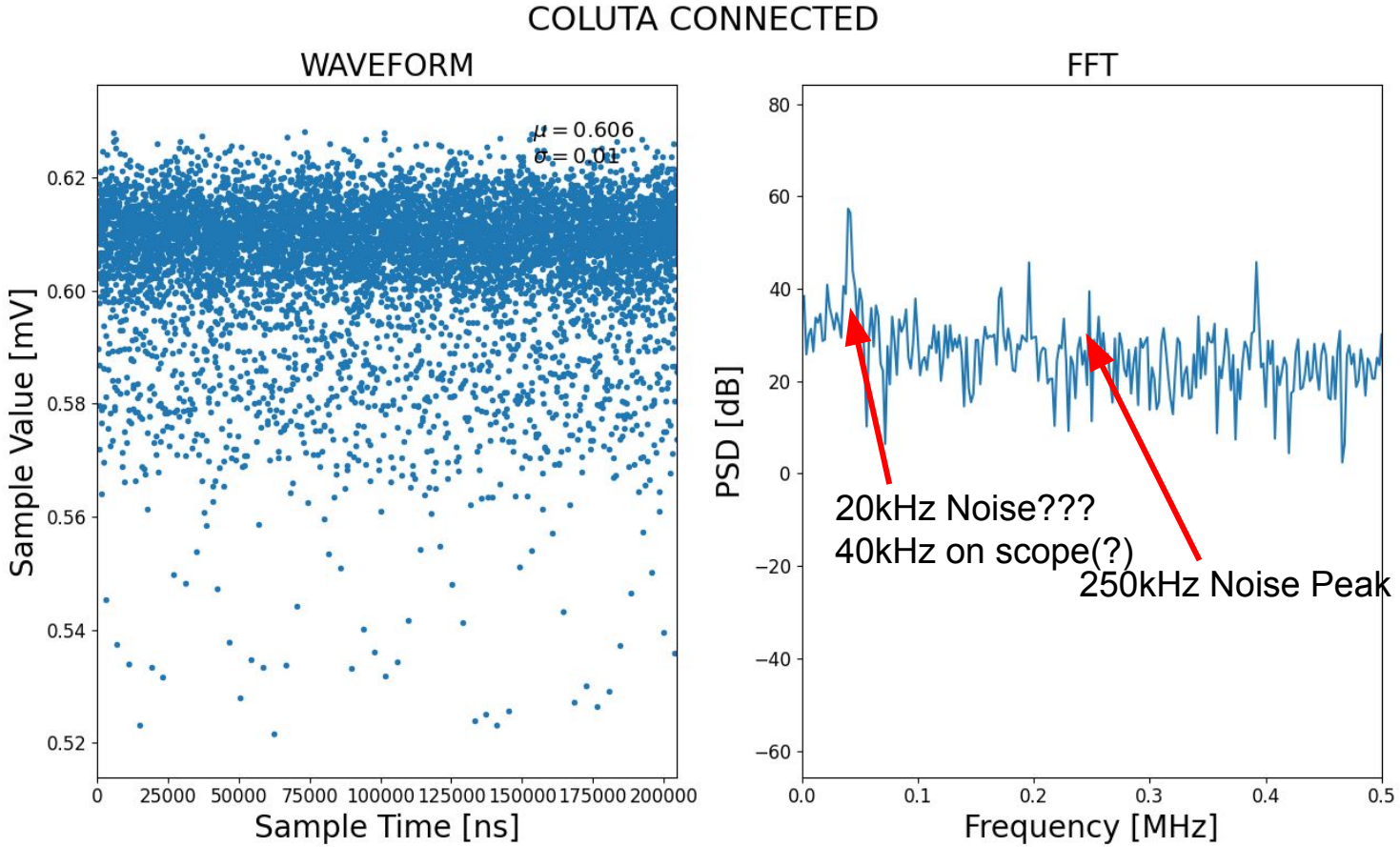
See transients every 25ns due to COLUTA sampling

Probe LAUROC Outputs with Diff Scope when no COLUTA Connected, Smaller 40MHz Impact

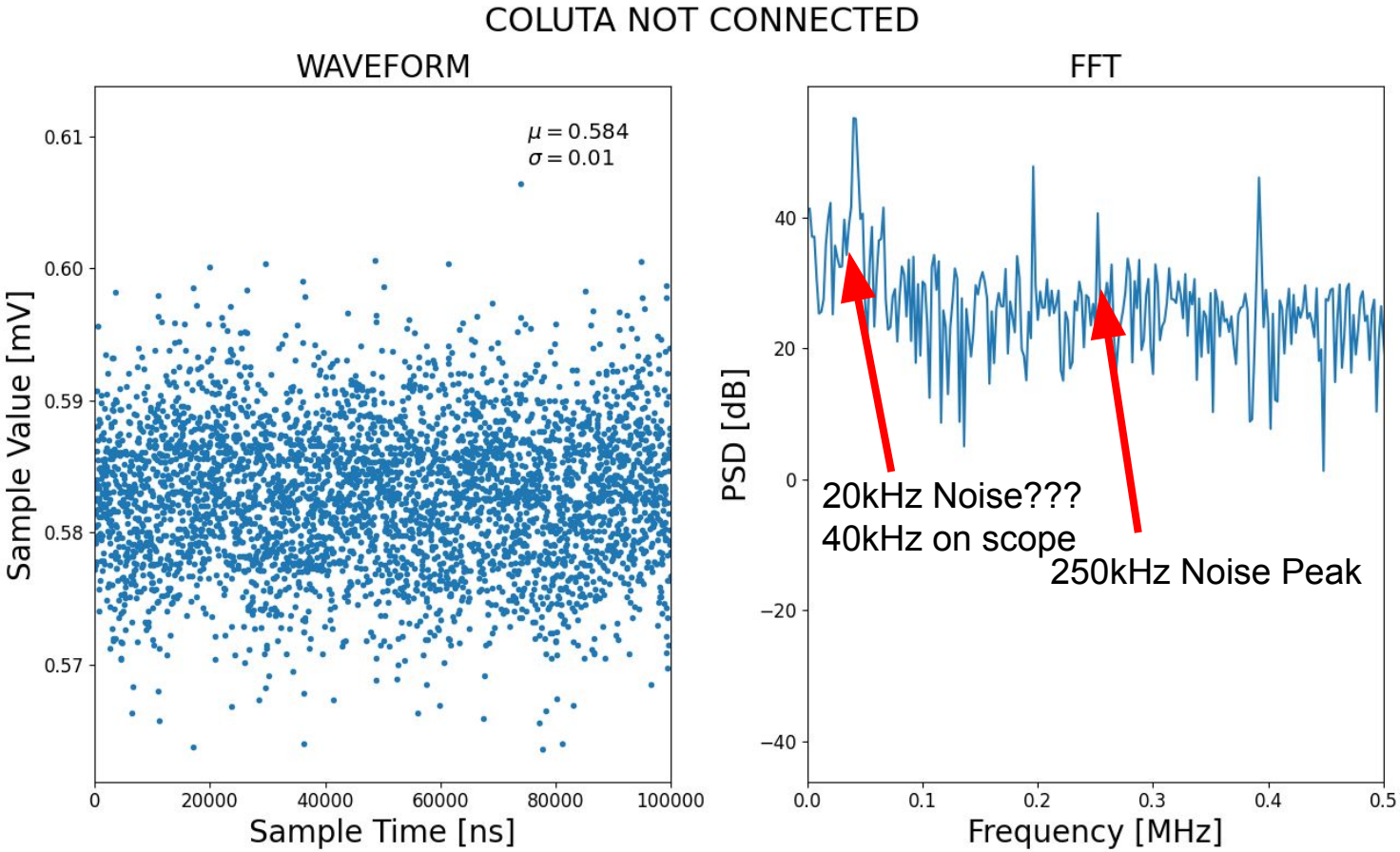


No transients when COLUTA not connected

250kHz+20kHz(?) Noise Visible on LAUROC Outputs with Diff. Scope and COLUTA Connected

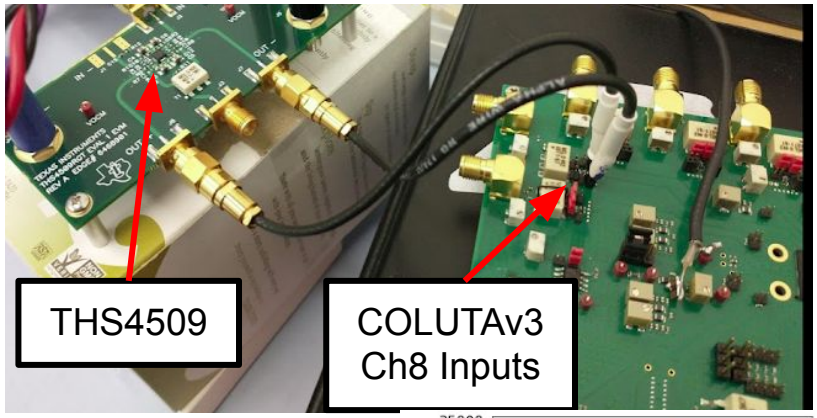


250kHz+20kHz(?) Noise Visible on LAUROC Outputs with Diff Scope and No COLUTA Connected

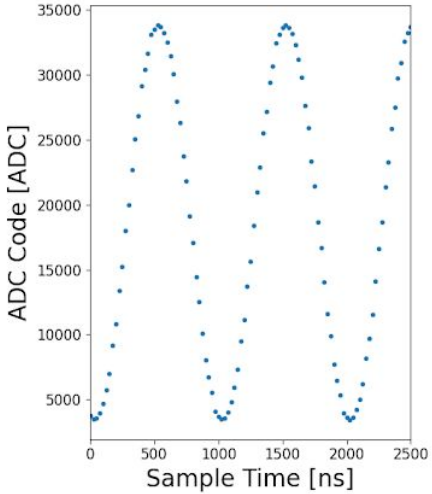


COLUTAv3 MDAC Input Driven by THS4509 PA

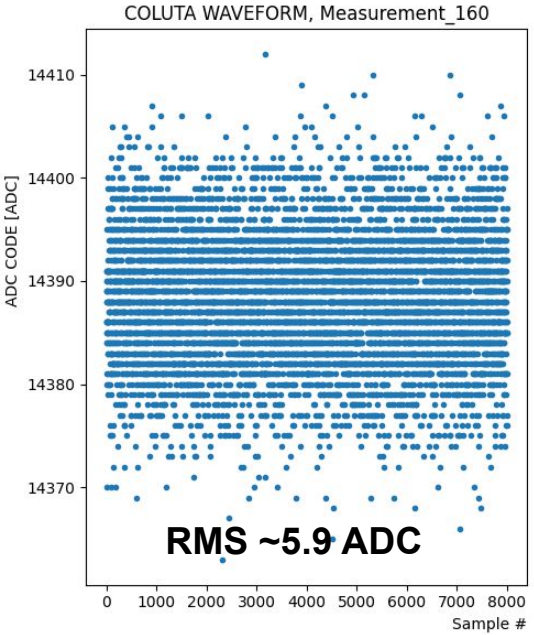
THS4509 injecting Sine Wave to COLUTA Ch

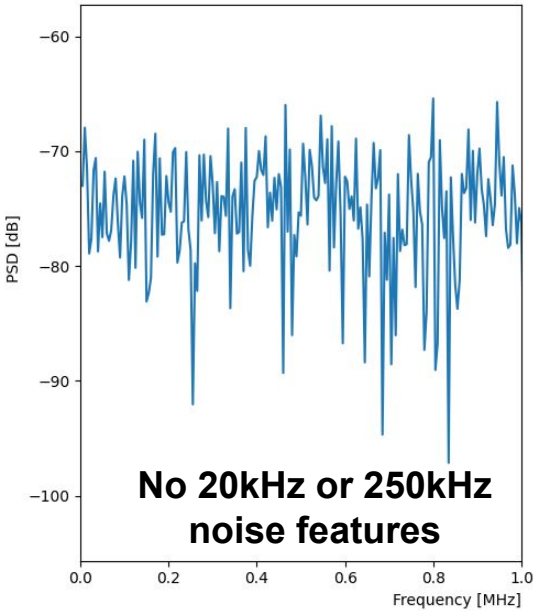


Example COLUTA Sampled Sine Wave Signal via THS4509



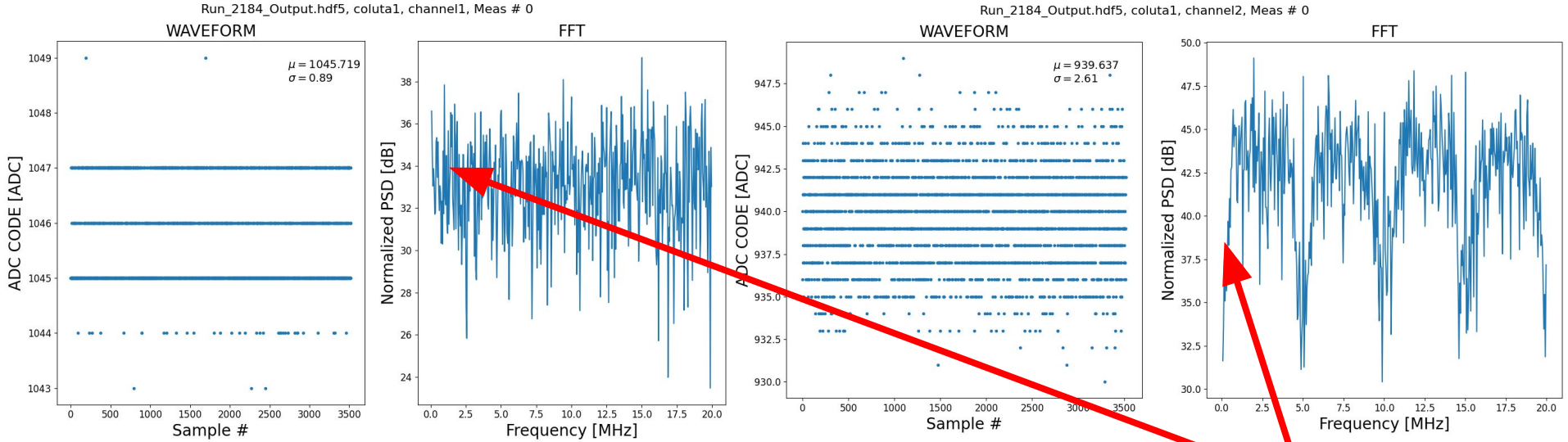
THS4509 into CV3 Board Ch8 Waveform+FFT





- Tried driving COLUTAv3 with THS4509 on Cv3 testboard as a comparison
- Do not see 20kHz “bump”

Reminder: Analog Testboard Noise Measurements



Config	LG, DRE 1x	HG, DRE 1x	LG, DRE 4x	HG, DRE 4x
Run #	2011	2011	2012	2012
Ped. RMS [ADC]	0.77	2.59 +/- 0.07	2.30 +/- 0.30	10.52 +/- 0.17

No 20kHz bump

1x LG noise lower on analog testboard vs Slice Testboard DRE Chs (0.77ADC vs 1.5ADC)

- Analog Testboard used LAUROC1 + COLUTAv2 (all DRE chs)
  - For COLUTAv2 only difference was using DRE channels with larger input capacitance
- No obvious 20 kHz “bump” in FFTs, correlated noise < 5%

Summary of Slice Testboard Noise Issues

- Pedestal noise measurements with Slice Testboard (that uses 8 LAUROC2 chips connected to 8 COLUTAv3 ADC chips) show some issues:
  - Individual channels seem significantly noisier than expected (particularly apparent for LO gain)
  - Coherent noise across channels is significantly higher than <5% specification and what was achieved previously with Analog Testboard (using LAUROC1 and COLUTAv2)
- Two main noise features observed: 250kHz line and 20kHz “bump”
- **250kHz noise** from onboard DC/DC converters
  - COLUTA channel not connected to LAUROC does not see 250kHz noise
  - Can be removed using external PS
  - Scope shows 250kHz noise on LAUROC outputs, even when COLUTA not connected
- **20kHz noise:**
  - Appears to be correlated across board halves
  - Opposite phase between LG and HG channels
  - COLUTA channel not connected to LAUROC does not see 20kHz noise
  - Not removed using the external PS
  - Noise remains when PA, G20 and S1 disabled
  - Not removed by adding 50Ohm series resistors to LAUROC outputs
  - Can be removed by adjusting LAUROC DAC VDC HG/LG to low values ie. <5 counts
  - Scope might show 20kHz noise on LAUROC outputs, even with COLUTA disconnected (???)
  - Not seen in Analog Testboard or Cv3 testboard + THS4509 sampled waveforms

Some questions for PA/S team

- For open input (or for some fixed Cdet), what are the measured and expected LAUROC noise levels (in muV) at output of HI and LO gain shapers?
- Do you see 20 kHz noise feature on your dedicated LAUROC (or ALFE) testboards?
  - If not, do you think your measurements would be sensitive to its presence?
  - What ADC are you using to digitize the PA/S output signals?
- Have you measured LAUROC output noise as a function of the DAC VDC used to set the shaper output baseline voltage?
- Is anti-correlation between HI and LO 20 kHz noise related to the fact that DAC VDC value moves HI and LO baseline voltages in opposite directions?
- Any ideas about source of (20 kHz) correlated noise, and how to mitigate and/or remove it?
- What would these results imply with regard to expectations for ALFE2?

BACKUP

From March 2021 LAr-Week:

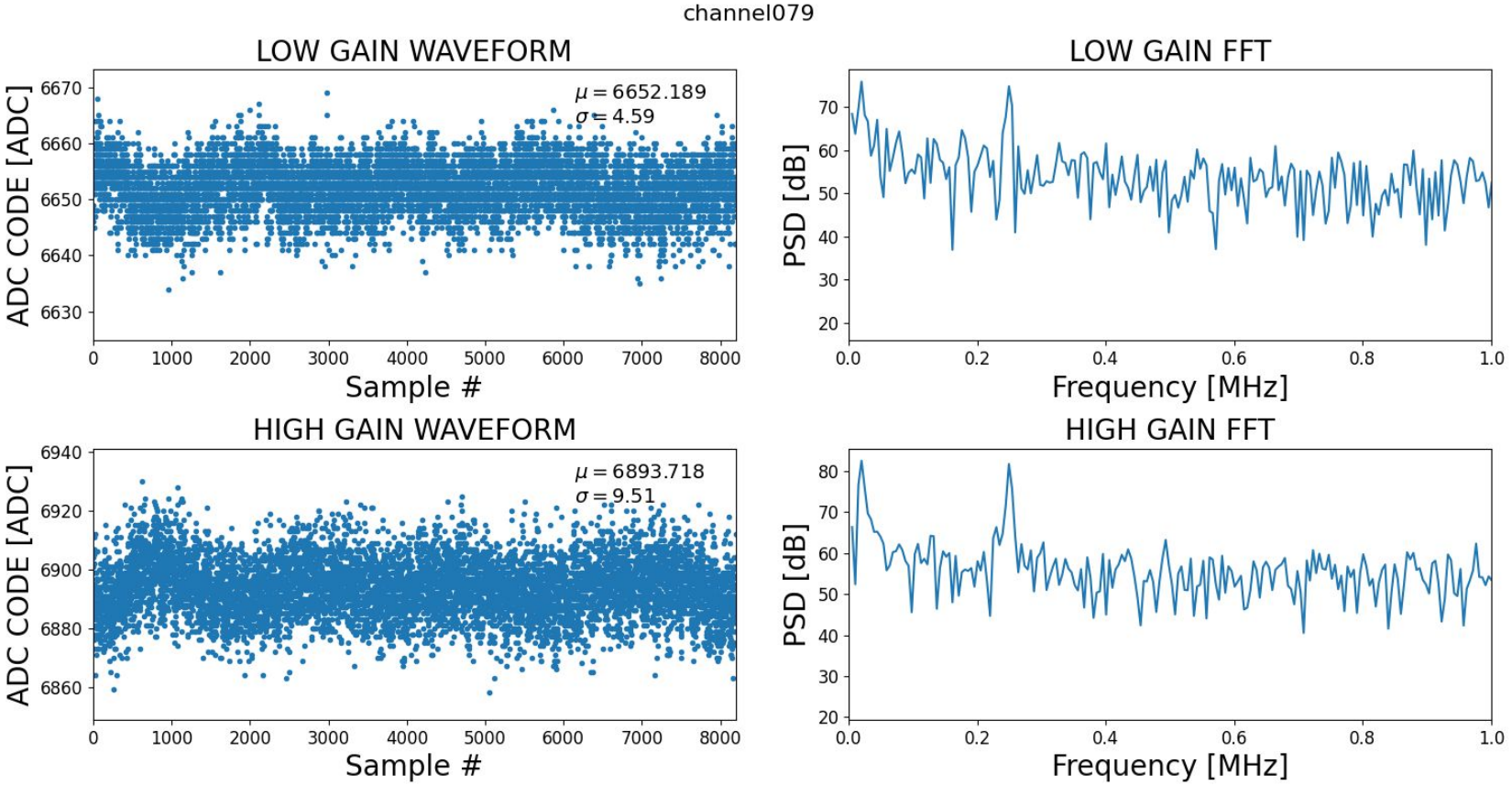
Investigating 20 kHz Noise

We have so far tried a number of modifications to the board to see if we could isolate the source of the 20 kHz noise:

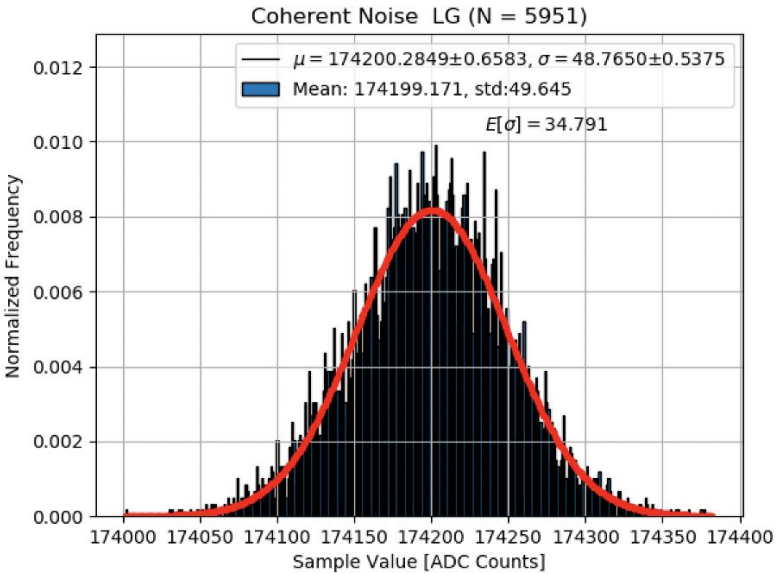
- Adding a Faraday cage over the input connectors
- Adding a Faraday cage over the preamps
- Shorting the signal input pins
- Disabling the PA/S 40 MHz clock
- Removing the AC-coupling capacitor in the input protection networks, in order to disconnect the PA/S input
- Partially disabling the preamp
  - ON_pa=0, ON_g20=1, ON_lg_s1=1, ON_hg_S1=1, ON_lg_s2=1, ON_hg_s2=1
  - ON_pa=0, ON_g20=0, ON_lg_s1=1, ON_hg_s1=1, ON_lg_s2=1, ON_hg_s2=1
  - ON_pa=0, ON_g20=0, ON_lg_s1=0, ON_hg_s1=0, ON_lg_s2=1, ON_hg_s2=1

The 20kHz noise remained roughly consistent through all these tests

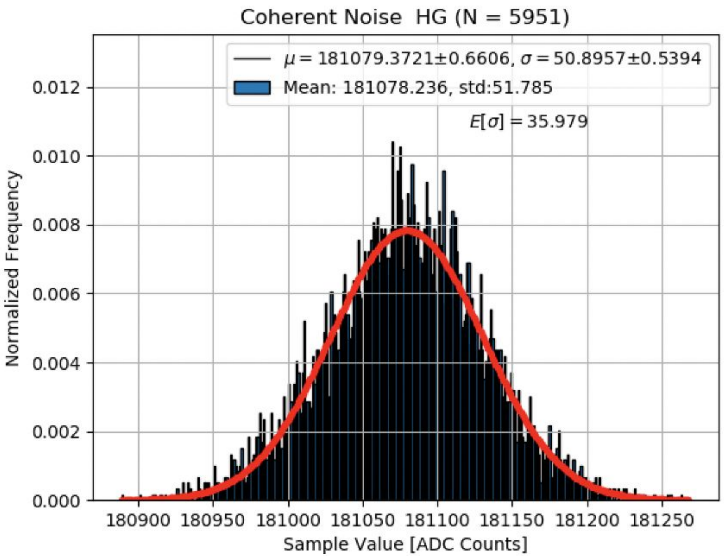
Slice Testboard Noise Features, 8192 Sample Readout



Correlated Noise Measurement

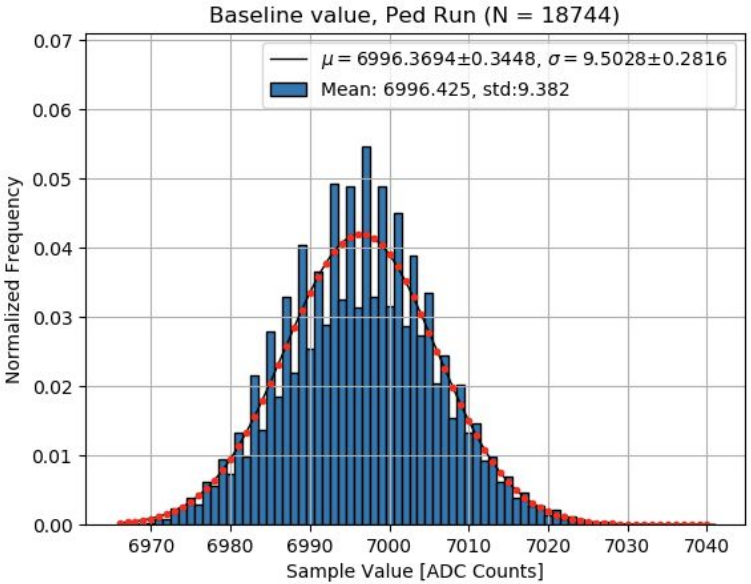


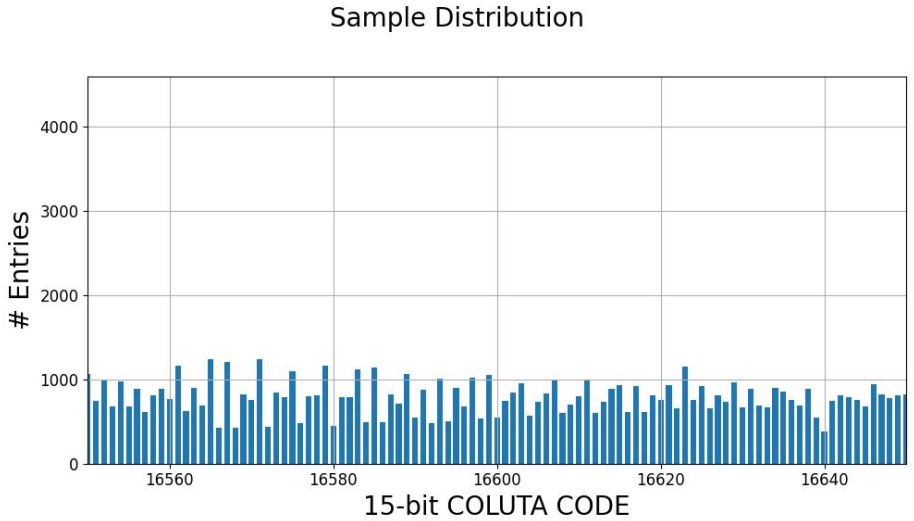
Sqrt(sig^2 – E[sig]^2) = 34.2 cts



Sqrt(sig^2 – E[sig]^2) = 36.0 cts

Even/Odd Effect, Not Related to 250kHz/20kHz Noise





20kHz Noise Appears When DAC VDC > 5 Counts

DACB HG	DACB LG	Run	HG BL [ADC]	LG BL [ADC]	HG RMS [ADC]	LG RMS [ADC]	LG 20kHz Noise Peak wrt Noise Floor	HG 20kHz Noise Peak wrt Noise Floor
62	32	310	7190	6570	9.0	5.2	25dB	35dB
0	0	313	Underflow	11860	7.9	3.9	3dB	3dB
5	5	326	Underflow	10952	7.7	3.5	8dB	8dB
10	10	324	223	10400	7.8	4.45	12.5dB	13dB
15	15	315	950	9500	7.6	4.6	15dB	13dB
31	31	317	2970	6650	8.2	5.5	22.1dB	20.5
48	48	319	5470	4070	8.6	5.9	22B	23dB
63	63	322	7320	1790	9.2	7.3	28dB	28dB

Noise Features Remain with LAUROC Clocks OFF