COLUTA to LpGBT mapping

Jaroslav Bán

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

COLUTA outputs(1)

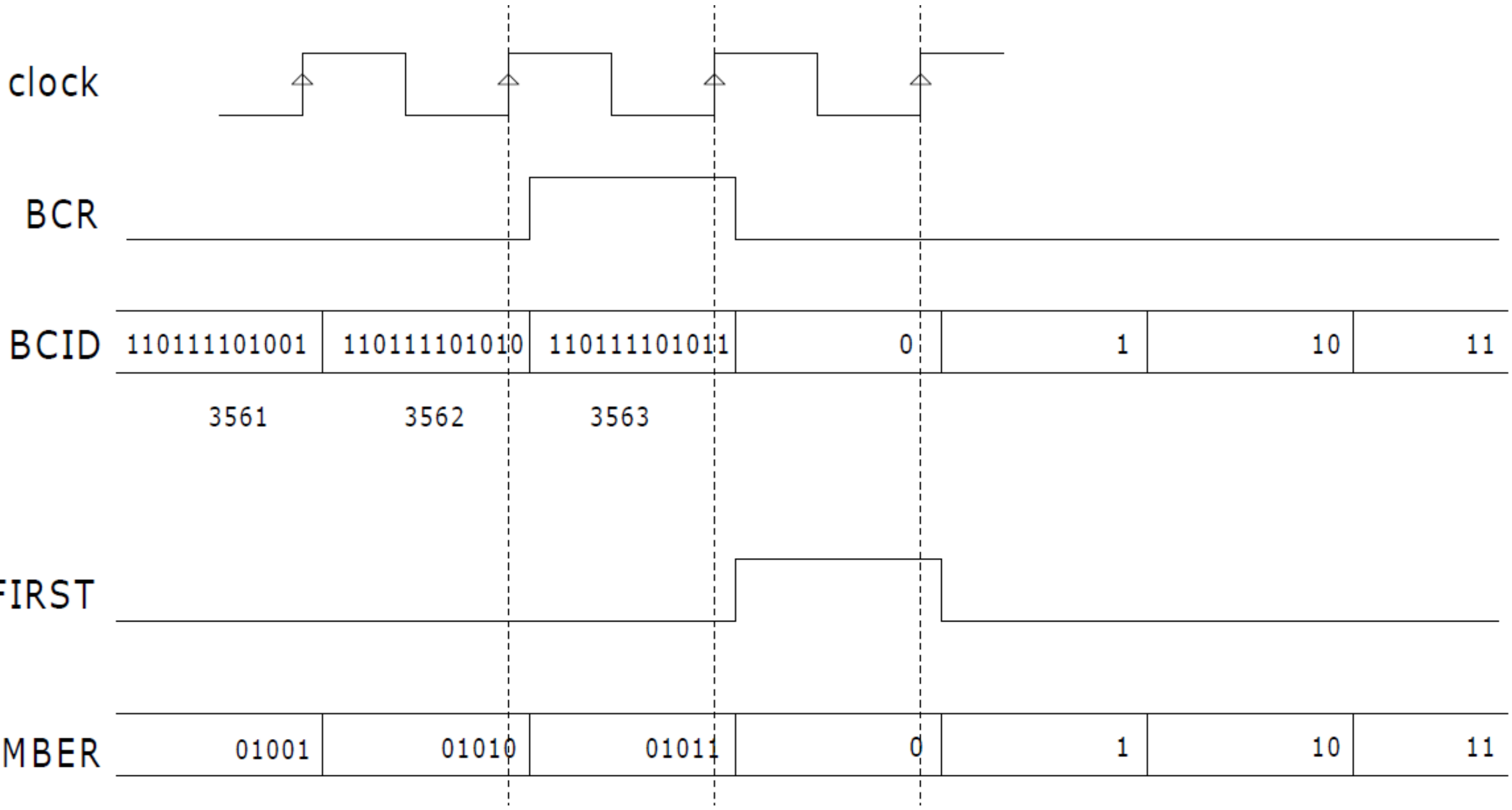
COLUTA ADC outputs data on 10 serial data lines
at the speed of 640MHz.

They are:
-F1
-Data1 – Data8
-F2

F1&F8 format is always: {1’b1, 1’b0, FIRST, BCNUMBER[4:0],8h00}
Datax format in a normal mode is: {OVR,ADC_COUNT[14:0]} ***

***Formats of Data lines are described in COLUTAV3 datasheet
Some of them are discussed in the back-up slides below

Frame signals timing



COLUTA outputs(2)

LpGBT chip strobes the user data into its own data frame structure without knowing what is the user data frame (MSB position).

In order to align COLUTA data with LpGBT data boundaries, COLUTA has to have

-the way to uniquely detect its own data frame format (Done by Fx format {1,0,xxxxxx,0000000}.)

-have the mechanism to adjust the data in terms of 640MHz ticks

(Done by an extra hardware at the backend of COLUTA. Controlled by I2C.)

LpGBT uplink frame structure

We expect the LpGBT working in FEC5 mode and at 10.24Gbps speed.

User data mapped to the I/O lines are Data[223:0].

The goal of this document is to describe the mapping between Data[223:0] and COLUTA data.

This mapping are done through connection between COLUTA data lines and LpGBT I/O group lines

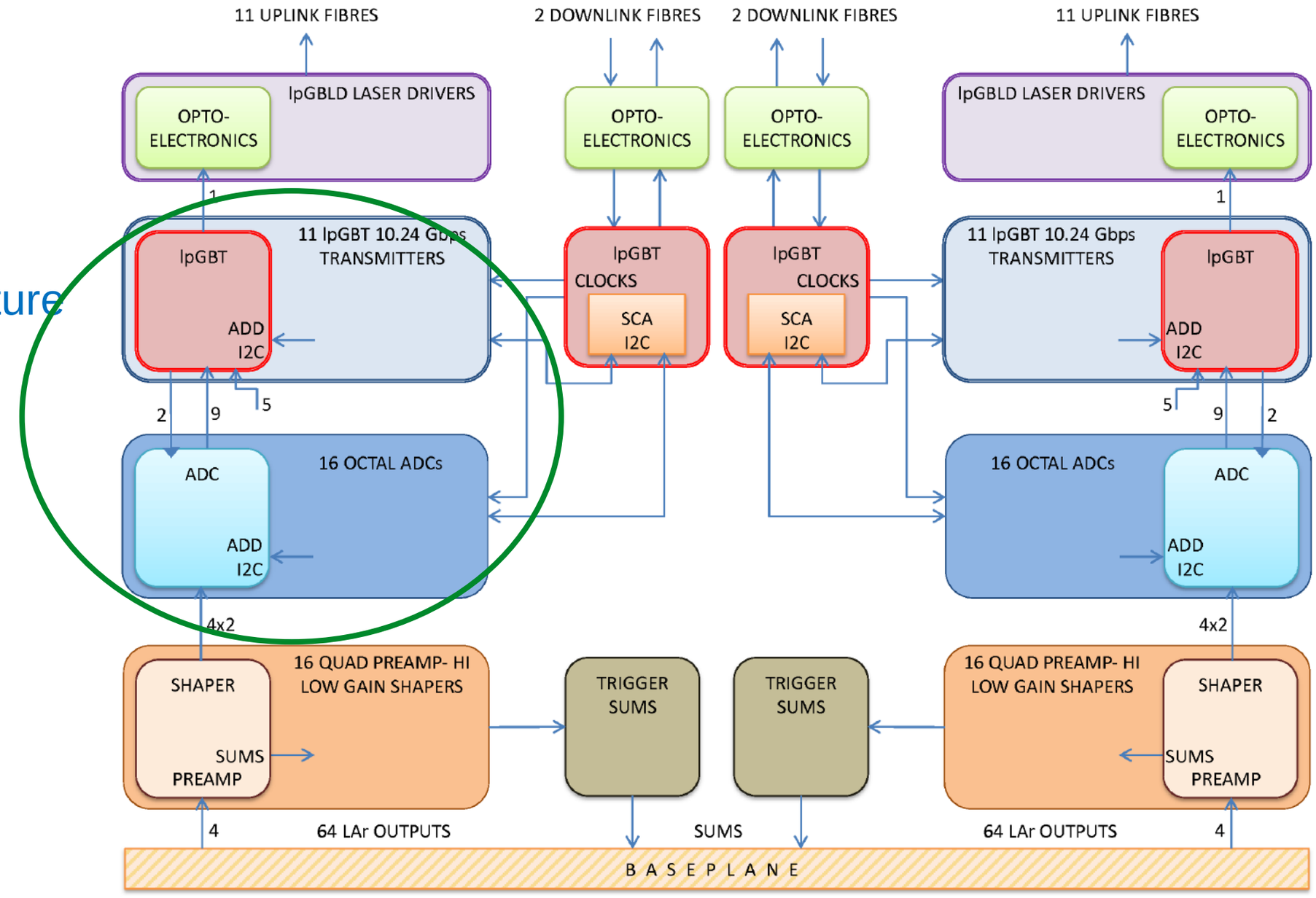
Frame	Function	I/O Group
FRMUP[9:0]	FEC[9:0]	
FRMUP[19:10]	FEC[19:10]	
FRMUP[35:20]	Data[15:0]	0
FRMUP[51:36]	Data[31:16]	0
FRMUP[67:52]	Data[47:32]	1
FRMUP[83:68]	Data[63:48]	1
FRMUP[99:84]	Data[79:64]	2
FRMUP[115:100]	Data[95:80]	2
FRMUP[131:116]	Data[111:96]	3
FRMUP[147:132]	Data[127:112]	3
FRMUP[163:148]	Data[143:128]	4
FRMUP[179:164]	Data[159:144]	4
FRMUP[195:180]	Data[175:160]	5
FRMUP[211:196]	Data[191:176]	5
FRMUP[227:212]	Data[207:192]	6
FRMUP[243:228]	Data[223:208]	6
FRMUP[249:244]	{4'b0, DownIC[1:0]}	See text
FRMUP[251:250]	EC[1:0]	
FRMUP[253:252]	IC[1:0]	
FRMUP[255:254]	H[1:0]	HFH[1:0] = 2'b10

10.24 Gbps - FEC5 uplink frame structure (before interleaving)

FEB2 big picture

Baseline for FEB2 architecture proposes to connect

16 ADC's
to
11 LpGBT chips

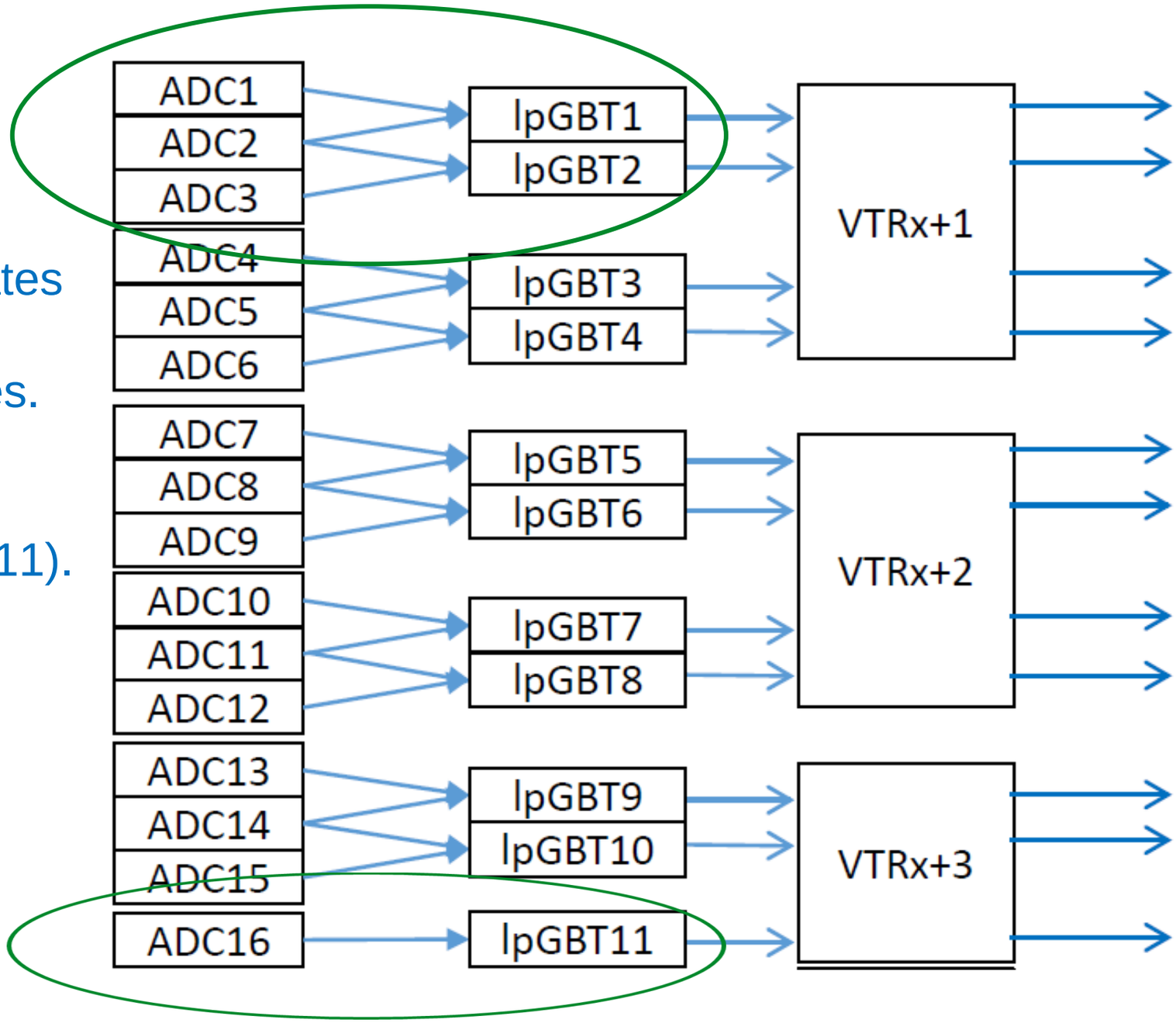


Half FEB2 big picture

The mapping of
16 ADC's to 11 LpGBT chips translates into
repeating 3ADC to 2LpGBT structures.

Also an extra structure will appear:
1ADC to 1LpGBT (ADC16 to LpGBT11).

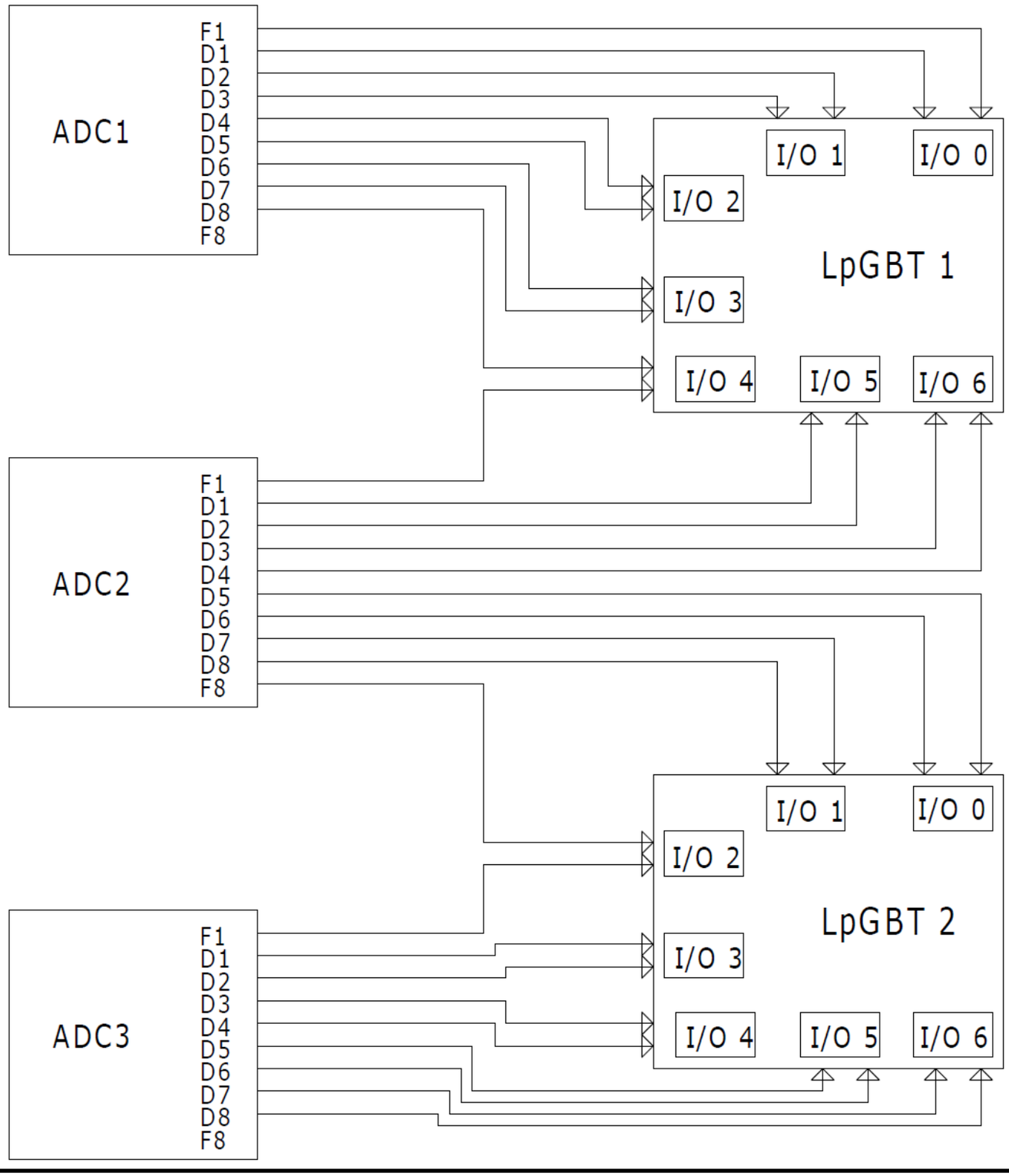
If this scheme is routable we will have 3 different COLUTA to LpGBT mappings



3 ADC to 2 LpGBT structure

"3ADC to 2LpGBT" structures lead to two LpGBT formats (ADC normal mode):

	LpGBT1	LpGBT2
Data[15: 0]	ADC1_F1	ADC2_D5
Data[32: 16]	ADC1_D1	ADC2_D6
Data[57: 32]	ADC1_D2	ADC2_D7
Data[63: 48]	ADC1_D3	ADC2_D8
Data[79: 64]	ADC1_D4	ADC2_F8
Data[95: 80]	ADC1_D5	ADC3_F1
Data[111: 96]	ADC1_D6	ADC3_D1
Data[127:112]	ADC1_D7	ADC3_D2
Data[143:128]	ADC1_D8	ADC3_D3
Data[159:144]	ADC2_F1	ADC3_D4
Data[175:160]	ADC2_D1	ADC3_D5
Data[191:176]	ADC2_D2	ADC3_D6
Data[207:192]	ADC2_D3	ADC3_D7
Data[223:208]	ADC2_D4	ADC3_D8



1 ADC to 1 LpGBT structure

1ADC to 1LpGBT structure leads to an extra format:

LpGBT11

Data[15: 0]	ADC16_F1
Data[32: 16]	ADC16_D1
Data[57: 32]	ADC16_D2
Data[63: 48]	ADC16_D3
Data[79: 64]	ADC16_D4
Data[95: 80]	ADC16_D5
Data[111: 96]	ADC16_D6
Data[127:112]	ADC16_D7
Data[143:128]	ADC16_D8
Data[159:144]	ADC16_F8
Data[175:160]	reserved
Data[191:176]	reserved
Data[207:192]	reserved
Data[223:208]	reserved

Remarks to the formats

We have 3 LpGBT data formats:

LpGBT1 format
LpGBT2 format
LpGBT11 format

The data in these three formats correspond to one ADC sample. ADC sample data packet will never be distributed over 2 LpGBT frames as soon as COLUTA phase aligner is setup properly.

The COLUTA phase aligner is set-up once for given COLUTA-LpGBT connection.

The procedure has these steps (example for LpGBT1 format):
-take LpGBT1 data
-see if LpGBT1 Data1[15:0] is 10xxxxxx00000000
-if not change the phase aligner parameter for ADC1 and repeat first two steps until you see correct frame
-set the same phase aligner parameter to ADC2
-Data[159:144] should be now always identical to Data1[15:0]

Conclusion

-COLUTA to LpGBT mapping is described

-we expect 3 different LpGBT data formats

-COLUTA data content depends on its working mode

Backup Slides

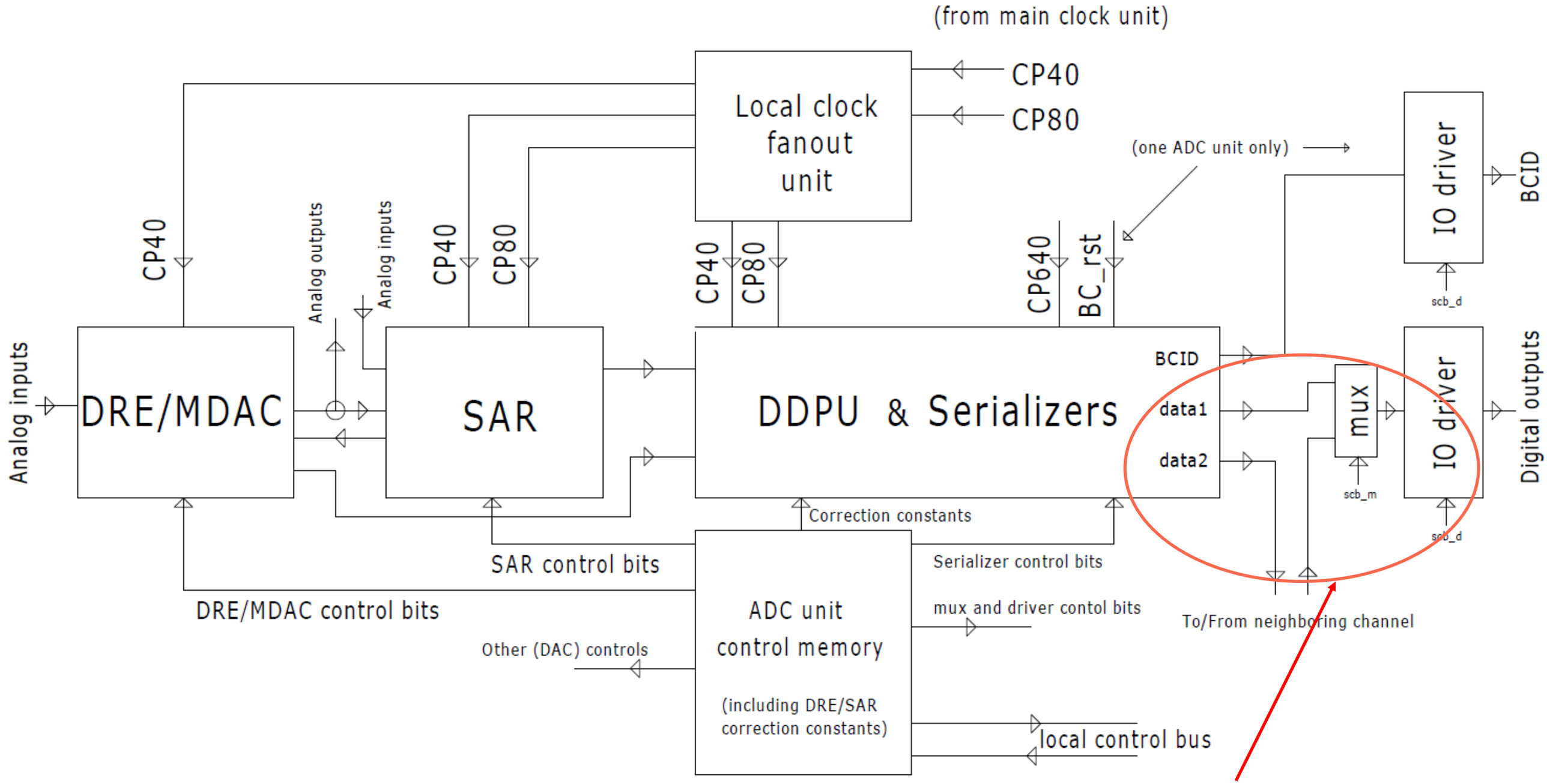
COLUTAV3 data channel (1)

COLUTA V3 chip design requests to transmit more than 16 bits in some modes.

As the relation (mapping and bandwidth) between COLUTA and LpGBT chip is fixed on the board level, V3 backend implements the solution for that problem within COLUTA chip.

Implemented solution introduces 3 transmission modes:
-normal mode (standard 16 bit channel mode)
-32bit Low Gain mode
-32bit High Gain mode

COLUTAV3 data channel (2)



New. Dictated by request to transmit more that 16 bits in some modes

COLUTA transmission modes

COLUTA back-end can process data in different modes defined by ddpu_mode[3:0] bits.

```
//  ddpu_mode[0] 0 => DDPU arithmetic flavor is MDAC
//                   1 => DDPU arithmetic flavor is DRE
//  ddpu_mode[1] 0 => normal  mode
//                   1 => 32 bit raw data mode
//  ddpu_mode[2] 0 => non corrected SAR/MDAC bits are used
//                   1 => SAR/MDAC bits are corrected
//  ddpu_mode[3] 0 => serializer normal mode
//                   1 => serializer test mode
```

Normal or 32 bit raw mode

Controlled by ddpu_mode[1] & scm_m bits

	ADC output	MUX: normal mode	MUX: 32 bit LG mode	MUX: 32 bit HG mode
D1	LG1	LG1[15:0]	LG1[15:0]	HG1[31:16]
D2	HG1	HG1[15:0]	LG1[31:16]	HG1[15:0]
D3	HG2	HG2[15:0]	LG2[15:0]	HG2[31:16]
D4	LG2	LG2 [15:0]	LG2[31:16]	HG2[15:0]
D5	LG3	LG3[15:0]	LG3[15:0]	HG3[31:16]
D6	HG3	HG3[15:0]	LG3[31:16]	HG3[15:0]
D7	HG4	HG4[15:0]	LG4[15:0]	HG4[31:16]
D8	LG4	LG4 [15:0]	LG4[31:16]	HG4[15:0]

Serializer test mode (1)

The mode is set by ddpu_mode[3]=1'b1.

Mode format:

{4'b1010, I2C_CHIP_ID[3:0], CH_NUMBER[2:0], 5'b01001}

Data outputs in serializer test mode are:

	ADC1	ADC2	ADC3
D1:	1010 0000 000 01001	1010 0001 000 01001	1010 0010 000 01001
D2:	1010 0000 001 01001	1010 0001 001 01001	1010 0010 001 01001
D3:	1010 0000 010 01001	1010 0001 010 01001	1010 0010 010 01001
D4:	1010 0000 011 01001	1010 0001 011 01001	1010 0010 011 01001
D5:	1010 0000 100 01001	1010 0001 100 01001	1010 0010 100 01001
D6:	1010 0000 101 01001	1010 0001 101 01001	1010 0010 101 01001
D7:	1010 0000 110 01001	1010 0001 110 01001	1010 0010 110 01001
D8:	1010 0000 111 01001	1010 0001 111 01001	1010 0010 111 01001

This mode allows DAQ to recognize the topological position of the data source on the FEB2 (and confirm the mapping).

Serializer test mode (2)

LpGBT data for serializers in the test mode (format from slide 7):

	LpGBT1	LpGBT2
Data[15: 0]	10 x xxxxx 00000000	1010 0001 100 01001
Data[32: 16]	1010 0000 000 01001	1010 0001 101 01001
Data[57: 32]	1010 0000 001 01001	1010 0001 110 01001
Data[63: 48]	1010 0000 010 01001	1010 0001 111 01001
Data[79: 64]	1010 0000 011 01001	10 x xxxxxx 0000000 ***
Data[95: 80]	1010 0000 100 01001	10 x xxxxxx 0000000
Data[111: 96]	1010 0000 101 01001	1010 0010 000 01001
Data[127:112]	1010 0000 110 01001	1010 0010 001 01001
Data[143:128]	1010 0000 110 01001	1010 0010 010 01001
Data[159:144]	10 x xxxxxx 0000000	1010 0010 011 01001
Data[175:160]	1010 0001 000 01001	1010 0010 100 01001
Data[191:176]	1010 0001 001 01001	1010 0010 101 01001
Data[207:192]	1010 0001 010 01001	1010 0010 110 01001
Data[223:208]	1010 0001 011 01001	1010 0010 111 01001

***all four ADC frames must be the same

32 bit mode

32 bit raw data mode will allow to send data using two 640MHz ADC neighboring data channels.

Lower 16 bits are transmitted by serializer A (data1) of the DDPU.
We annotate it as ADCx_LGy[15:0] for low gain channels
and ADCx_HGy[15:0] for high gain channels
Format of lower bit word is
for DRE flavor
{ spare[1:0], before_edge_tst, after_edge_tst, 5'b00000, dre_r2[2:0], sar_r2[20:17]};
and for MDAC flavor
{ spare[1:0], before_edge_tst, after_edge_tst, mdac_r2[11:4], sar_r2[20:17]};

Higher 16 bits are transmitted by serializer B (data2) of the DDPU.
We annotate it as ADCx_LGy[31:16] for low gain channels
and ADCx_HGy[31:16] for high gain channels
Format of higher bit word is always
{sar_r2[16:1]};

LG mode (1)

LpGBT data in LG mode (slide 7 and slide 15 combined):

	LpGBT1	LpGBT2
Data[15: 0]	ADC1_F1	ADC2_LG3[15: 0]
Data[32: 16]	ADC1_LG1[15: 0]	ADC2_LG3[31:16]
Data[57: 32]	ADC1_LG1[31:16]	ADC2_LG4[15: 0]
Data[63: 48]	ADC1_LG2[15: 0]	ADC2_LG4[31:16]
Data[79: 64]	ADC1_LG2[31:16]	ADC2_F8
Data[95: 80]	ADC1_LG3[15: 0]	ADC3_F1***
Data[111: 96]	ADC1_LG3[31:16]	ADC3_LG1[15: 0]
Data[127:112]	ADC1_LG4[15: 0]	ADC3_LG1[31:16]
Data[143:128]	ADC1_LG4[31:16]	ADC3_LG2[15: 0]
Data[159:144]	ADC2_F1	ADC3_LG2[31:16]
Data[175:160]	ADC2_LG1[15: 0]	ADC3_LG3[15: 0]
Data[191:176]	ADC2_LG1[31:16]	ADC3_LG3[31:16]
Data[207:192]	ADC2_LG2[15: 0]	ADC3_LG4[15: 0]
Data[223:208]	ADC2_LG2[31:16]	ADC3_LG4[31:16]

***all four ADC frames must be the same

LG mode (2)

LpGBT data in LG mode (slide 8 and slide 15 combined):

	LpGBT11
Data[15: 0]	ADC16_F1
Data[32: 16]	ADC16_LG1[15: 0]
Data[57: 32]	ADC16_LG1[31:16]
Data[63: 48]	ADC16_LG2[15: 0]
Data[79: 64]	ADC16_LG2[31:16]
Data[95: 80]	ADC16_LG3[15: 0]
Data[111: 96]	ADC16_LG3[31:16]
Data[127:112]	ADC16_LG4[15: 0]
Data[143:128]	ADC16_LG4[31:16]
Data[159:144]	ADC26_F1
Data[175:160]	reserved
Data[191:176]	reserved
Data[207:192]	reserved
Data[223:208]	reserved

HG mode(1)

LpGBT data in HG mode (slide 7 and slide 15 combined):

	LpGBT1	LpGBT2
Data[15: 0]	ADC1_F1	ADC2_HG3[31:16]
Data[32: 16]	ADC1_HG1[31:16]	ADC2_HG3[15: 0]
Data[57: 32]	ADC1_HG1[15: 0]	ADC2_HG4[31:16]
Data[63: 48]	ADC1_HG2[31:16]	ADC2_HG4[15: 0]
Data[79: 64]	ADC1_HG2[15: 0]	ADC2_F8
Data[95: 80]	ADC1_HG3[31:16]	ADC3_F1***
Data[111: 96]	ADC1_HG3[15: 0]	ADC3_HG1[31:16]
Data[127:112]	ADC1_HG4[31:16]	ADC3_HG1[15: 0]
Data[143:128]	ADC1_HG4[15: 0]	ADC3_HG2[31:16]
Data[159:144]	ADC2_F1	ADC3_HG2[15: 0]
Data[175:160]	ADC2_HG1[31:16]	ADC3_HG3[31:16]
Data[191:176]	ADC2_HG1[15: 0]	ADC3_HG3[15: 0]
Data[207:192]	ADC2_HG2[31:16]	ADC3_HG4[31:16]
Data[223:208]	ADC2_HG2[15: 0]	ADC3_HG4[15: 0]

***all four ADC frames must be the same

HG mode (2)

LpGBT data in HG mode (slide 8 and slide 15 combined):

	LpGBT11
Data[15: 0]	ADC16_F1
Data[32: 16]	ADC16_HG1[31:16]
Data[57: 32]	ADC16_HG1[15: 0]
Data[63: 48]	ADC16_HG2[31:16]
Data[79: 64]	ADC16_HG2[15: 0]
Data[95: 80]	ADC16_HG3[31:16]
Data[111: 96]	ADC16_HG3[15: 0]
Data[127:112]	ADC16_HG4[31:16]
Data[143:128]	ADC16_HG4[15: 0]
Data[159:144]	ADC26_F1
Data[175:160]	reserved
Data[191:176]	reserved
Data[207:192]	reserved
Data[223:208]	reserved