COLUTAv4: Update

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On behalf of the COLUTA Team

June 15th, 2022

1. COLUTAv4 ADC & Testboard Overview
2. Performance Testing
3. Radiation Testing
4. BGA Packaging
5. Production Testing Preparation

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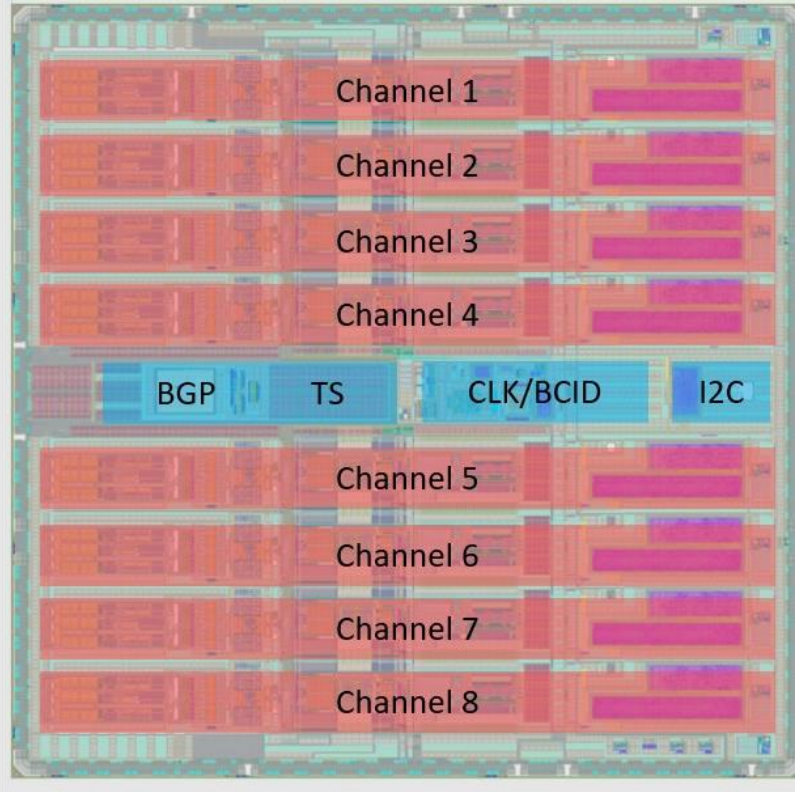
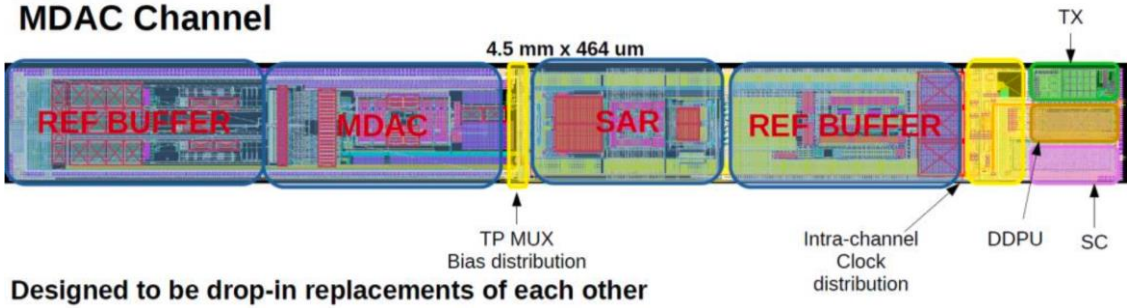
COLUTAv4 ADC

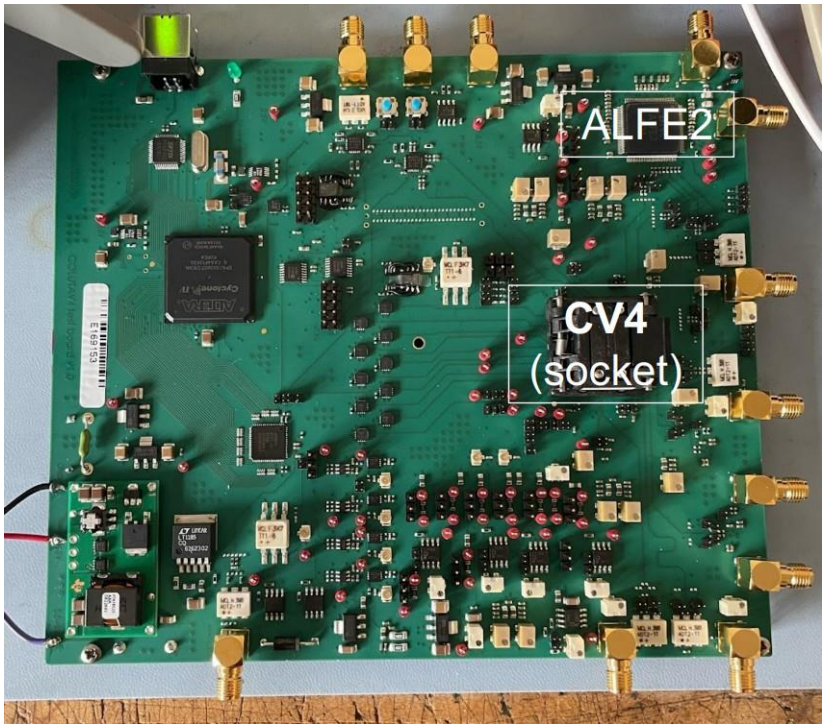
- 8 channel, 15-bit ADC
- MDAC+SAR+DDPU Architecture
- TSMC 65nm
- 40 MSPS
- 5.854 x 5.456 mm^2
- 4.3 million transistors
- 1.2 V operation with 2 Vpp differential input
- Received Dec. 20th
- 20/100 packaged in QFN
  - Performance assessed for all packaged chips





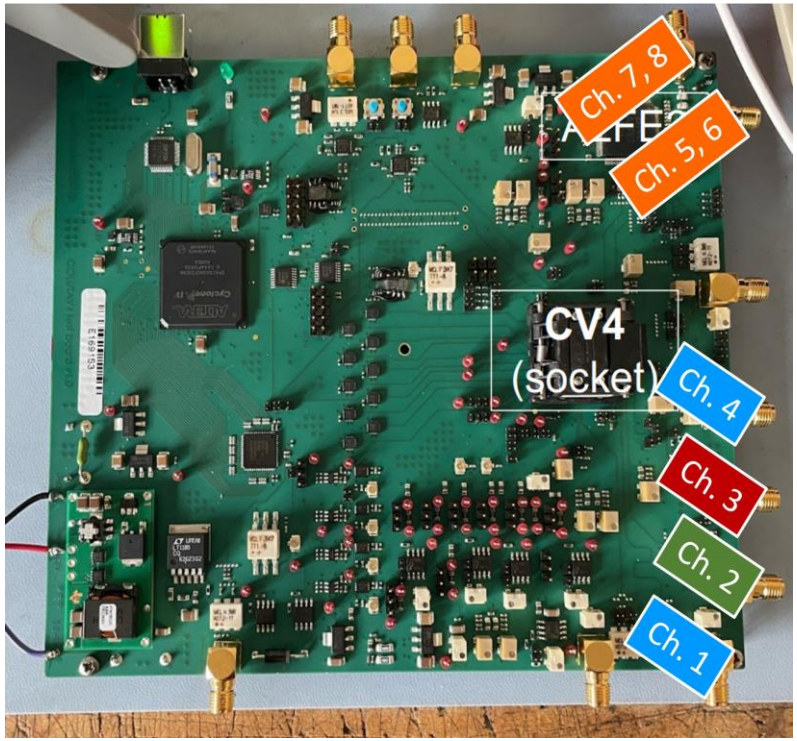
COLUTAv4 Testboard

- Includes ALFE2 for PA/S integration testing
- First board assembled in early Feb.
- Socketed boards used for initial testing
  - Board with soldered chip arrived this week
- Additional testboards provided to UT-Austin and Saclay
  - Saclay progress with COLUTA test board:
    - Talk: Status of ADC Production QC Setup



Test Setup

- CV4 Channels
  - Ch 1, 4: transformer input
  - Ch 2: commercial amplifier input
  - Ch 3: connected to onboard DAC
    - Modified COLUTA input network so DAC chip can drive COLUTA
  - Ch 5-8: connected to ALFE2
    - Ch 6, 7: high gain
    - Ch 5, 8: low gain
- Input signals provided by AWG
  - Connected with filters (for sinewave) and/or attenuators (LAr pulse input)
- On board DAC used for linear ramp input
- Calibration for MDAC & SAR performed with on-chip circuits and checked off-chip



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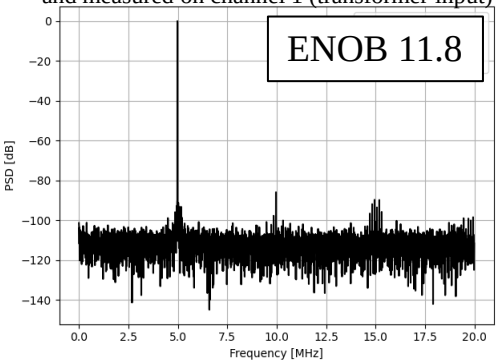
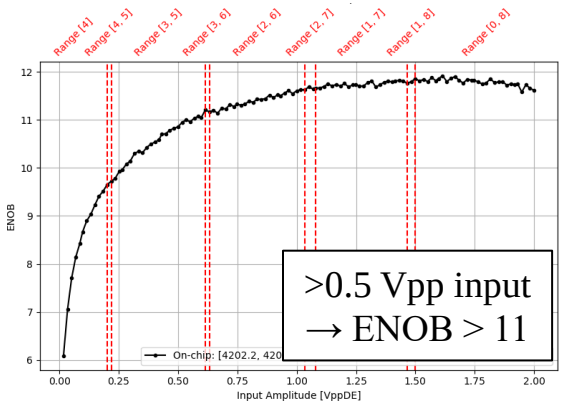
Sine Wave Performance

- Vary sinewave input amplitude to characterize performance
- Performance characterized up to high frequencies (close to Nyquist)
- Preliminary performance of soldered down chip measured yesterday!

Socketed chip performance

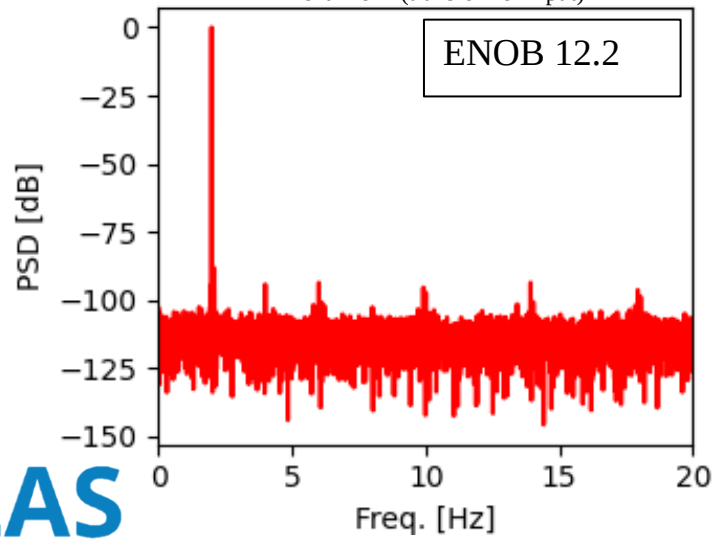
Near full-scale amplitude, frequency of 5 MHz and measured on channel 1 (transformer input)

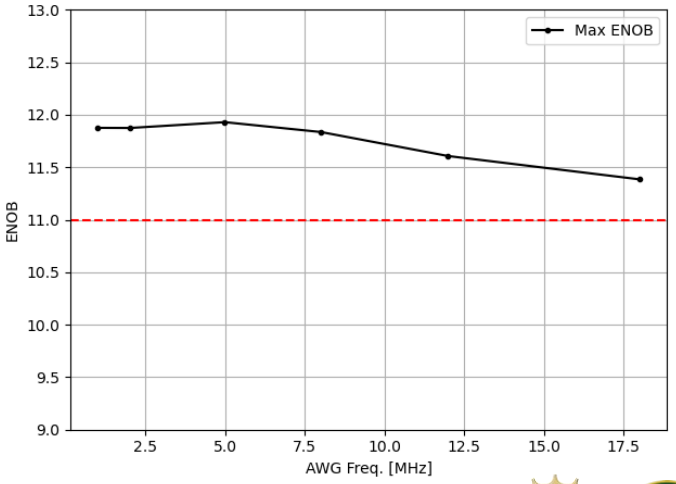




Soldered chip performance

Near full-scale amplitude, frequency of 2 MHz and measured on channel 4 (transformer input)

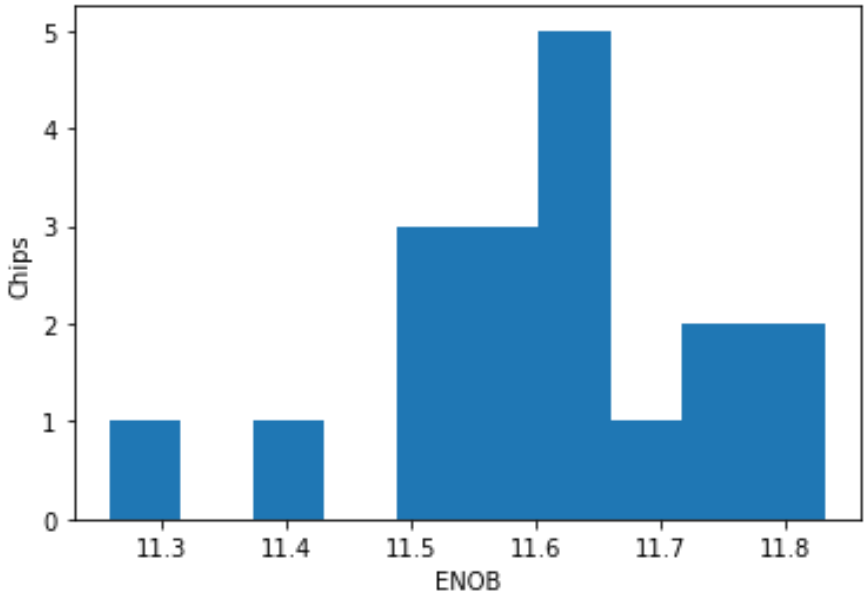




ATLAS EXPERIMENT

COLUTA Yield and Stability

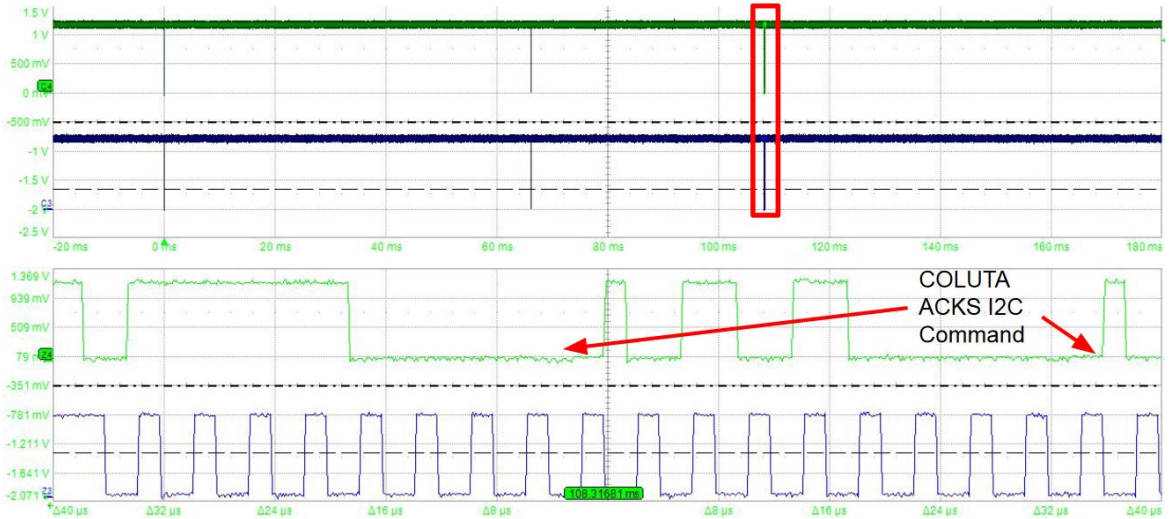
- Performance measured across 18-chips
  - 2 did not configure (may be possible to recover)
- ENOB of >11-bits (average 11.61-bits)
  - Sinewave characteristics: 5 MHz and full scale amplitude
  - Performance characterized using channel 1
  - Used on-chip calibration
- On chip calibration checked by comparing with off-line derived constants
  - Constants vary < 1% over 48+ hrs



False Start Tests

- **In CV3** NO-ACK was systematically observed for particular timing relationships between SCL and the state machine's on-chip 40 MHz clock
- **In CV4** to improve I2C Robustness we added a Schmitt trigger and modified synchronization to SDA and SCL inputs
- Test in CV4 with repeated false start signals

I2C Write Command AFTER I2C False Start



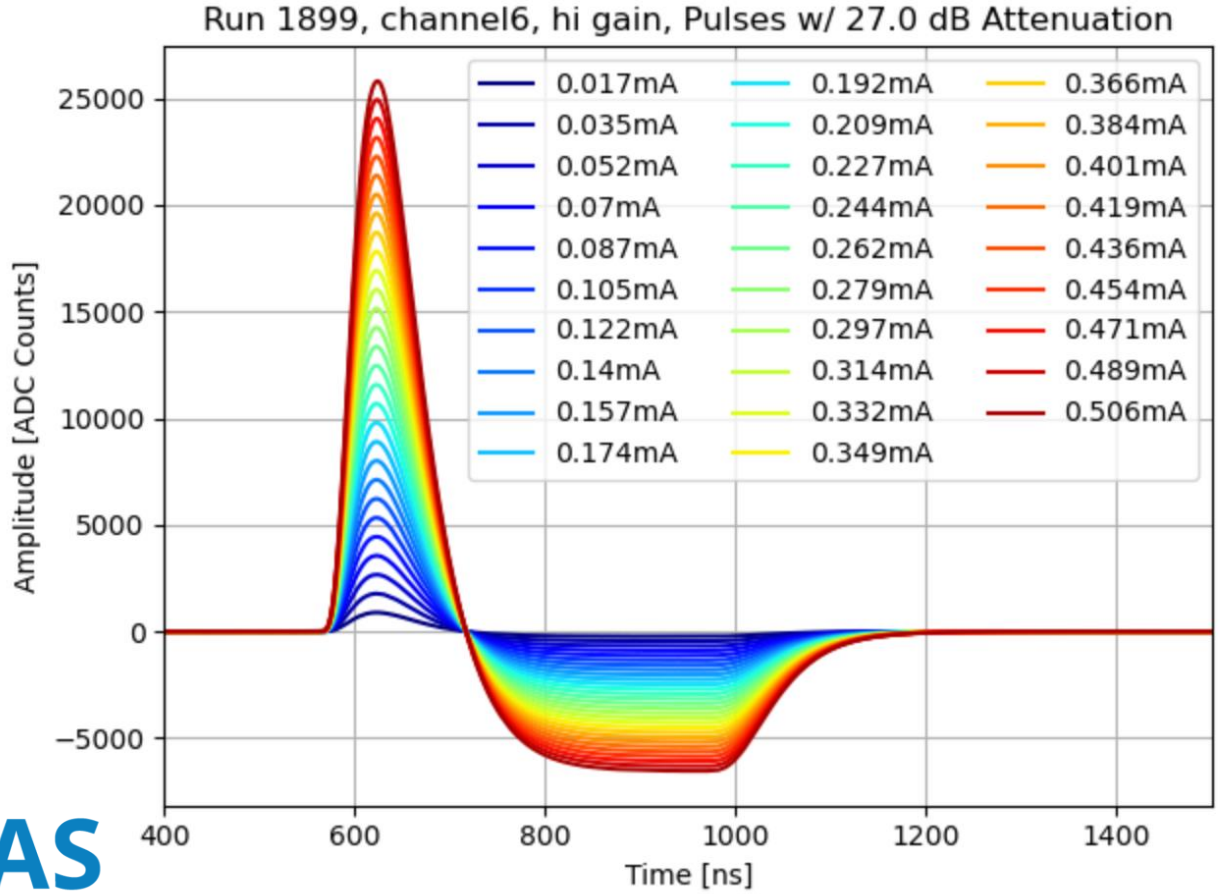
Test sequence:

1. Reset COLUTA
2. Perform first I2C write
   → Check for ACK
3. Send I2C false start signal
4. Perform second I2C write
   → Check for ACK

In 3000 + tests every I2C write command was acknowledged

PA/S Integration Tests

- ALFE2 successfully configured with 25 Ω
- 30 pulses interleaved to create fine resolution pulse for analysis (OFCs)
- Talk: FEB 2 Prototype Development



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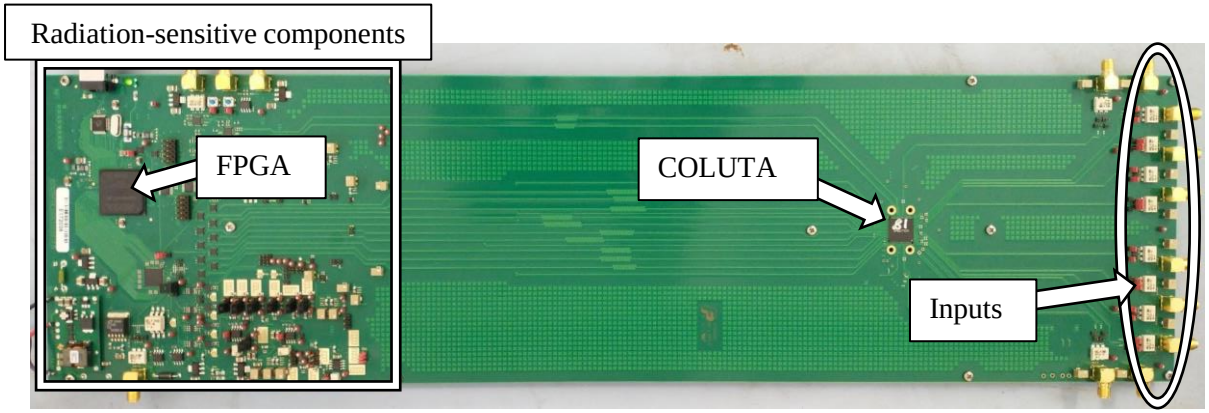
Radiation Testing



- Radiation board designed in Feb.-Mar.
  - Elongated original testboard, removed ALFE2, altered inputs to 8 identical transformer inputs
- Fabricated and assembled in Apr.-May
- Arrived last week and I2C communication with COLUTA verified
- Testing planned for Aug. 6&7 at MGH in Boston
  - Repeat of tests done for CV3, focus on SEU tests in data stream and configuration bits:
    - Cv3 → Cv4: moved the triple-modular redundant D-flip
    - flops farther apart to improve SEU tolerance

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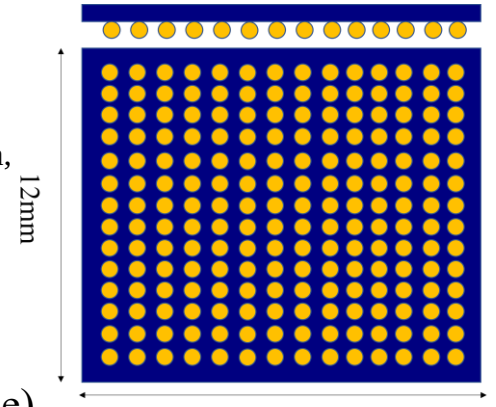
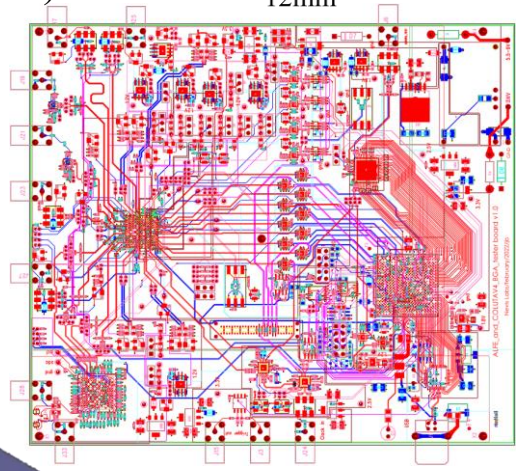
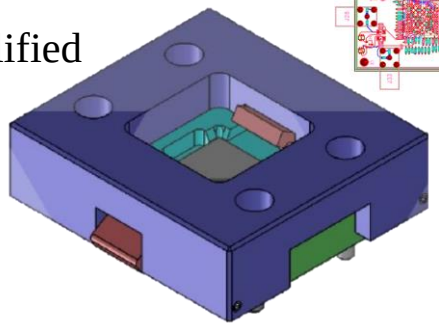
BGA Packaging

- JCET selected by tendering process → PO issued in mid-May
  - Same vendor and package spec as PA/S
    - Package spec: Low-Profile Fine Pitch Ball Grid Array (LFPBGA), ball pitch 0.8 mm, size 12 mm x 12 mm, solder ball array (14x14)
    - 2D barcode spec: with 10µm etching depth, 8mm x 8mm area, version 1 QR code (21x21), Q redundancy 25 %
- Production schedule
  - Fall 2022: 80 CV4 chips to be packaged (depends on JCET's schedule)
  - Spring 2023: 1000 chips from preseries (CV5, tape-out following FDR) to be packaged (JCET schedule likely not the limiting factor)
  - Late 2023 and following: production packaging of ~80,000 chips
- Board designed for BGA package
- VA innovation socket studied as a candidate for BGA
  - Tested at Saclay
  - Specs: uses open top design with pogo pins, qualified for 500k-700k cycles, automatically cleaned







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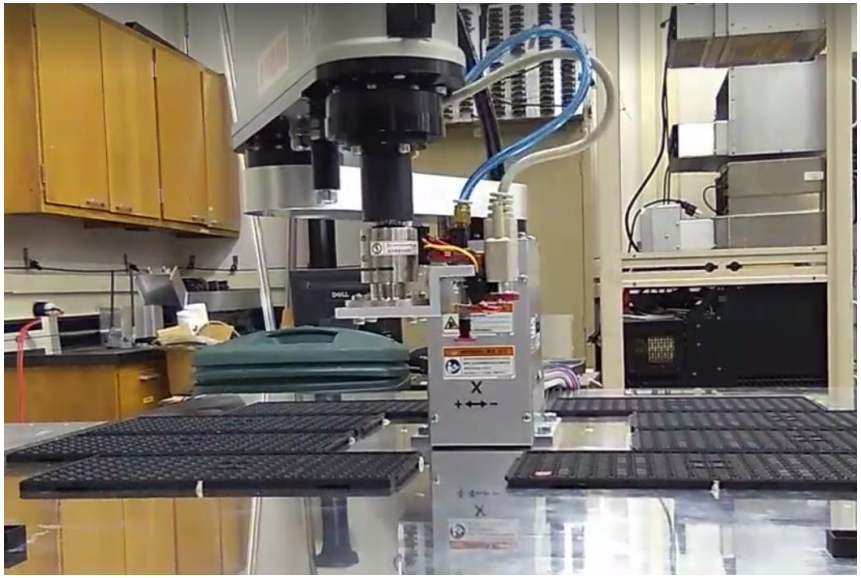
Production Testing Preparation

UT Austin

- Reliable pick and place of plastic “chips” in 1280 pockets in working envelope



Saclay

- Automation is ongoing
- Industrial robot to be purchased which includes camera system implemented for reading 2d barcodes

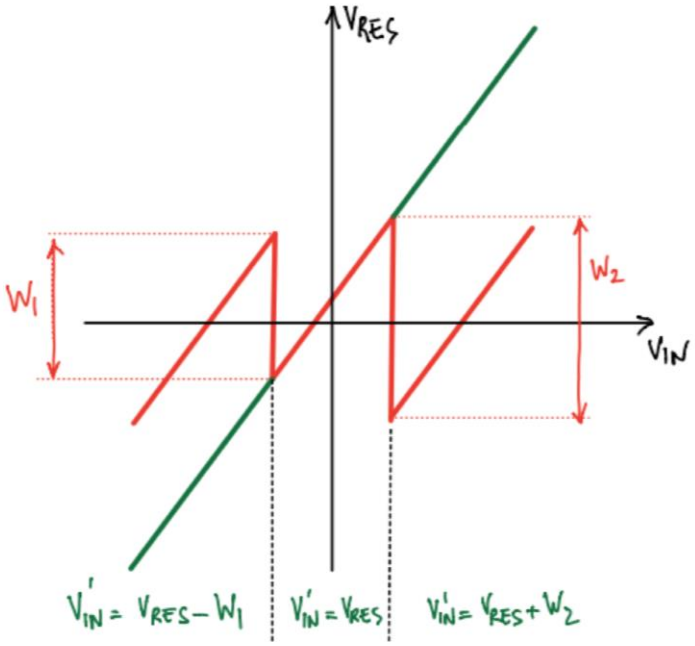
Conclusions

- Continued performance tests show good results for :
  - Dynamic range measurements (INL/DNL results in previous talk)
  - False start tests → I2C robustness fixes worked
  - Pre-amp shaper integration tests underway → Talk: FEB 2 Prototype Development
- Radiation boards received and preparations underway for early Aug. tests at MGH
- BGA packaging progressing → PO issued
- Production testing automation is ongoing
- Preparations for FDR underway. Preparing list of remaining measurements to be done in lab (e.g. cross talk). Preparing documentation, including updated QA/QC testing plans. Will be ready in early fall.
- Thanks!

ATLAS EXPERIMENT

Backup

Foreground Calibration Principle



Simplified diagram for three subranges; chip has 9 subranges and 8 W-constants

- Given a piece-wise linear transfer curve with the same gain in all sections and giver the heights of the transitions Wi, you can reconstruct a linear V'in from the residue Vres
  - V'in gain and offset error will be corrected by the system

Optimization of MDAC On-Chip Weights

- On-chip MDAC calibration
  - MDAC contains 9 distinct subranges
  - Calibration processes "stitches" together subranges with a set of 8 weights to create a linear transfer function
  - Weights derived from on-chip circuit
- Offline (FMinSearch) calibration
  - Offline "fitted" calibration derives weights to yield best possible sine performance
  - Used only to debug on-chip process
- On-chip calibration constants systematically ~4-5 counts lower than offline constants
  - True for multiple CV4 channels and chips
  - Reason for this still under investigation...
  - For now added 4 count empirical offset to on-chip calib. for improved performance