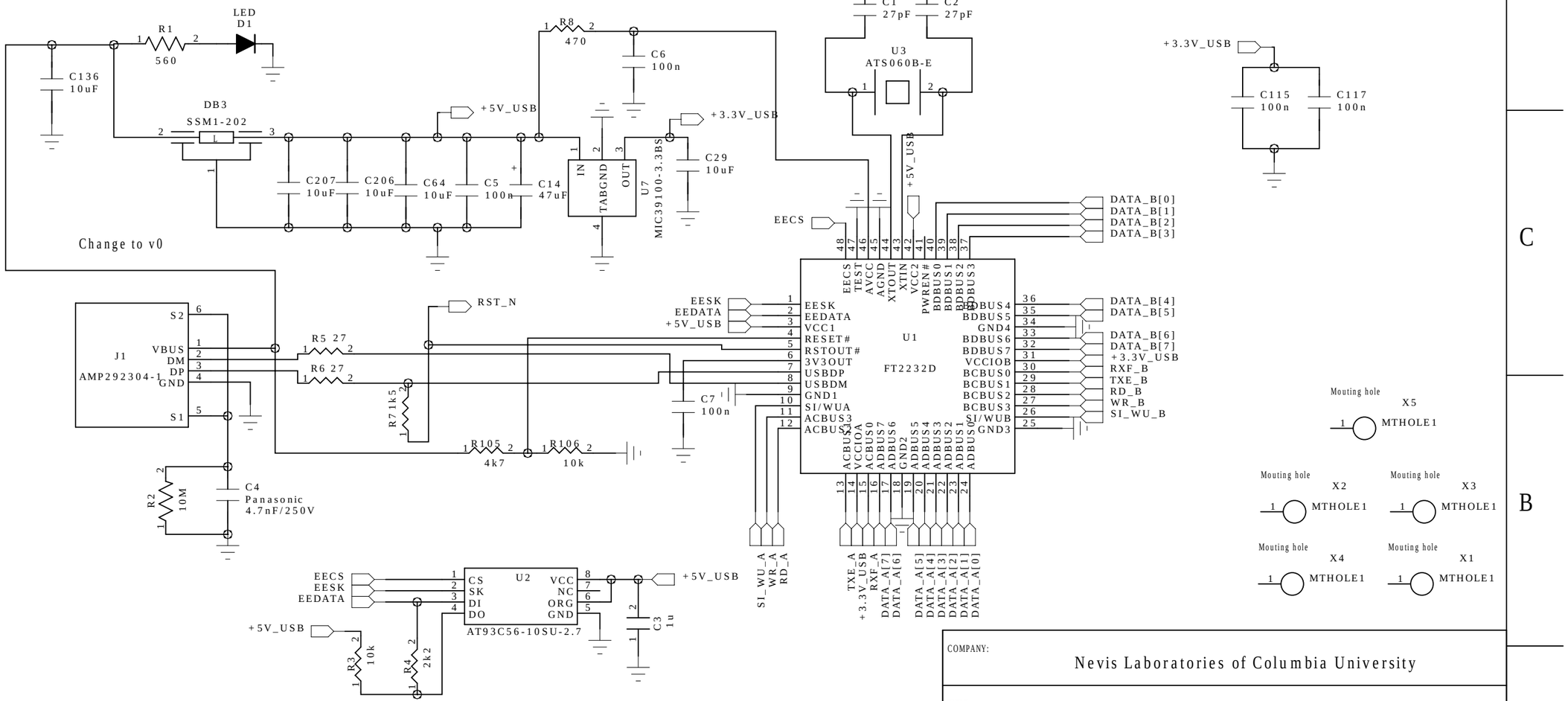
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

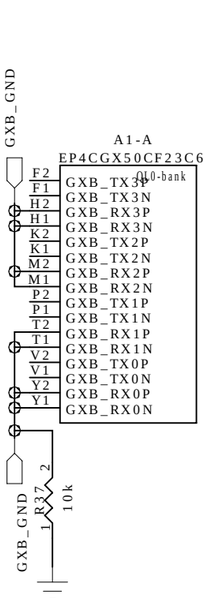


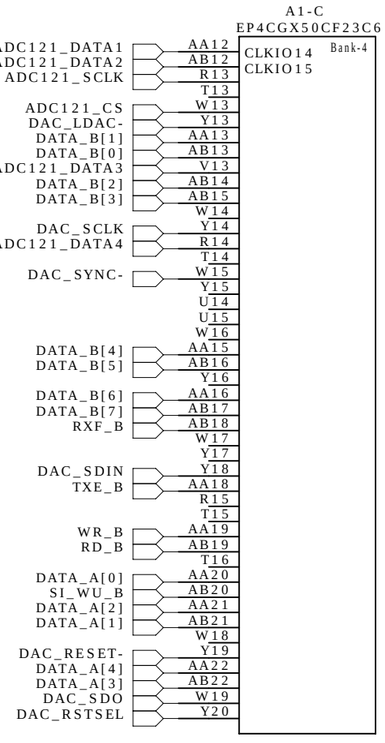
DRAWN: jb/2017	DATED: jb/2017	COMPANY: Nevis Laboratories of Columbia University	
CHECKED:	DATED:	TITLE: COLUTAV3 test board	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 1OF 10

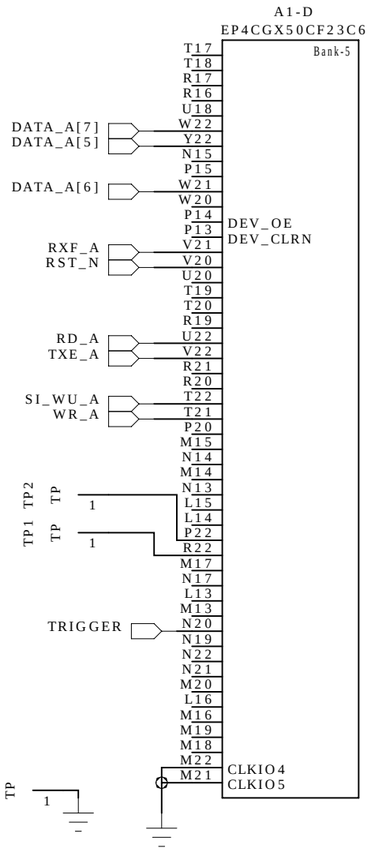
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

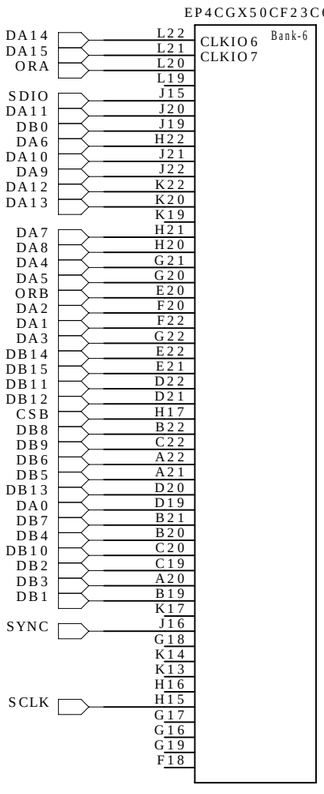
DRAWN: jb/2019	DATED:	COMPANY: Nevis Laboratories of Columbia University	
CHECKED:	DATED:	TITLE: COLUTA4 test board	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B / DRAWING NO: v0 / REV: 0
RELEASED:	DATED:	SCALE:	SHEET: 2 OF 25

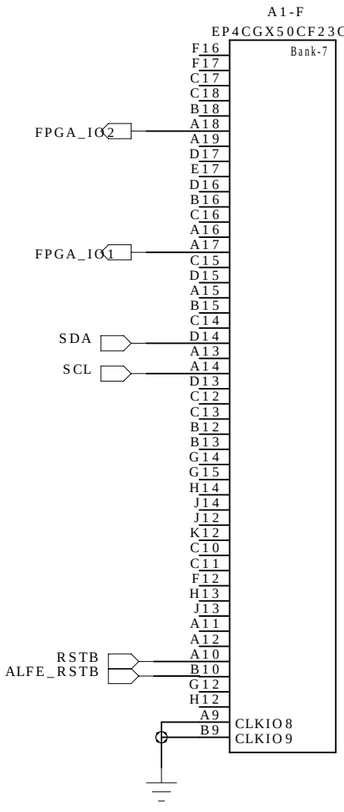
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

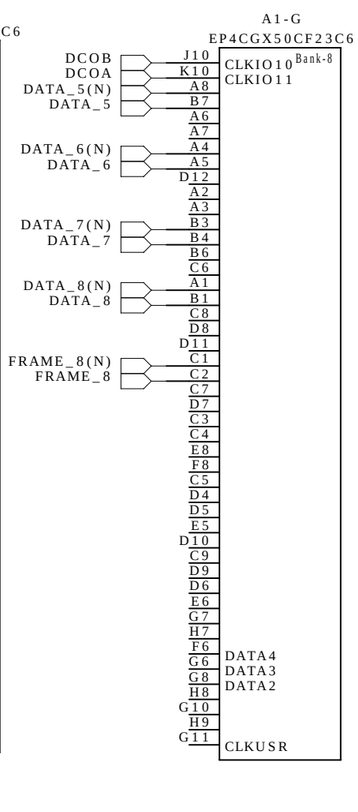


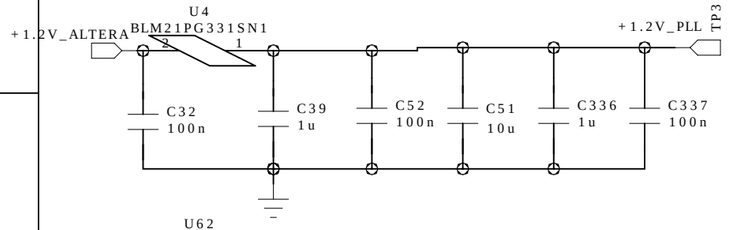


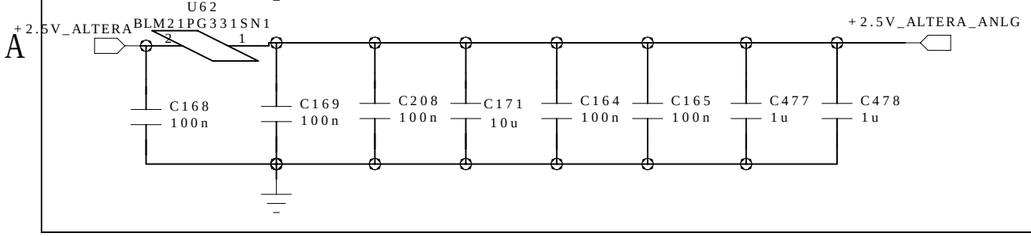












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CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: COLUTA4 test board	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: B
RELEASED: jb	DATED: <Release Date>	DRAWING NO: v0	REV: 0
		SCALE: <Scale>	SHEET: 3 25

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

+3.6V_RAW
C40 47uF
U20 MIC39100-3.3BS (IN, TABGND, OUT)
C65 10uF
C62 100n
C1206B
C60 10u
T66 KEYSTONE_TP
+3.3V_CLK
U35 MIC39100-2.5BS (IN, GNDTAB, OUT)
T67 KEYSTONE_TP
+2.5V_CLK
C56 47uF
C58 47uF
C50 0.1
C45 0.1
C5510u
C369 0.1

+2.5V_CLK +2.5V_CLK +2.5V_CLK +2.5V_CLK +2.5V_CLK
8k2 8k2 820 8k2 820 820
S0 S1 S2 S3 S4 S5

out0 = /16 out1=/16 out2=/1 out3=/16

all ouputs are LVDS

9508_RSTB
0.47uF C362
1uF C365
+2.5V_CLK

U72 AD9508BCPZ

S0	19	SCLK/SCL/S0	
9508_SYNCB	20	SYNC	
MAIN_CLK+	21	CLK	
MAIN_CLK-	22	CLK	
+2.5V_CLK	23	IN_SEL	
S1	24	SDIO/SDA/S1	
	18	RESET	
	17	OUT3	
	16	OUT3	
	15	PROG_SEL	
	14	EXT_CAP1	
	13	VDD2	
	12	OUT2	
	11	OUT2	
S5	10	S5	
S4	9	S4	
	8	OUT1	
	7	OUT1	
	6	VDD1	
	5	EXT_CAP0	
	4	SDO/S3	
	3	OUT0	
	2	OUT0	
	1	CS/S2	
	25	DP	

S2 S3 +2.5V_CLK

C61 0.47uF
1uF C366

R185 50 100n C364 CLKIN_40N
R186 50 100n C363 CLKIN_40P
R187 50 100n C156 CLKIN_640N
R188 50 100n C148 CLKIN_640P

AD_9650_CLK- H2 HEADER_50MIL
H3 HEADER_50MIL
R90 100
0.1 C145 9650_CLK-
0.1 C146 9650_CLK+
AD_9650_CLK+ H5 HEADER_50MIL
H4 HEADER_50MIL

FPGA_9508_RSTB H66 HEADER_50MIL
9508_RSTB H67 HEADER_50MIL
+2.5V_CLK 10k
7914J-1-000E S1
C367 0.1

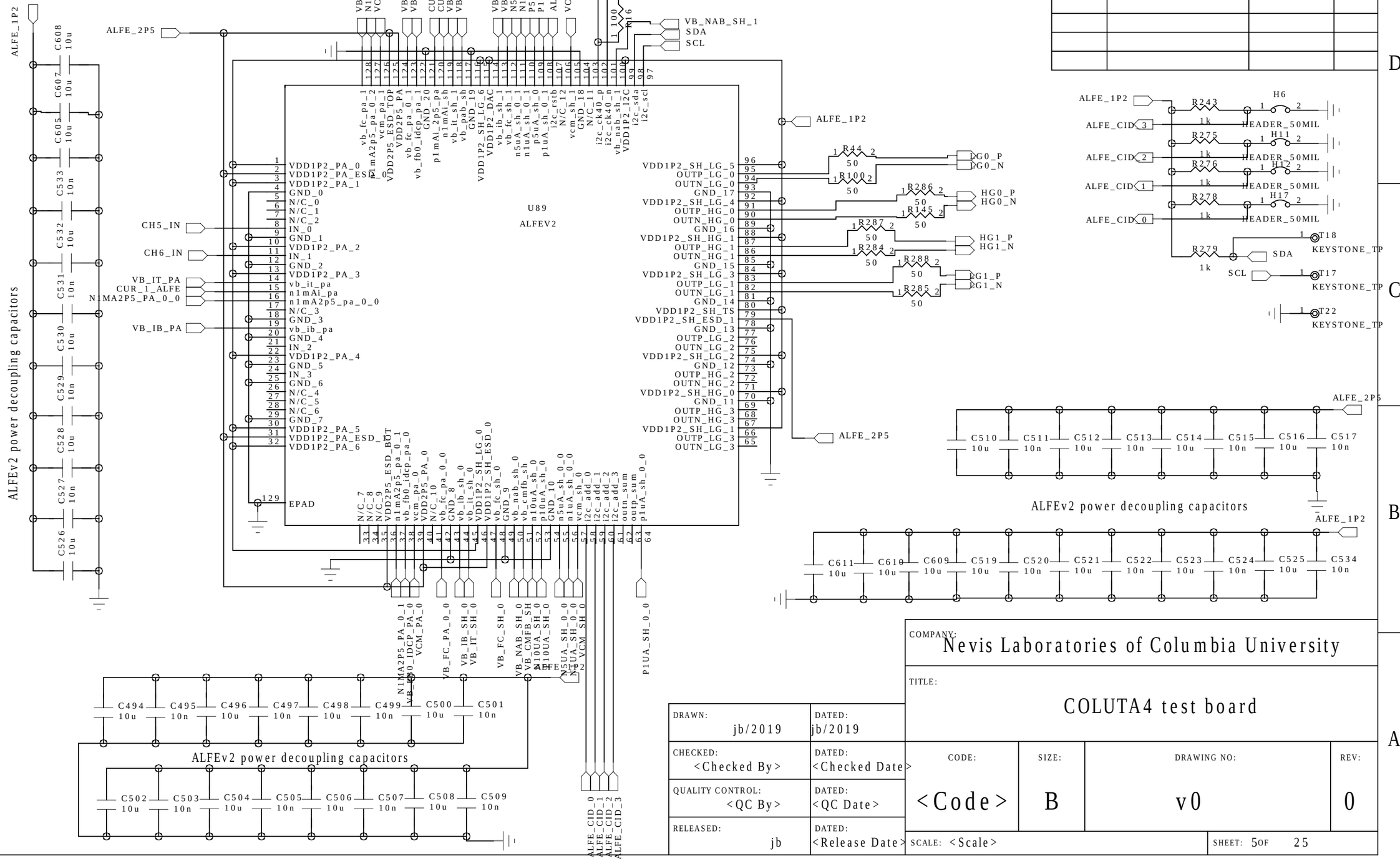
FPGA_9508_SYNCB H68 HEADER_50MIL
9508_SYNCB H69 HEADER_50MIL
+2.5V_CLK 10k
7914J-1-000E S2
C368 0.1

+3.3V_CLK
C41 0.1
J2 MC100EPT20 (VCC, D, GND, Q, /Q)
120 C42 0.1
120 C43 0.1
J15 J3 CON/SMA/PC_JACK
TRIGGER

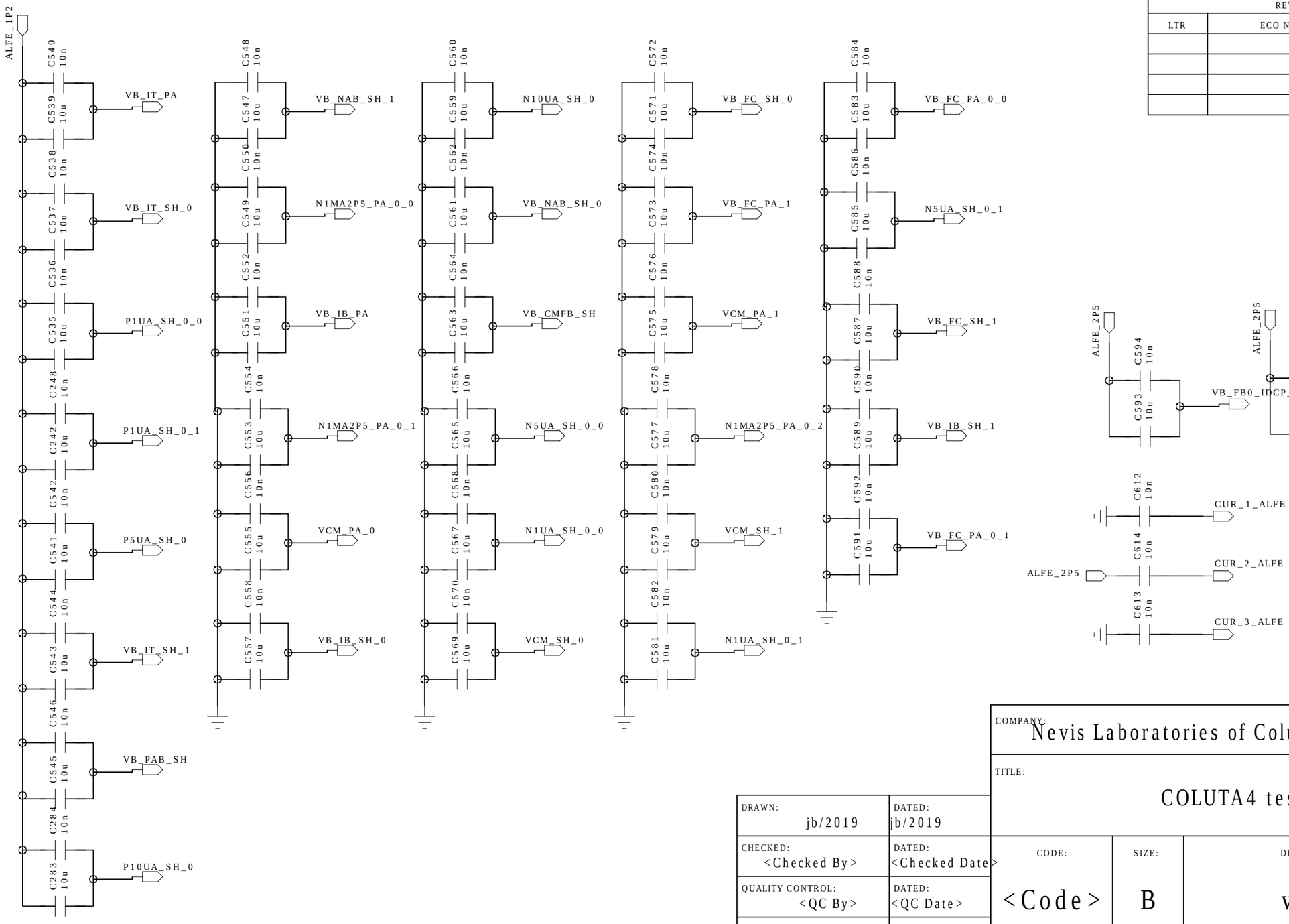
R22 100
FPGA_CLK+ FPGA_CLK-

DRAWN: jb/2019	DATED: jb/2019	COMPANY: Nevis Laboratories of Columbia University	
CHECKED:	DATED:	TITLE: COLUTA4 test board	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	DRAWING NO: v0	REV: 0
		SCALE:	SHEET: 4 OF 25

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN: jb/2019	DATED: jb/2019	COMPANY: Nevis Laboratories of Columbia University	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: COLUTA4 test board	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: B
RELEASED: jb	DATED: <Release Date>	DRAWING NO: v0	REV: 0
		SCALE: <Scale>	SHEET: 5 OF 25



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

DRAWN: jb/2019	DATED: jb/2019		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: jb	DATED: <Release Date>		

COMPANY: Nevis Laboratories of Columbia University

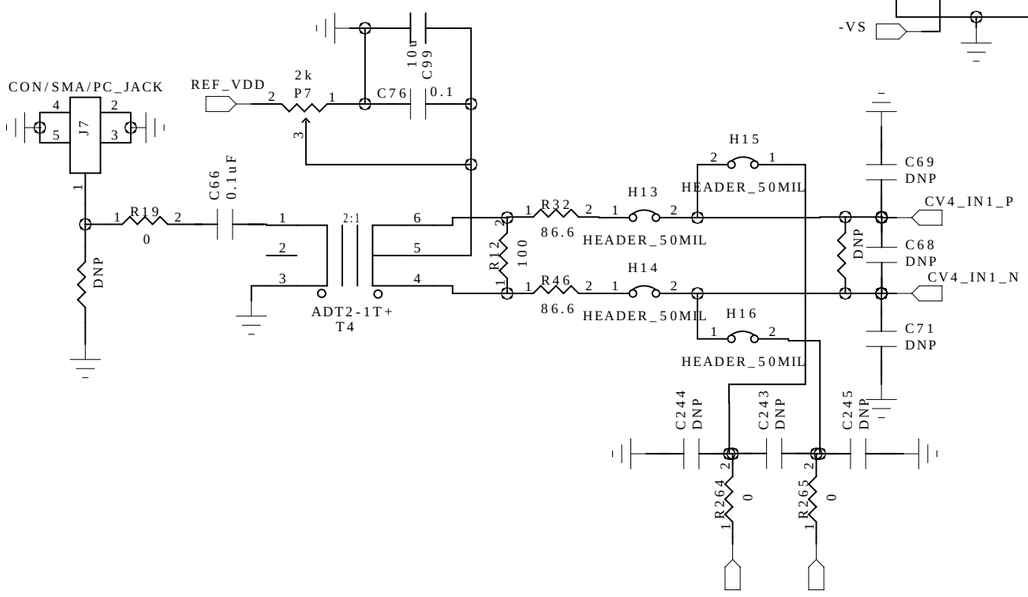
TITLE: COLUTA4 test board

CODE:	SIZE:	DRAWING NO:	REV:
<Code>	B	v0	0

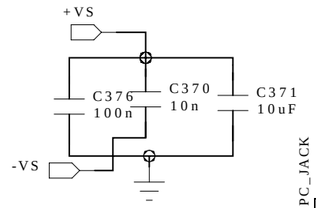
SCALE: <Scale> SHEET: 6 OF 25

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

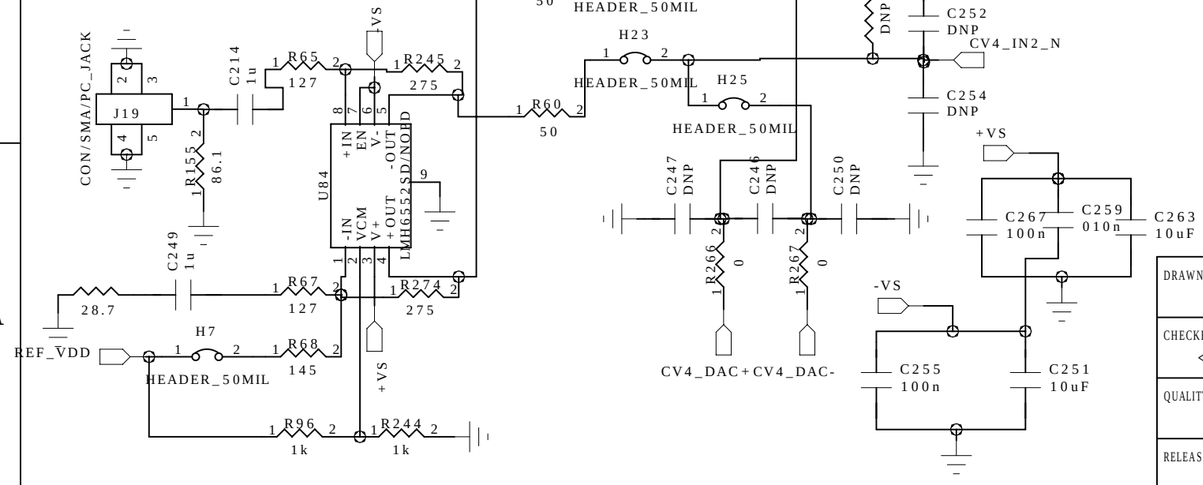
"post-post mod" with 75mm delay line



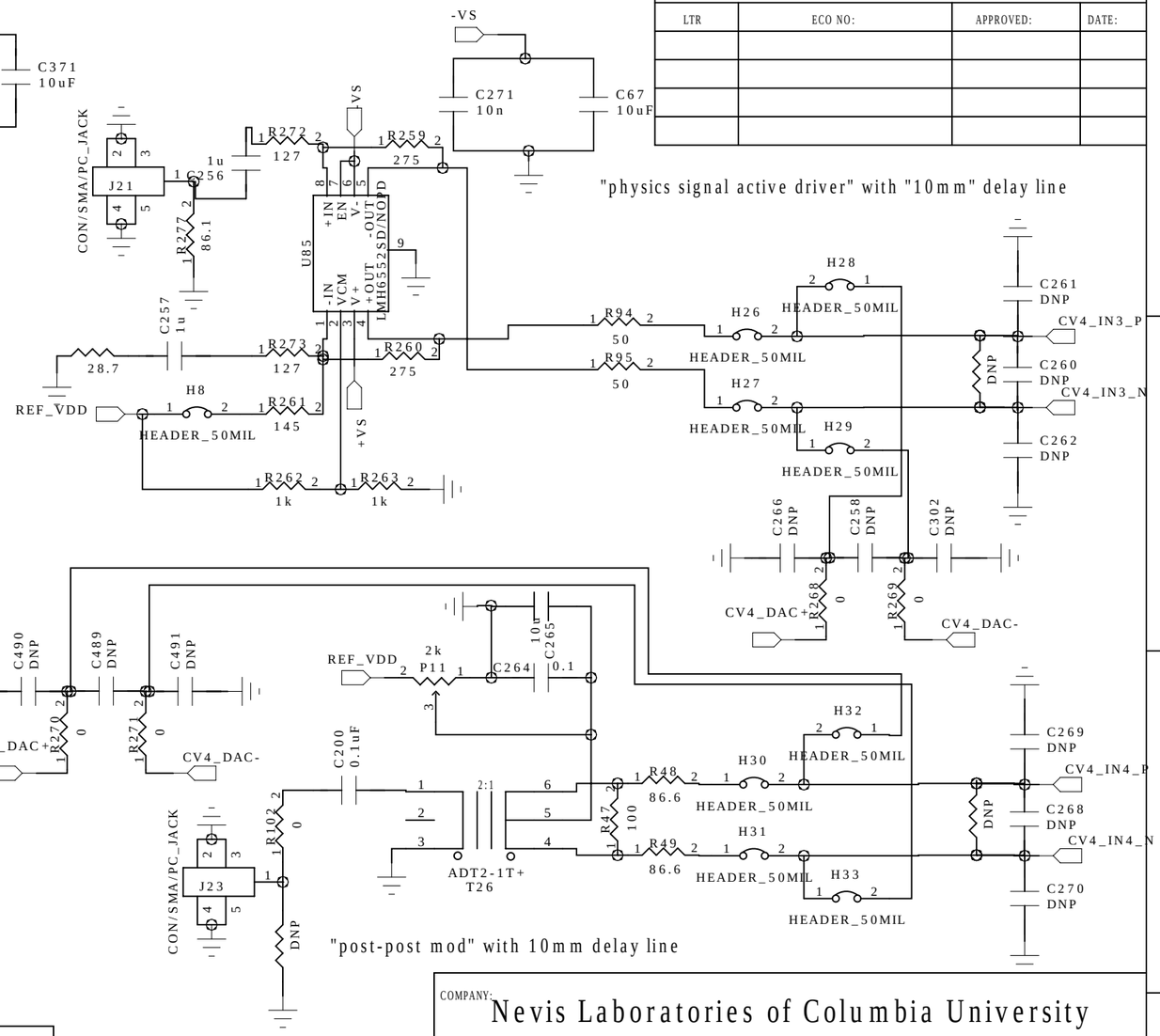
+VS / -VS



"physics signal active driver" with "75mm" delay line



"post-post mod" with 10mm delay line



+VS / -VS

DRAWN: jb/2019	DATED: jb/2019	COMPANY: Nevis Laboratories of Columbia University	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: COLUTA4 test board	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: B
RELEASED: jb	DATED: <Release Date>	DRAWING NO: v0	REV: 0
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REVISION RECORD			
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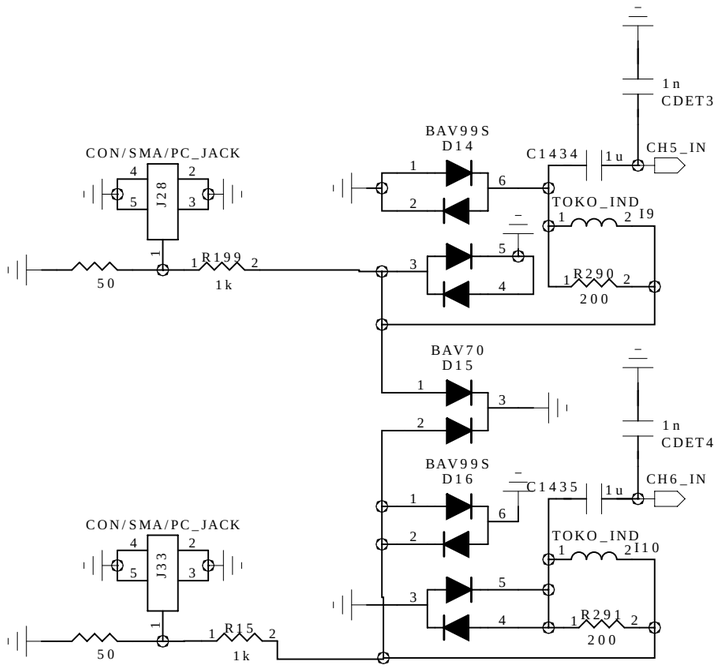

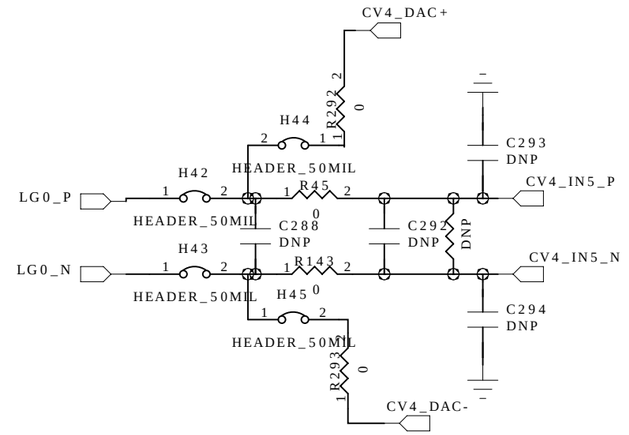

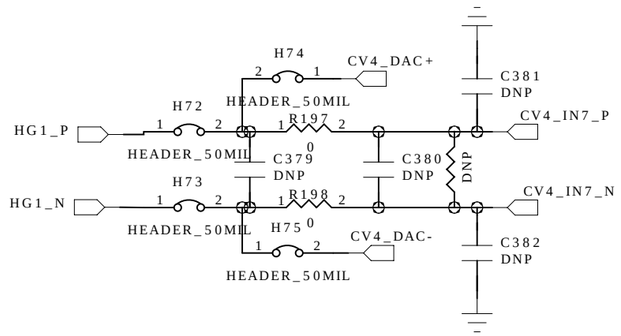

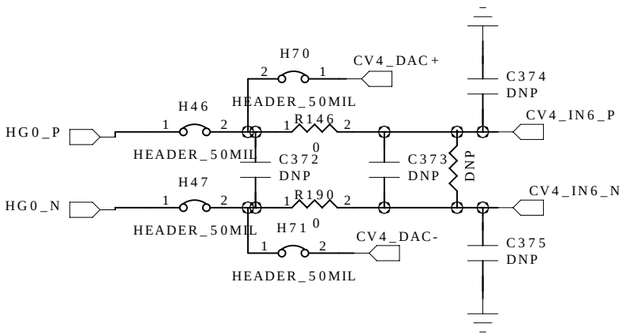

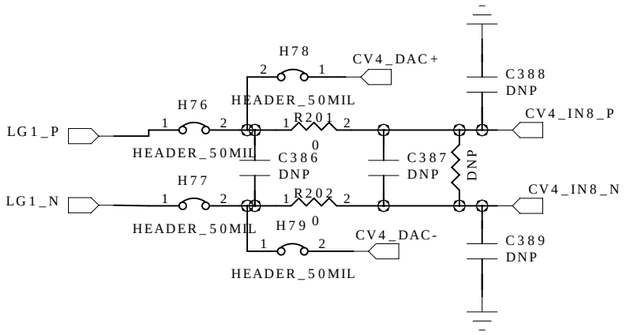

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RELEASED: jb	DATED: <Release Date>	DRAWING NO: v0	REV: 0
		SCALE: <Scale>	SHEET: 8 OF 25

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

REF_VDD
J18
KEYSTONE_TP KEYSTONE_TP
T19
T20
R27
1k
P2
2k
IBIAS_EXT
200mV across 1kOhm resistor
JUMPER/3P
C338 0.1
C339 0.1

VDDA1_SAR
C123 1u
C26 0.1
C122 0.1

VDDA2_SAR
C273 1u
C238 0.1
C272 0.1

VDDA3_SAR
C276 1u
C274 0.1
C275 0.1

VDDA_DRE
C162 1u
C160 0.1
C161 0.1
C96 0.1

VDDA_MDAC
C237 1u
C172 0.1
C173 0.1
C391 0.1

VDDA_DRE
VDDA_MDAC
U21
COLUTA_V4_SOCKET
R115 100

CV4_IN1_P 1 IN1_P
CV4_IN1_N 2 IN1_N
CID_2 3 CID[2]
CV4_IN2_P 4 IN2_P
CV4_IN2_N 5 IN2_N
6 VDDA_MDAC14_4
CV4_IN3_P 7 IN3_P
CV4_IN3_N 8 IN3_N
CV4_IN4_P 9 IN4_P
CV4_IN4_N 10 IN4_N
11 VDDA_MDAC14_1
VREFN_BYP 12 VREFN_BYP
VDD_BGP 13 VDD_BGP
VREFP_BYP 14 VREFP_BYP
15 VDDA_MDAC58_1
CV4_IN5_P 16 IN5_P
CV4_IN5_N 17 IN5_N
CV4_IN6_P 18 IN6_P
CV4_IN6_N 19 IN6_N
20 VDDA_MDAC58_2
CV4_IN7_P 21 IN7_P
CV4_IN7_N 22 IN7_N
CID_1 23 CID[1]
CV4_IN8_P 24 IN8_P
CV4_IN8_N 25 IN8_N

MDAC14_VREFP_IN 100
MDAC14_VCM_IN 99
MDAC14_VREFN_IN 98
CID_3 97
VDDA1_SAR 96
SAR1_N 95
SAR1_P 94
VDDA2_SAR 93
SAR14_VREFN 92
SAR14_VREFP 91
SAR14_VCM 90
VDDA3_SAR 89
VDDD_SAR 88
RSTB 87
IBIAS_EXT 86
VDD_TS 85
TP1_VIO1 84
TP2_VIO2 83
TP3_VOUTN 82
TP4_VOUTP 81
BCR_AUX_N 80
BCR_AUX_P 79

VDDA_MDAC14_3 26
VDDA_MDAC14_2 27
MDAC14_VREFP_IN 28
MDAC14_VCM_IN 29
MDAC14_VREFN_IN 30
CID[3] 31
VDDA1_SAR14 32
SAR1_N 33
SAR1_P 34
VDDA2_SAR14 35
SAR14_VREFN 36
SAR14_VREFP 37
SAR14_VCM 38
VDDA3_SAR14_3 39
VDDA3_SAR14_2 40
VDDD_SAR14 41
RSTB 42
IBIAS_EXT 43
VDD_TS 44
TP1(VIO1) 45
TP2(VIO2) 46
TP3(IOA_VOUTP) 47
TP4(IOA_VOUTN) 48
BCR_AUX_N 49
BCR_AUX_P 50

FRAME1_P 75 FRAME1_P
FRAME1_N 74 FRAME1_N
VDDD_DDPU3 73
DATA1_P 72 DATA1_P
DATA1_N 71 DATA1_N
DATA2_P 70 DATA2_P
DATA2_N 69 DATA2_N
SCL 68 SCL
DATA3_P 67 DATA3_P
DATA3_N 66 DATA3_N
DATA4_P 65 DATA4_P
DATA4_N 64 DATA4_N
VDDD_DDPU2 63
DATA5_P 62 DATA5_P
DATA5_N 61 DATA5_N
DATA6_P 60 DATA6_P
DATA6_N 59 DATA6_N
SDA 58 SDA
DATA7_P 57 DATA7_P
DATA7_N 56 DATA7_N
DATA8_P 55 DATA8_P
DATA8_N 54 DATA8_N
VDDD_DDPU1 53
FRAME8_P 52 FRAME8_P
FRAME8_N 51 FRAME8_N
GND 101
VDDD_DDPU

VDDD_DDPU
R204 1k
H80 HEADER_50MIL
CID_3
R205 1k
H81 HEADER_50MIL
CID_2
R206 1k
H82 HEADER_50MIL
CID_1
R207 1k
H83 HEADER_50MIL
CID_0
R141 1k
SDA
SCL
T51 KEYSTONE_TP
T28 KEYSTONE_TP
T30 KEYSTONE_TP

LVDS_E_3R to SLVS convertor

R59 120
BC_RST_P
R52 470
BCRST_P
BCRST_N
BC_RST_N
R58 470
R149 120

VDDD_DDPU
C390 0.1
C153 10uF
C2510u
C24 10uF

VDD_CLK
C19 10u
C16 10u
C144 0.1

VDD_TS
C330 1u
C18 1u
C31 0.1

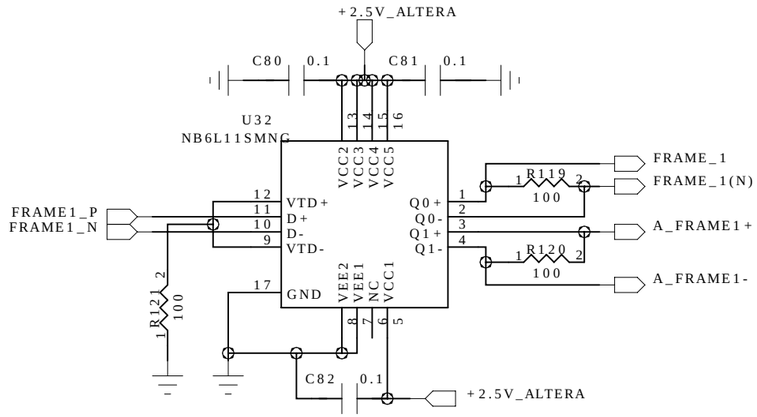
VDD_BGP
C92 1u
C17 0.1

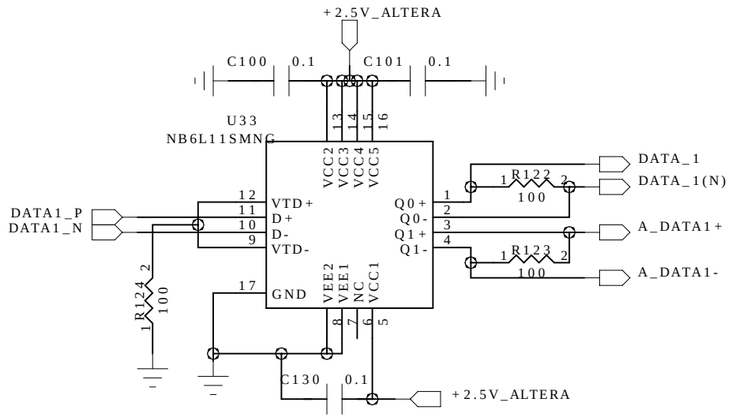
VDDD_SAR
C27 1u
C94 0.1
C95 0.1

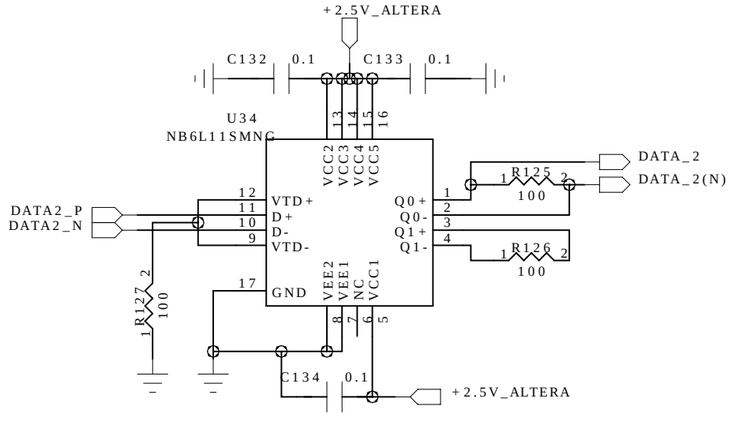
BCR_AUX_+
R109 120
R103 470
BCR_AUX_P
BCR_AUX_-
R108 470
BCR_AUX_N
R110 120

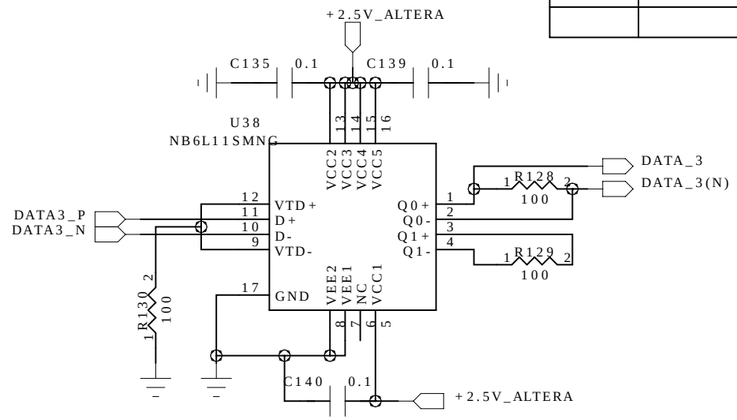
DRAWN: jb/2019	DATED:	COMPANY: Nevis Laboratories of Columbia University	
CHECKED:	DATED:	TITLE: COLUTA4 test board	
QUALITY CONTROL:	DATED:	CODE:	SIZE: B
RELEASED:	DATED:	DRAWING NO: v0	REV: 0
		SCALE:	SHEET: 9 25

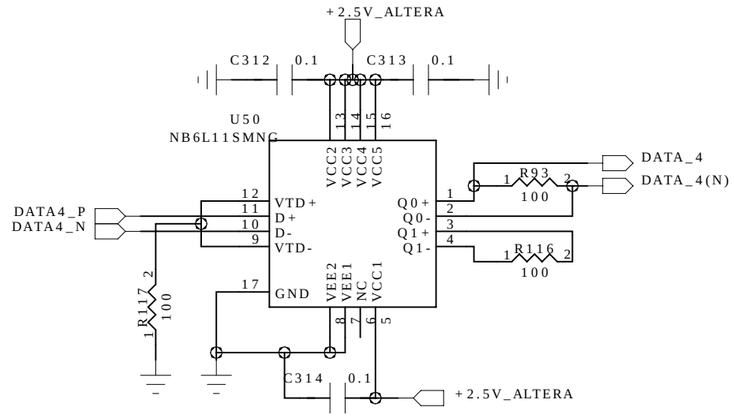
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:











DRAWN: jb/2019	DATED: jb/2019	COMPANY: Nevis Laboratories of Columbia University	
		TITLE: COLUTA4 test board	
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: B
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: v0	REV: 0
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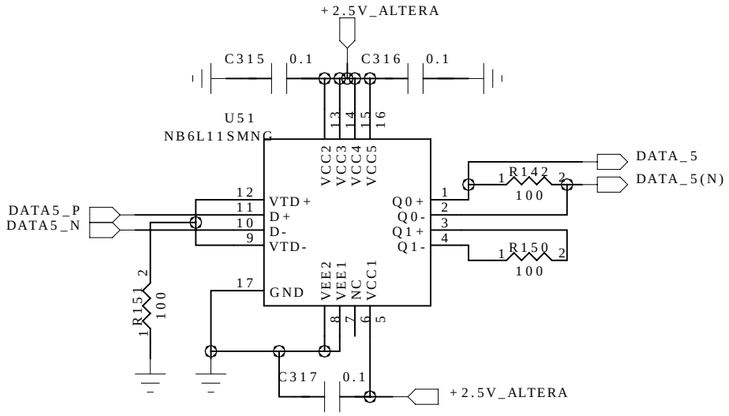

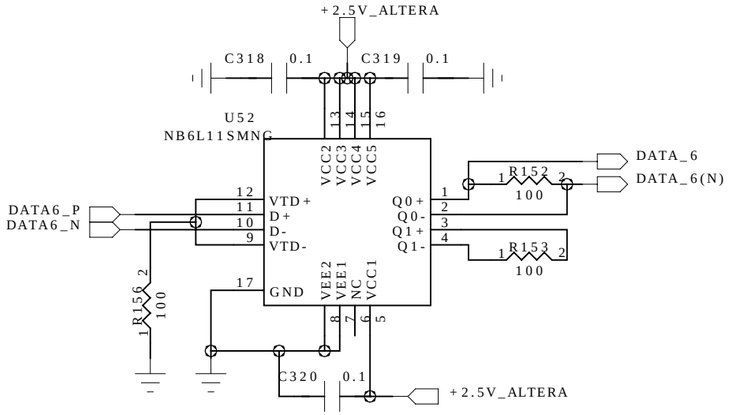

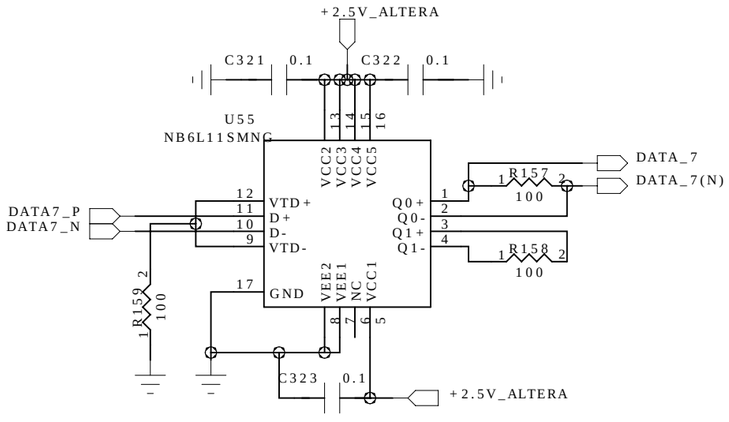

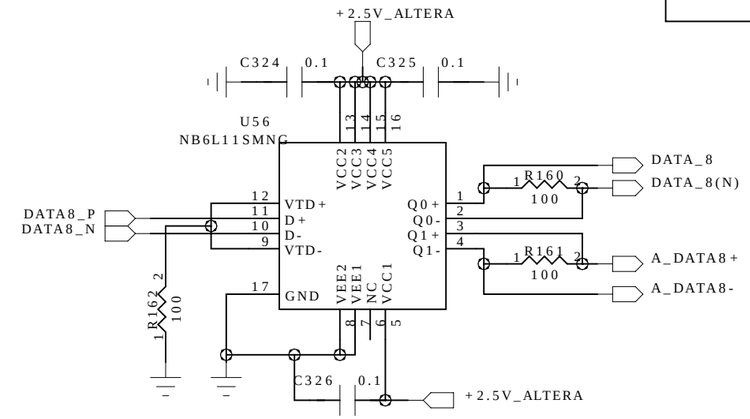

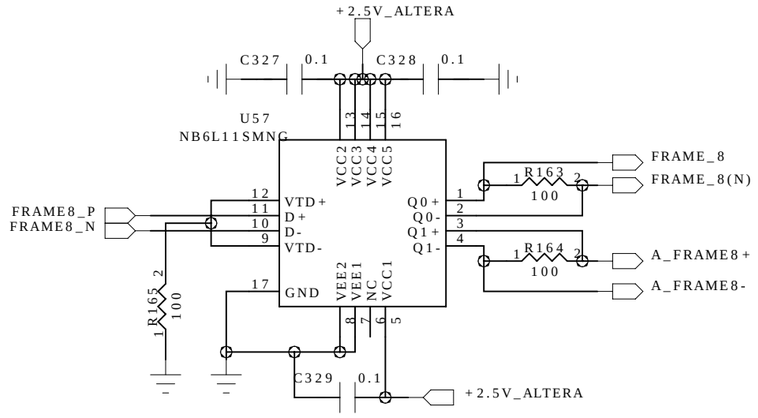

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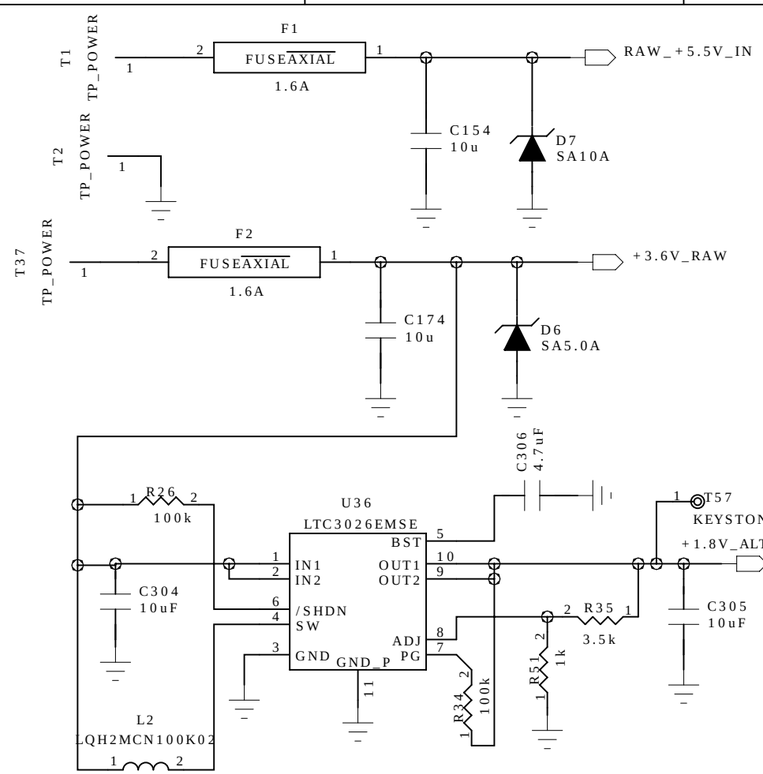

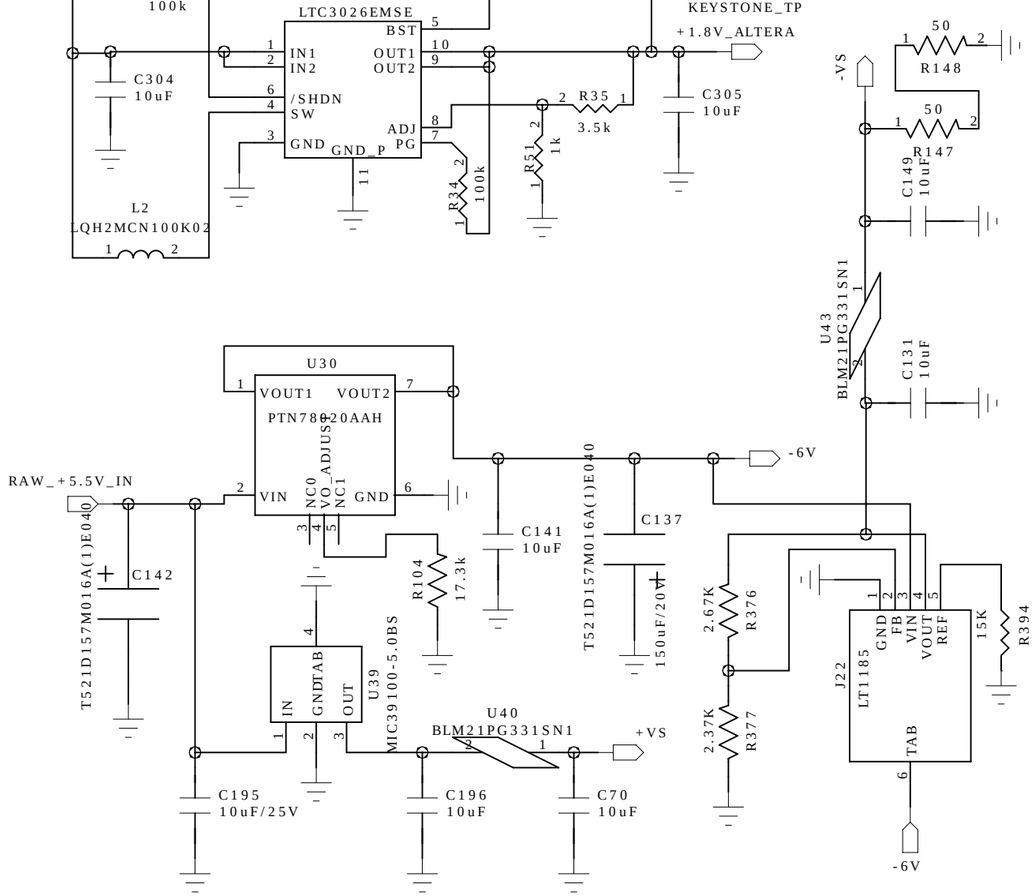

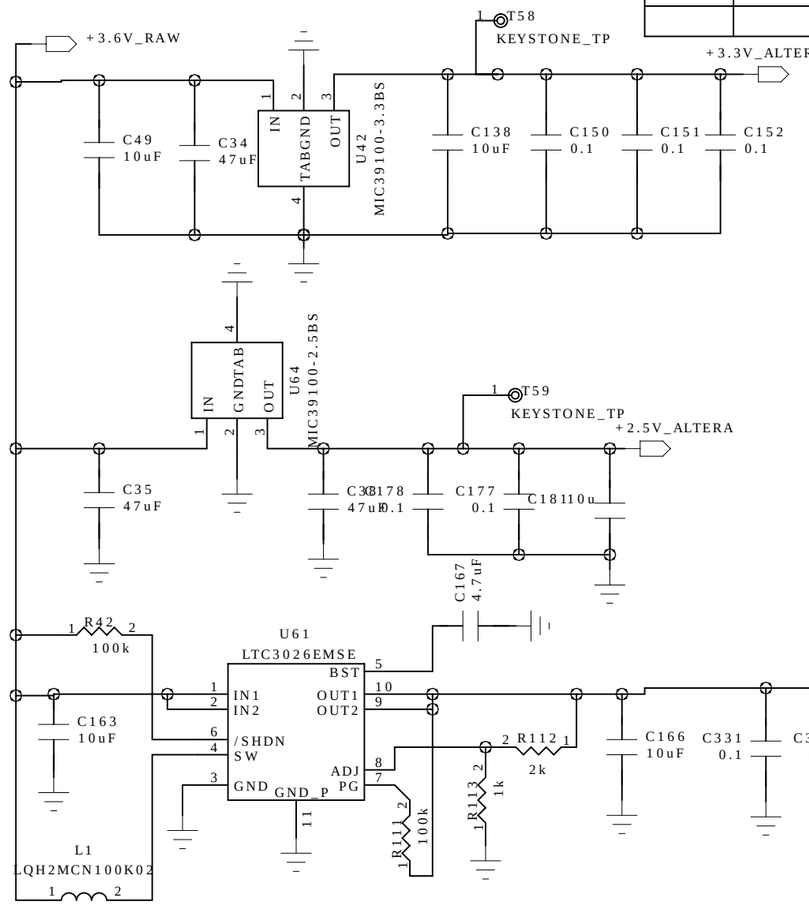

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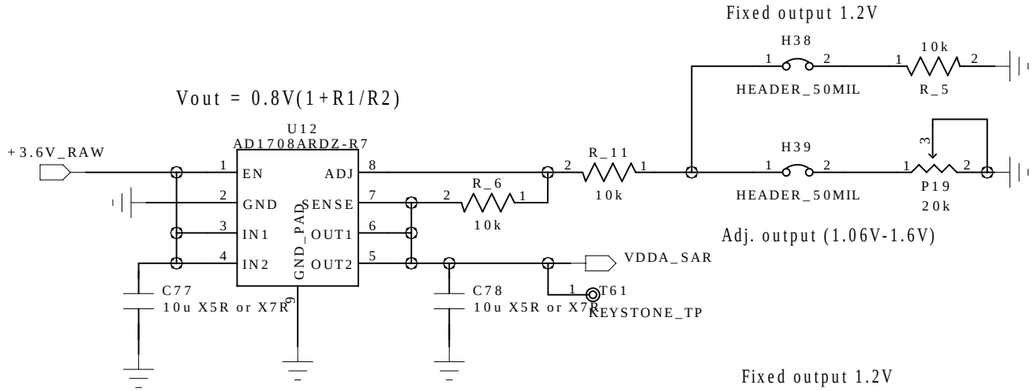

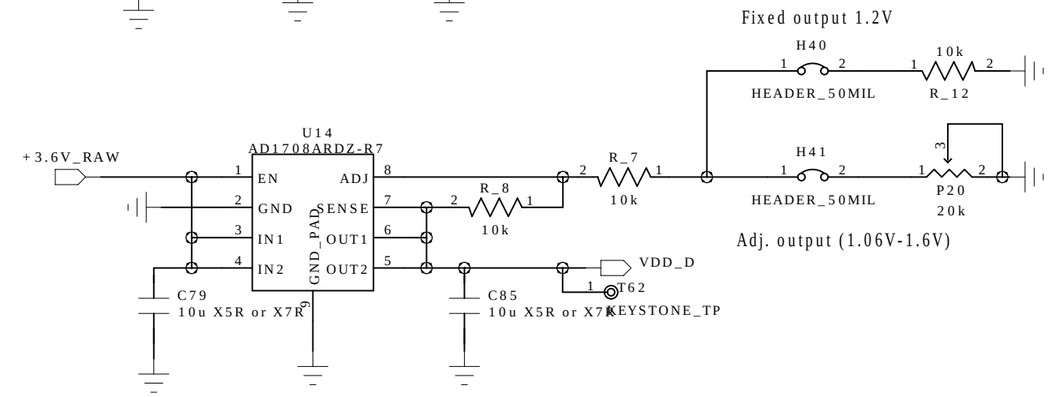

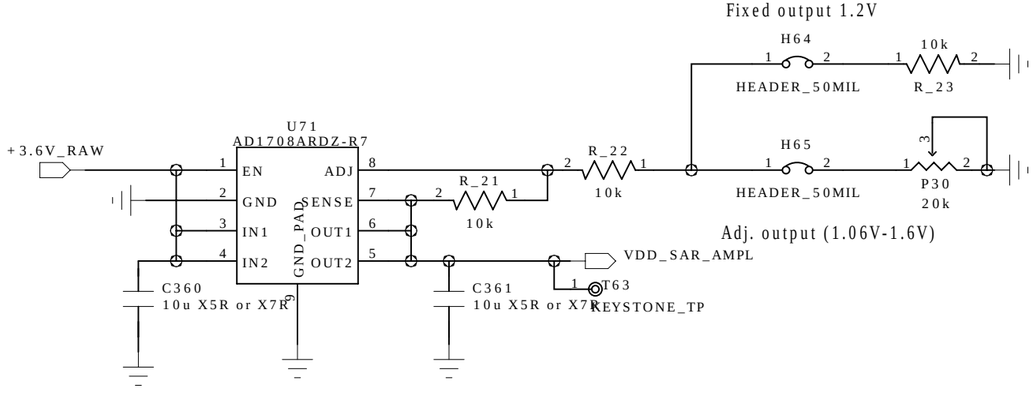

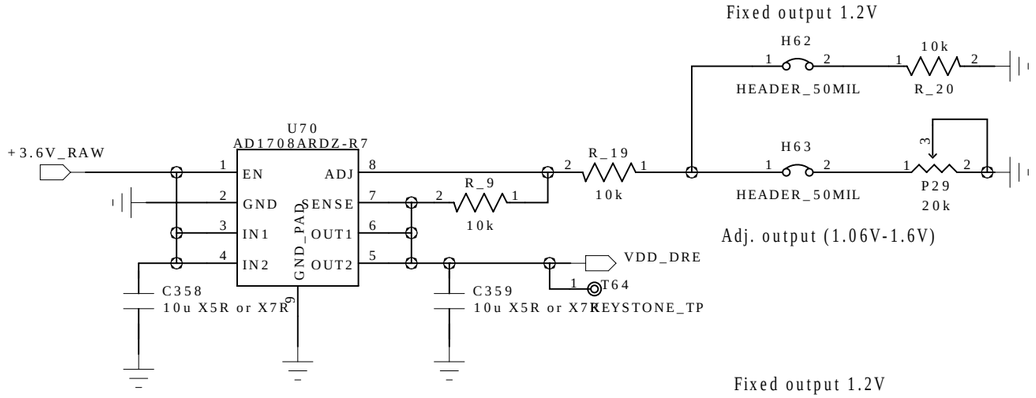

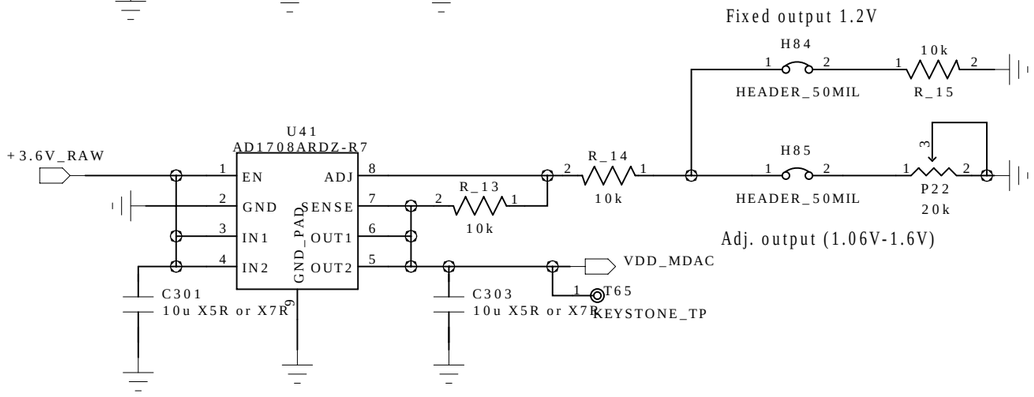

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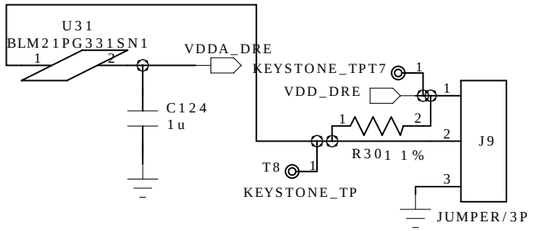

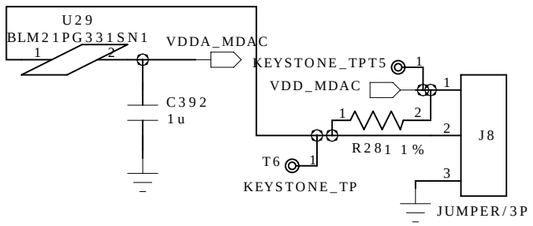

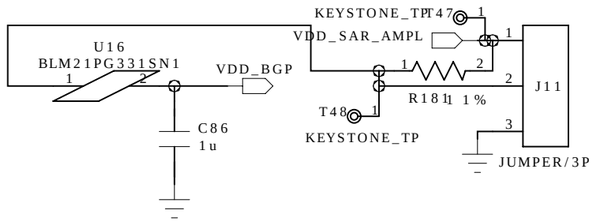

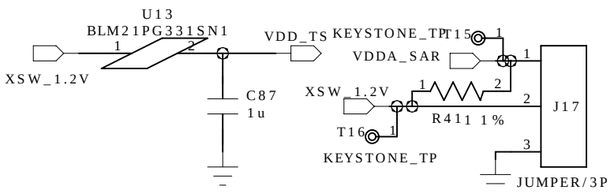

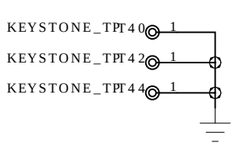

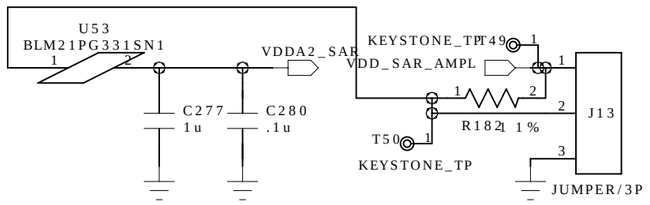

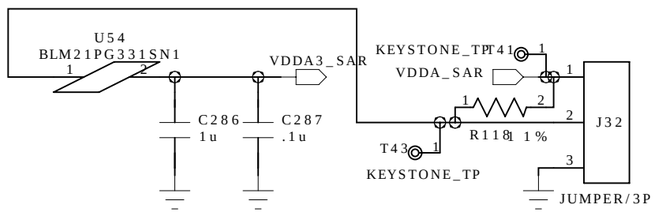

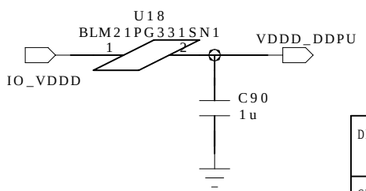

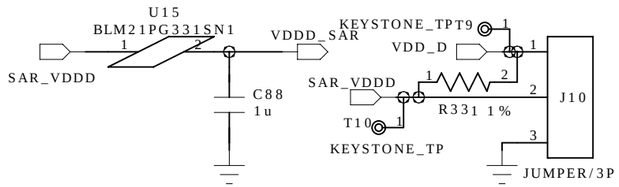

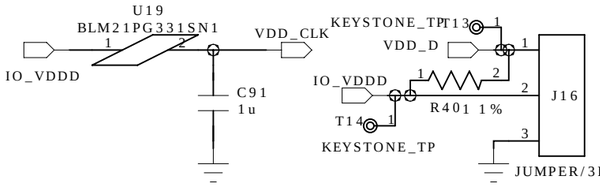

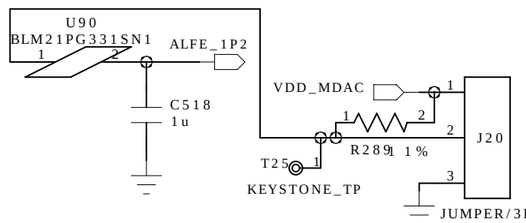

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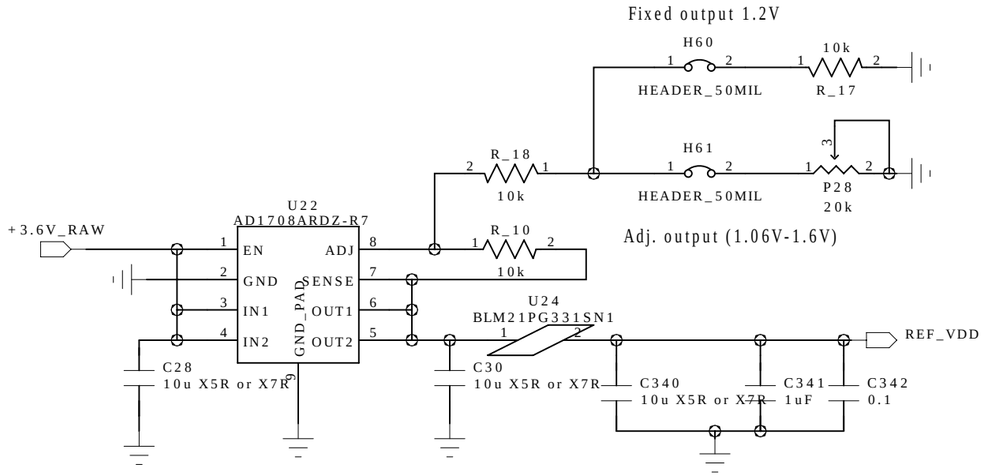

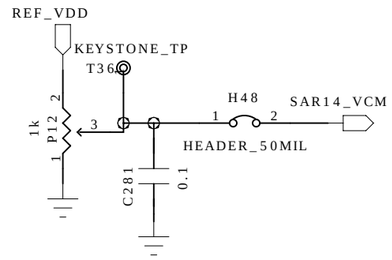

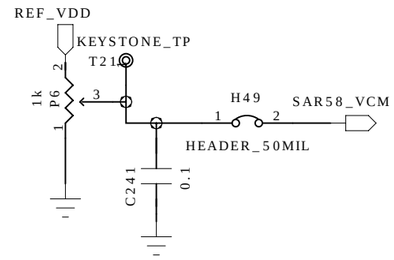

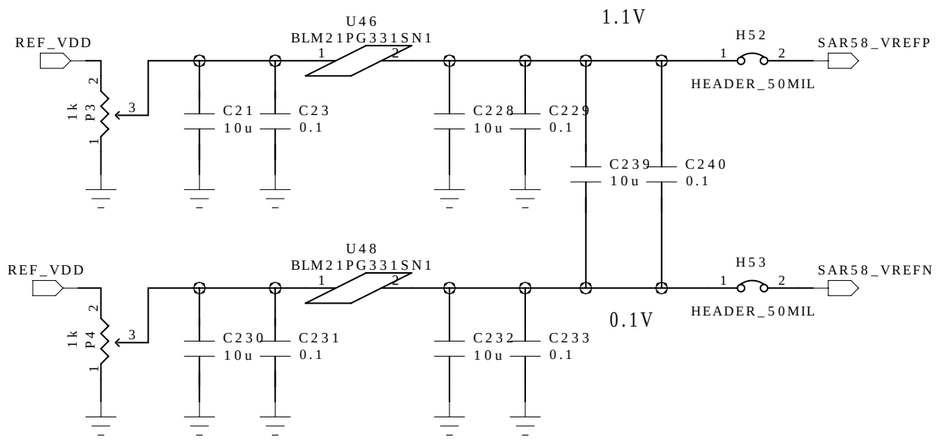

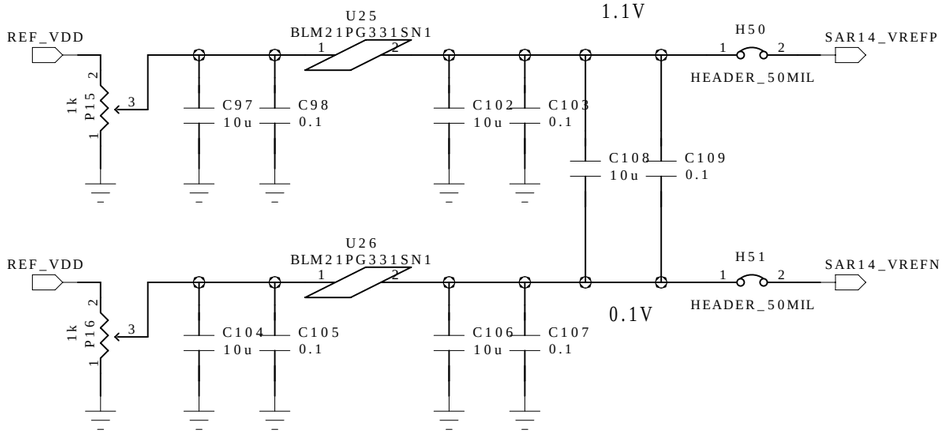

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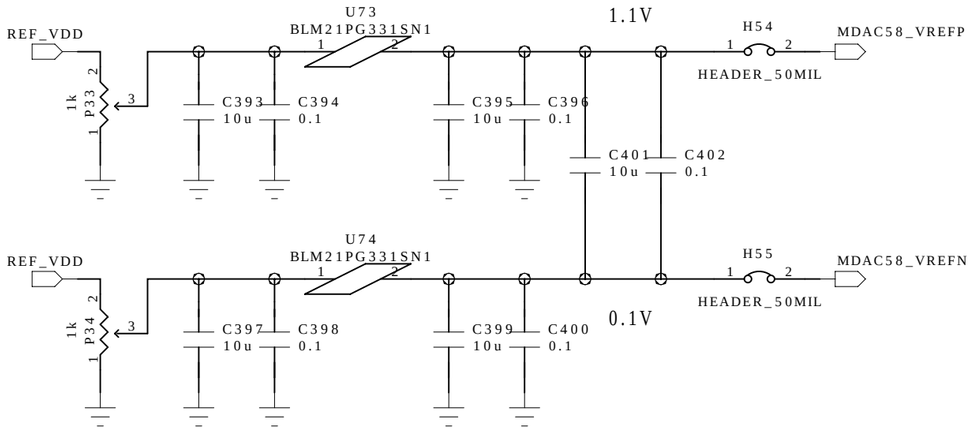

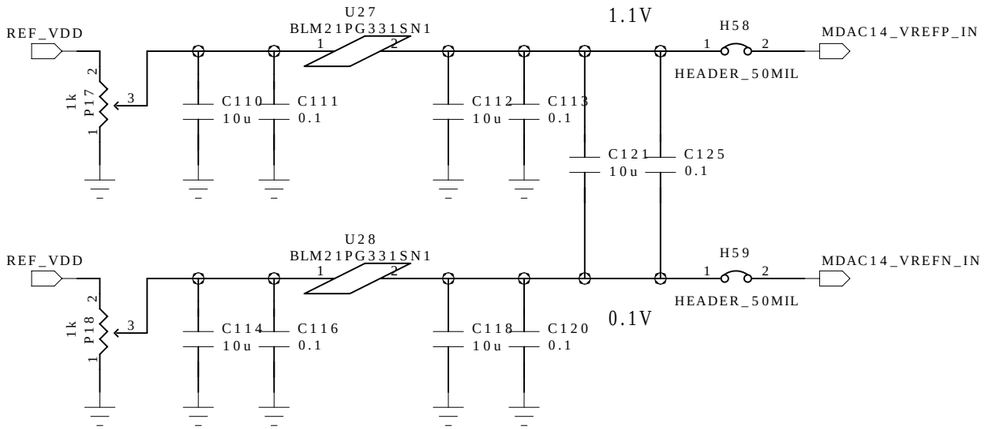

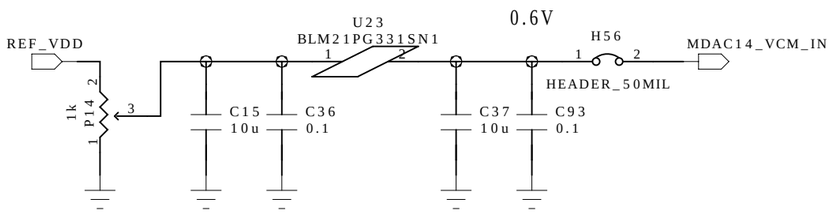

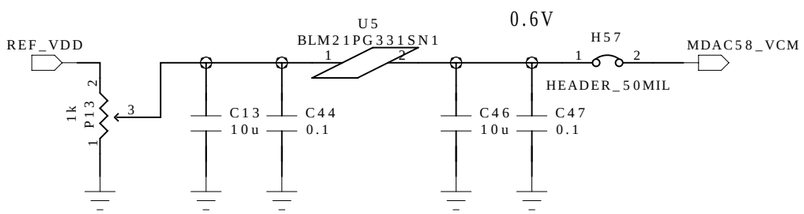

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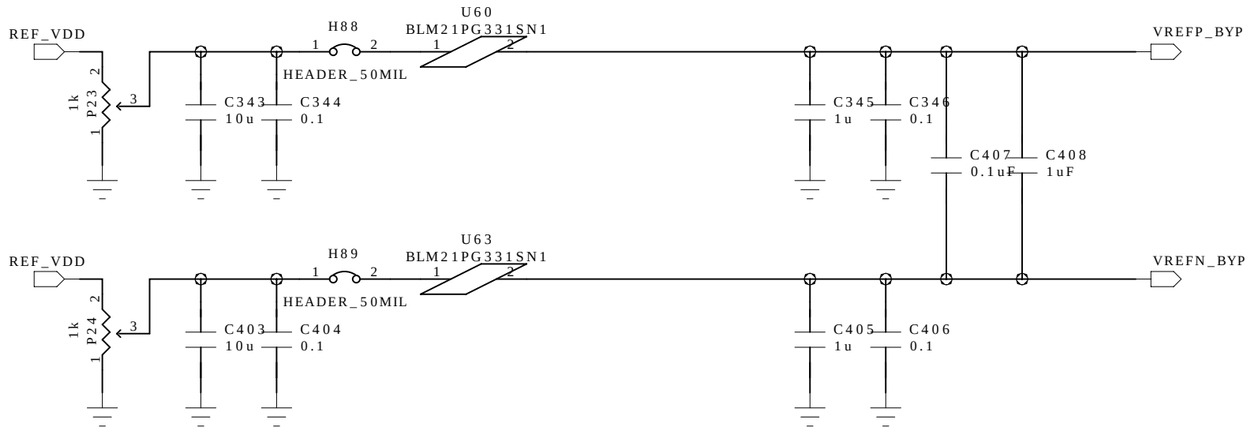

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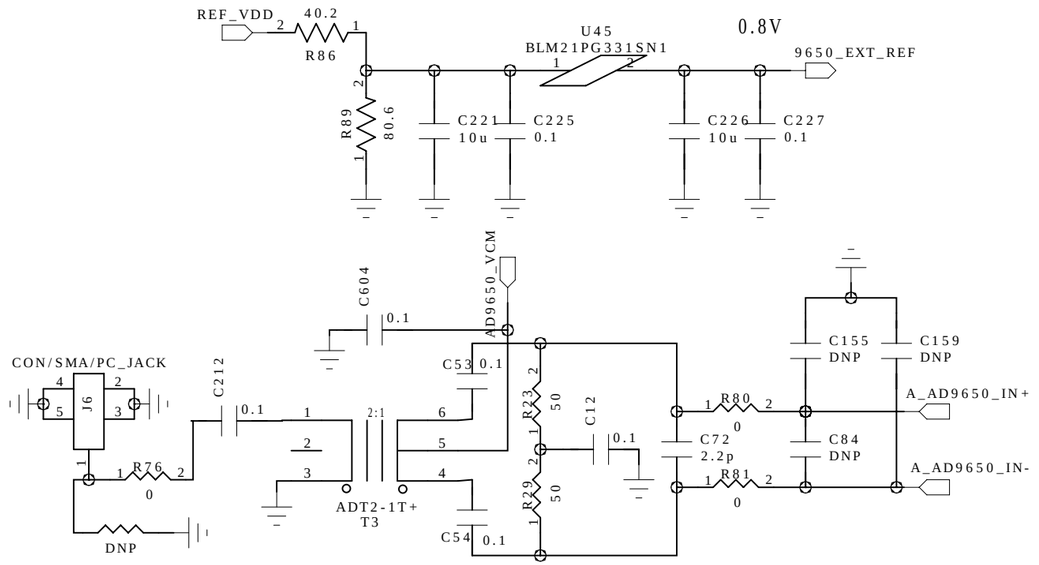

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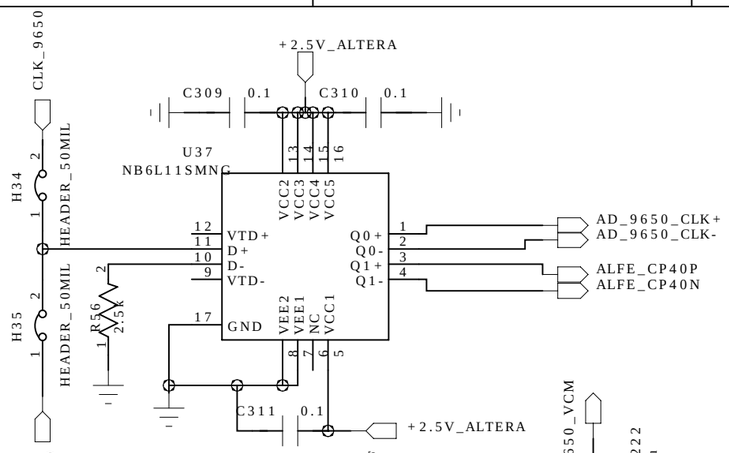

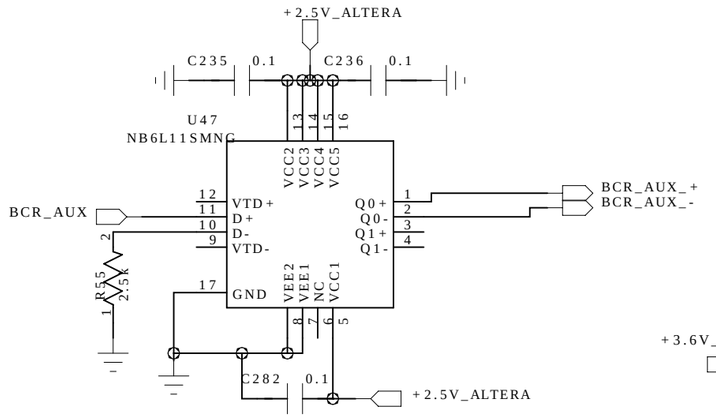

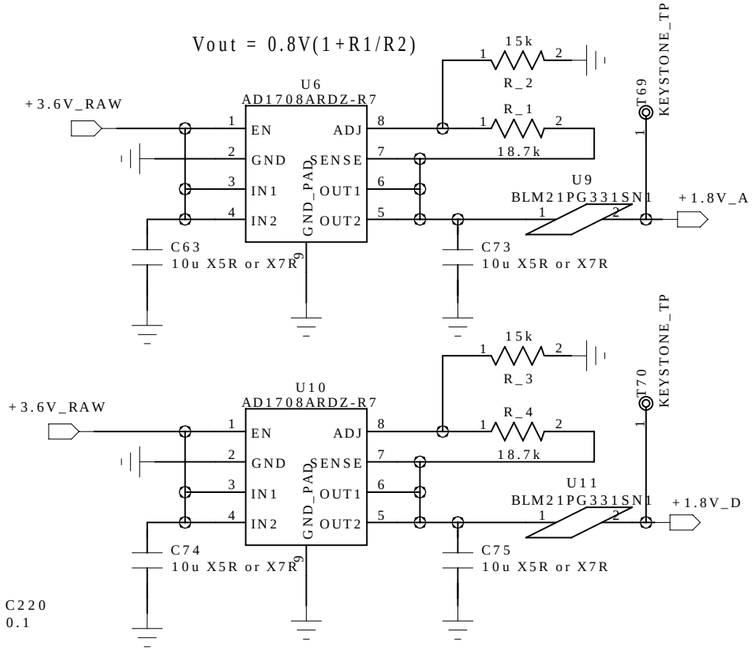

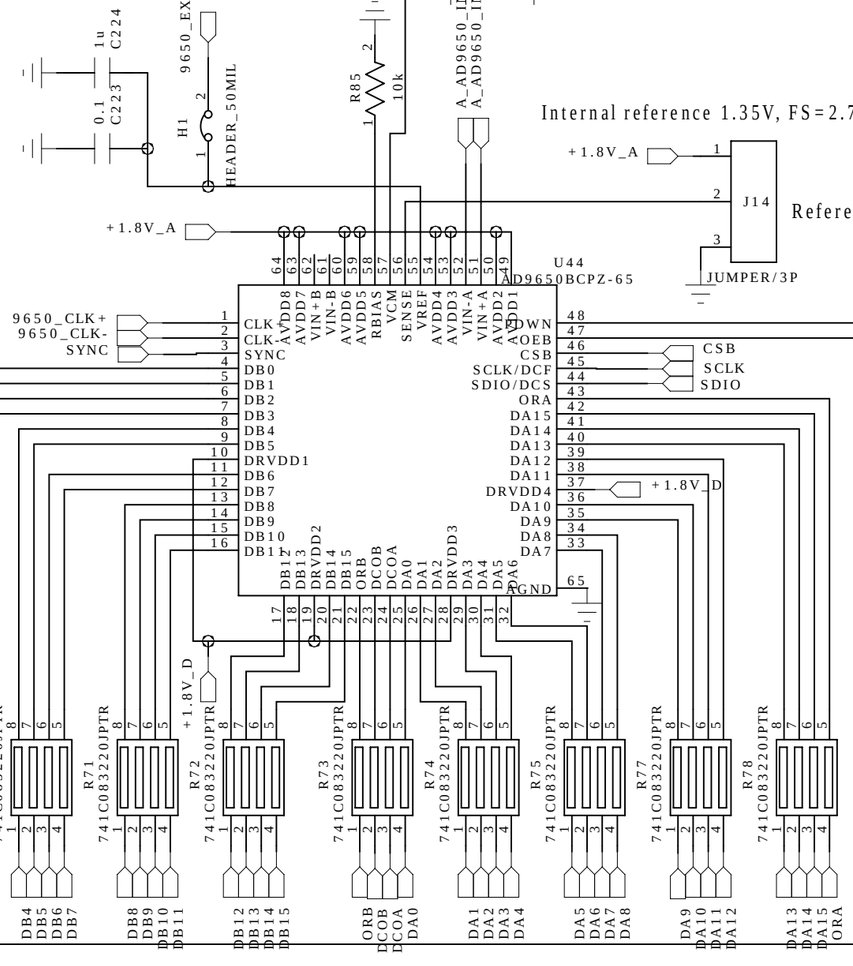

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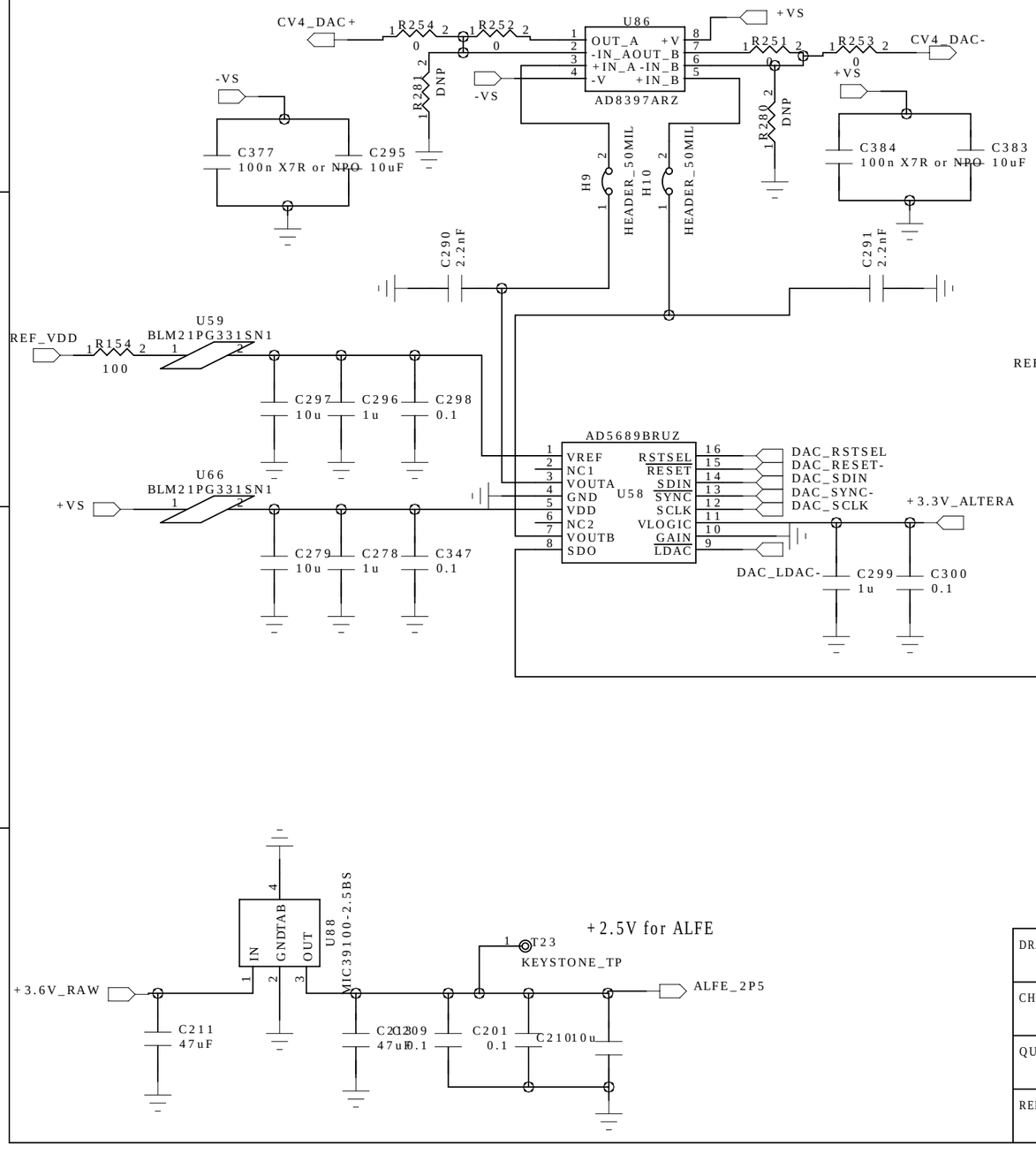

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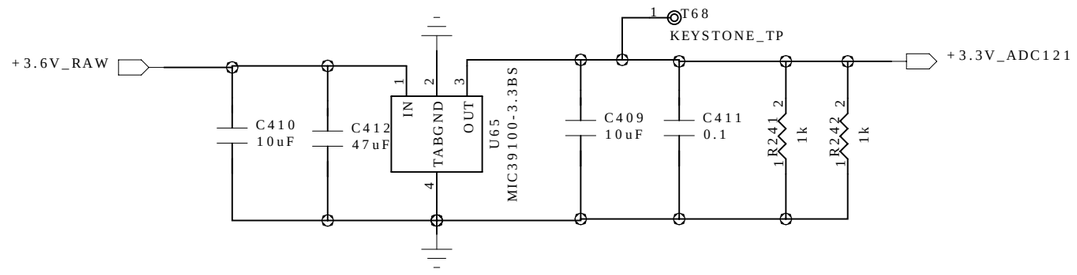

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H92 2 1 CP
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TP1_VIO1

KEYSTONE_TP T31
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HEADER_50MIL R234
H94 2 1 AN
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H95 2 1 BN
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VMIO
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2 50 1 R209
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U75 ADA4817-1ACPZ
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-VS
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R167 348 1 2
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KEYSTONE_TP T53
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VA
GND
VIN
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R173 1 2 50
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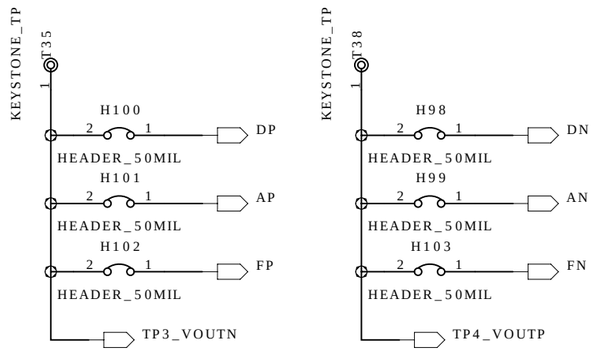

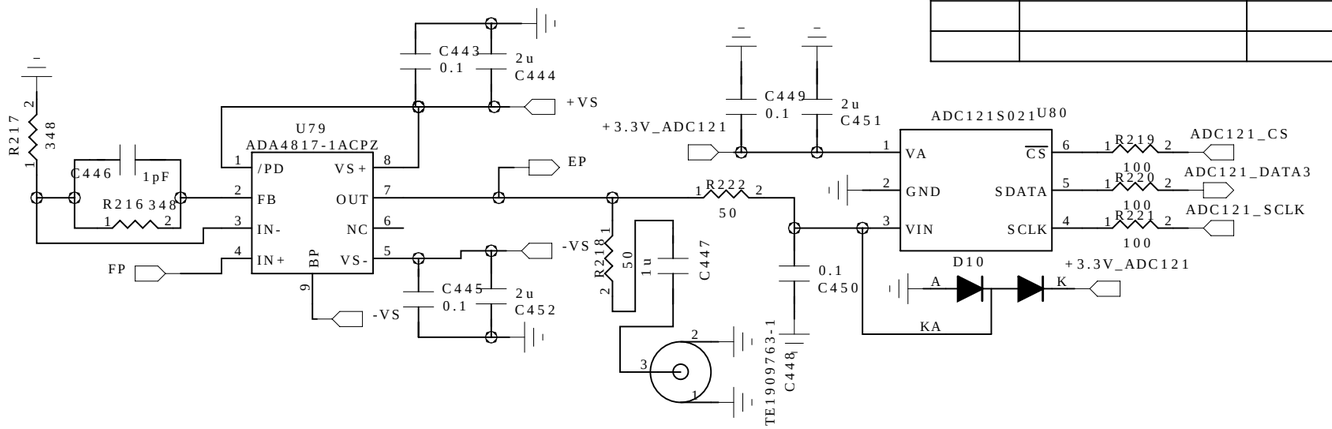

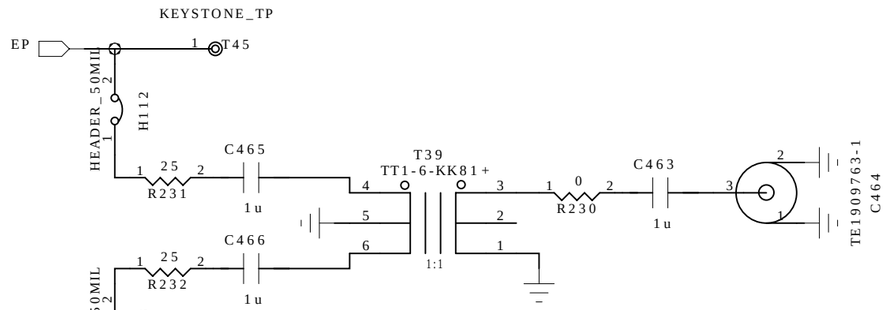

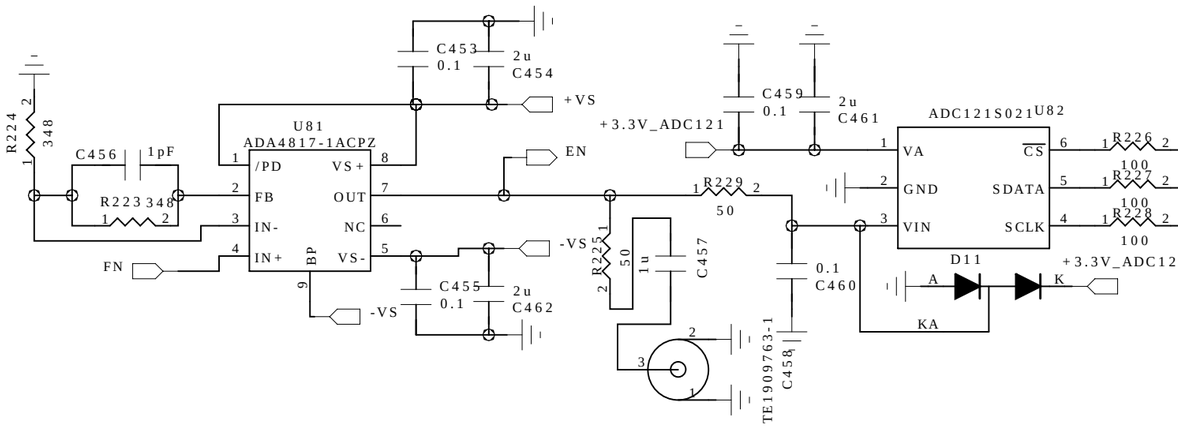

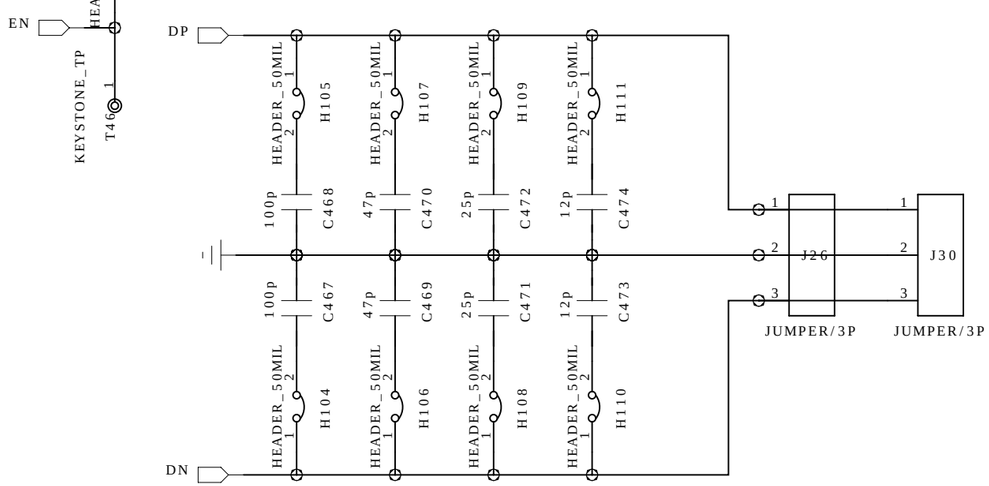

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REVISION RECORD			
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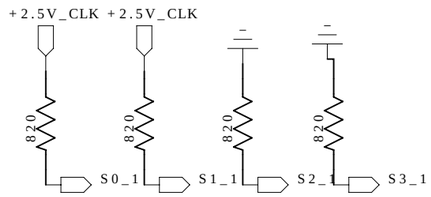

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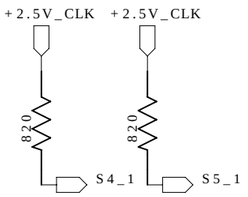
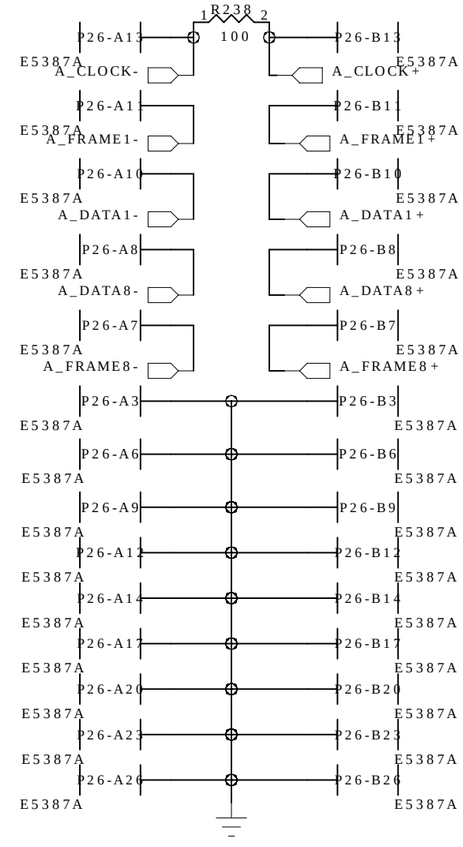


all ouputs are LVDS



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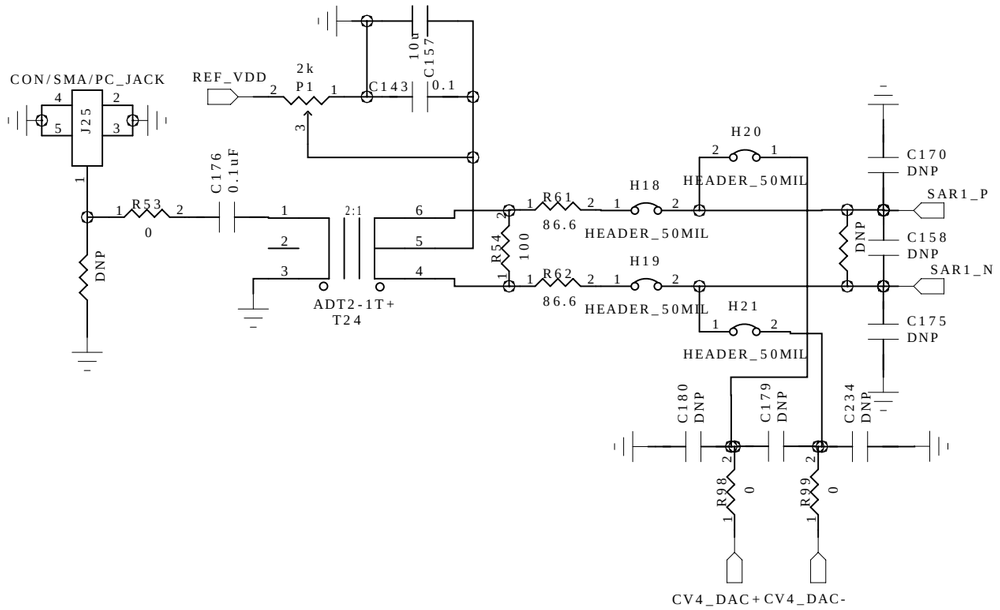

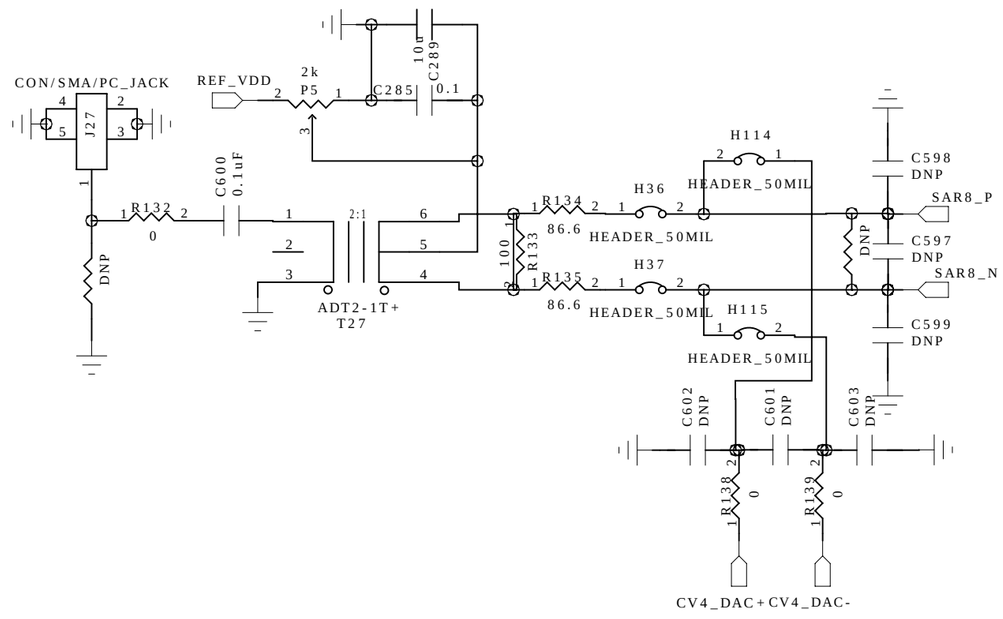

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