# ALFE2 datasheet

ALFE2 is a 4-channel low noise analog front-end ASIC designed for the readout of Liquid Argon Calorimeter in the ATLAS detector on the HL-LHC. The output will be digitized by a 14-bit ADC with a sampling rate of 40 MSPS. Two different gains can be read out simultaneously to provide full dynamic range coverage and optimum resolution for small signals.

# Revisions

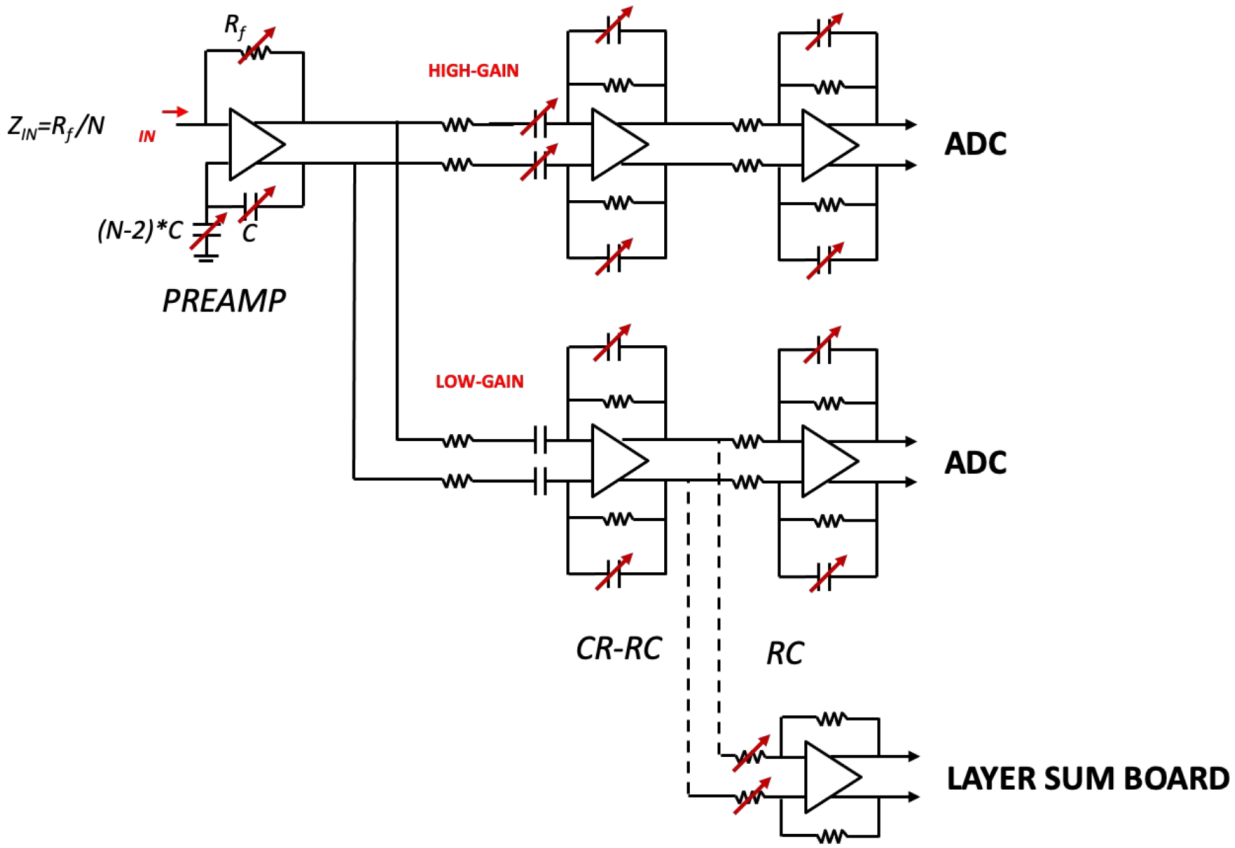
| Revision number | Key changes | Drafted by | Revision date |
|---|---|---|---|
| 0.1 | Initial draft | D. Matakias | 4/20/2022 |

# Table of contents

# Introduction

ALFE2 is the prototype analog front-end ASIC for the readout of Liquid Argon Calorimeter in the ATLAS detector on the HL-LHC. The primary goal of this prototype is to integrate the BGR and DAC for internal biasing without the need of implementing external current sources. It also integrates the I2C block from OMEGA for slow control and automatic configuration after reset.
ALFE2 comprises: four front-end (FE) channels, where each of them contains a preamplifier (PA), CR-RC2 shaper (SH) with two separate gain paths: Low-Gain (LG) and High-Gain (HG); Trigger sum (SUM) output with CR-RC shaping stage, configurable gain and channel switch; Bias networks generating bias voltages for the PA and SH; Slow-control block - implemented by means of I2C.

# Block diagram



# Power domains

ALFE2 power domains are listed in the following table:

| Power rail pin names | Voltage (V) | Nominal Current (mA) | Domain | Notes |
|---|---|---|---|---|
| VCC1V2_DAC | 1.2 | 5 | Digital | Internal DAC supply. |
| VCC1V2_I2C | 1.2 | | | I2C block supply. |
| VCC1V2_PA | 1.2 | 85 | 1.2 PA | PA input stage |
| VCC2V5_PA | 2.5 | 102 | 2.5 PA | PA output stage. Increases by ~3mA for 25 Ohm configuration |
| VCC1V2_SH_LG | 1.2 | 101 | Shaper | Shaper low gain channels |
| VCC1V2_SH_HG | | 91 | | Shaper high gain channels |
| VCC1V2_SH_TS | | 18 | | Shaper trigger sum. Increases by ~4mA when channel gains are set to 3. |

## Shaper power domain note

The shaper power supply has been split into high gain, low gain and trigger sum on ALFE2. This was done to mitigate potential crosstalk from high gain to low gain and trigger sum when the high gain saturates.
**Since there are internal connections (current mirrors) between high gain, low gain and trigger sum, it is critical to connect these pins all together on the same power plane.** Any voltage difference between these pins will be amplified and appear as noise on the output stage of ALFE2.

## Recommended power planes

Splitting the power rails should be done for debugging tests. In the final configuration of ALFE2, only 2 power planes will be used, 1.2V and 2.5V.
The I2C and DAC may be optionally isolated from the 1.2V power plane with a ferrite bead (tests on the ALFE2 prototype board did not yield any performance difference).

# Functional description

## Input stage (PA)

## Output stage (SH)

## Trigger sum (SUM)

## Control interface ( I2C block from OMEGA)

## Biasing network and internal reference

ALFE2 needs 3 bias currents to properly bias the internal circuits. These currents have a nominal value of 1 mA. The power consumption of ALFE2 is linearly dependent on the biasing current's value.

### Monitoring bias currents

The user may monitor the bias current nets indirectly by measuring the voltage on the following pins:

- n1mAi_pa: 1V2_PA domain bias current
- p1mAi_2p5_pa: 2V5_PA domain bias current
- n1mAi_sh: 1V2_SH and 1V2_SUM domain bias current

### Internal bias circuit

ALFE2 contains a triple channel 6-bit internal DAC and a BGR to generate the DAC reference voltage. This circuit can be used for ALFE2 biasing. This is the intended mode of operation.

### External reference voltage

The user may choose to bypass the BGR and provide the DAC reference voltage externally on the ext_vref_dac pin. This is intended for debugging. To switch to external reference voltage follow these steps:

- Configure ALFE2 control register "*bgr_sel*" to 0b11. (I2C address 0x0E, [7:6] This will disconnect the BGR from the internal DAC and connect the ext_vref_dac pin.
- Provide ~320mV to the ext_vref_dac pin. A resistor voltage divider may be used. It is recommended to connect a small capacitor (e.g. 10nF) to filter the input voltage.
- As a rule of thumb the chip power consumption must be very close to the default biasing option (BGR). Higher or lower power consumption indicates that the external reference voltage must be adjusted.

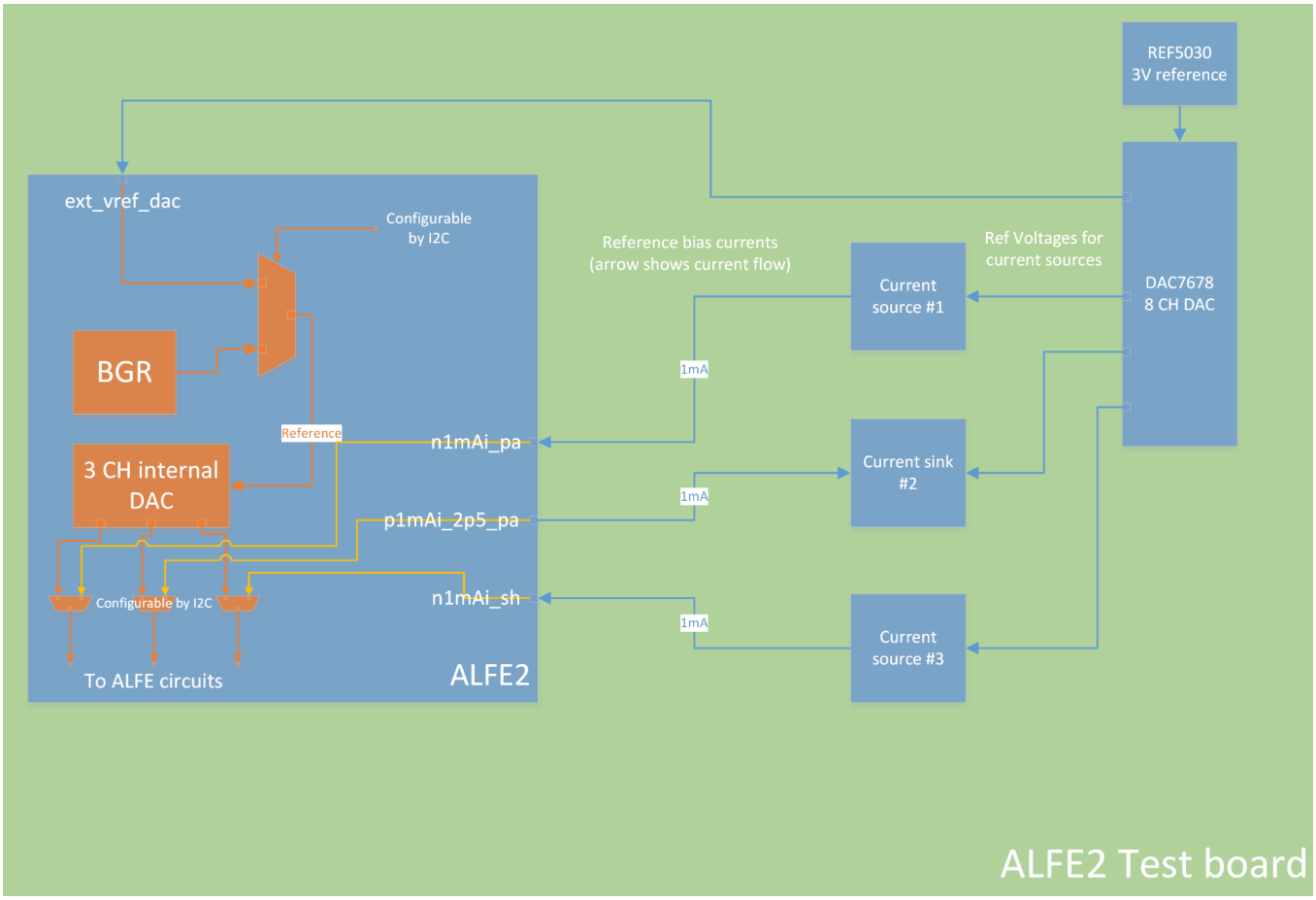
## Bypassing the internal DAC

ALFE2 can be configured to use external bias currents for any or all power domains. This is intended for debugging. In this case both the internal DAC and BGR are not used and disconnected. To use external bias currents follow these steps: (example is for all 3 bias currents)

- Configure ALFE2 control registers:
  - "*pa1v2_cur*" to 0b0 to provide external bias current to the 1V2_PA domain.
  - "*sh1v2_cur*" to 0b0 to provide external bias current to the 1V2_SH and 1V2_SUM domains.
  - "*pa2v5_cur*" to 0b0 to provide external bias current to the 2V5_PA domain.
- Depending on which registers are configured:
  - Connect 1mA **current source** to pin n1mAi_pa for the 1V2_PA domain.
  - Connect 1mA **current source** to pin n1mAi_sh for the 1V2_SH and 1V2_SUM domains.
  - Connect 1mA **current sink** to pin p1mAi_2p5_pa for the 2V5_PA domain.

## Biasing network block diagram and external circuits

The following block diagram shows the ALFE2 internal DAC and BGR as well as the external circuits used to bypass the DAC/BGR or provide external reference voltage to the DAC.

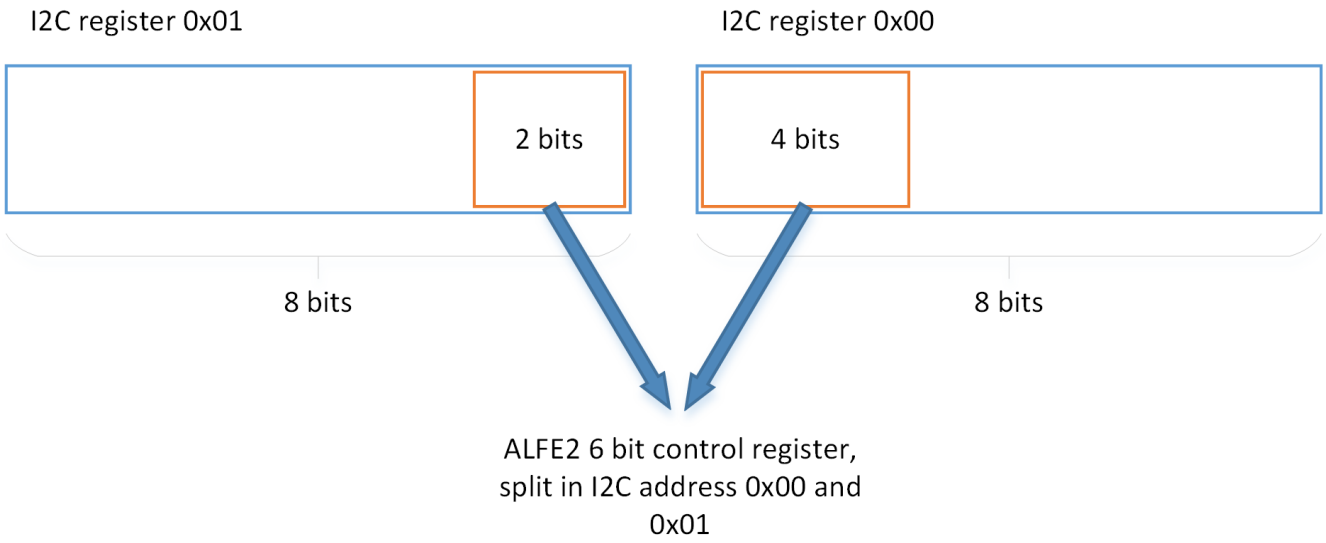


# Wire Bonding Pad and Package Pin List

# ALFE2 Control registers

ALFE2 has 16 8-bit I2C registers. All 128 bits can be read and written by the user. ALFE2 uses unary coding or thermometer code for most of its control registers. For the remaining registers the bits adjusted by the I2C block are used to directly interface with the ALFE2 circuits. (e.g. enable signal)
**Some ALFE2 control registers are split into multiple I2C registers. Therefore multiple I2C transactions are necessary to access them.**

## Example of an ALFE2 control register being split in 2 I2C registers




*This figure is presented as an example. The highlighted bits do not correspond to an actual ALFE2 control register.*

## I2C Register 0x00

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x00 | ch_pwr | Channel power down register. Each bit represents one channel.<br>0b0 channel is powered on<br>0b1 channel is powered off<br>The most significant bit of the register corresponds to channel 3.<br>[ CH3, CH2, CH1, CH0 ] | [3:0] | 0x0 |
| | pa_fb_r0 | Sets the preamplifier feedback resistance #0. Used to switch between 50 Ohm and 25 Ohm mode.<br>0b01 50 Ohm mode<br>0b11 25 Ohm mode | [5:4] | 0b01 |

| | | | | |
|---|---|---|---|---|
| | pa_fb_c0 | Sets the preamplifier feedback capacitance #0. Used to switch between 50 Ohm and 25 Ohm mode.<br>0b01 50 Ohm mode<br>0b11 25 Ohm mode | [7:6] | 0b01 |

## I2C Register 0x01

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x01 | pa_out_offset | Sets the offset current at the preamplifier output. Used to switch between 50 Ohm and 25 Ohm mode.<br>0x1 50 Ohm mode<br>0xF 25 Ohm mode | [3:0] | 0x1 |
| | pa_fb_c1 | Sets the preamplifier's feedback capacitance #1. Used to switch between 50 Ohm and 25 Ohm mode.<br>0b01 50 Ohm mode<br>0b11 25 Ohm mode | [5:4] | 0b01 |
| | imped_coarse | Input impedance coarse tuning. Used to switch between 50 Ohm and 25 Ohm mode.<br>0b11 50 Ohm mode<br>0b00 25 Ohm mode | [7:6] | 0b11 |

## I2C Registers 0x02, 0x03, 0x04

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x02,<br>0x03,<br>0x04 | imped_fine | Input impedance fine tuning. The tuning of the input impedance is done to account for process variations that might affect the input impedance of the chip. The register uses unary coding. Only 22 different values are possible. The register is split between 3 I2C addresses. To read/write this register all of these I2C registers must be accessed.<br>0x0007FF 50 Ohm mode<br>0x000FFF 25 Ohm mode | 0x04: [4:0]<br>0x03: [7:0]<br>0x02: [7:0] | 0x0000FF |

## I2C Registers 0x04, 0x05, 0x06

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x04 | pa_fb_r1 | Sets the preamplifier feedback resistance #1. Used to switch between 50 Ohm and 25 Ohm mode.<br>0b1 50 Ohm mode<br>0b0 25 Ohm mode | [5] | 0b1 |
| 0x04, 0x05 | pa_output_dc | Fine adjustment of the preamplifier output DC level. | 0x05: [5:0]<br>0x04: [7:6] | 0x1F |
| 0x05, 0x06 | sh_pt | Adjusts the shaper peaking time. The register uses unary coding. Only 11 values are possible. | 0x06: [7:0]<br>0x05: [7:6] | 0x01F |

## I2C Registers 0x07, 0x08

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x07 | en_sh_lg_gain_boost | Tune the LG output gain on the shaper stage. This option is intended to be used for the 25 Ohm configuration. This option does not affect the high gain outputs. The peaking time is slightly affected.<br>0b1 Enable gain boost<br>0b0 Disable gain boost | [0] | 0b0 |
| 0x07, 0x08 | sh_output_dc | Adjusts the DC level of the output pins. The register uses unary coding. Only 16 different DC levels are possible. | 0x08: [7:0]<br>0x07: [7:1] | 0x03FF |

## I2C Register 0x09

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x09 | sh_sum_pwr | Sum power down register.<br>0b0 sum is powered on<br>0b1 sum is powered off | [0] | 0b0 |
| | sh_sum_gain_ch0 | Individual control of the gain of each channel for the sum output. The register uses unary coding. Only 4 different values are possible. | [3:1] | 0b001 |
| | sh_sum_gain_ch1 | | [6:4] | 0b001 |

## I2C Register 0x09 (continued), 0x0A, 0x0B, 0x0C

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x09, 0x0A | sh_sum_gain_ch2 | Individual control of the gain of each channel for the sum output. The register uses unary coding. Only 4 different values are possible. | 0x0A: [1:0]<br>0x09: [7] | 0b001 |
| 0x0A | sh_sum_gain_ch3 | | [4:2] | 0b001 |
| 0x0A, 0x0B, 0x0C | sh_sum_output | Adjusts the DC level of the sum pin. The register uses unary coding. Only 16 different DC levels are possible. | 0x0C: [3:0]<br>0x0B: [7:0]<br>0x0A: [7:5] | 0x03FF |

## I2C Register 0x0C (continued), 0x0D, 0x0E

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x0C, 0x0D | dacn0_cur | Tuning of the current source bias current (1V2 PA domain). Tuning may be necessary due to process variations. This register uses binary format. | 0x0D: [1:0]<br>0x0C: [7:4] | 0x30 |
| 0x0D | dacn1_cur | Tuning of the current source bias current (1V2 SH and SUM domain). Tuning may be necessary due to process variations.This register uses binary format. | [7:2] | 0x30 |
| 0x0E | dacp1_cur | Tuning of the current sink bias current (2V5 PA domain). Tuning may be necessary due to process variations. This register uses binary format. | [5:0] | 0x0F |

## I2C Register 0x0E (continued), 0x0F

| I2C addr | Control Name | Description | Bits | Default after reset |
|---|---|---|---|---|
| 0x0E | bgr_sel | Select the source for the internal DAC reference.<br>0b01 Use BGR for the DAC reference<br>0b11 User voltage provided to the ext_ref_dac pin.<br>0b10 and 0b00 Do not use. This will disconnect both BGR and ext_ref_dac pin. | [7:6] | 0b11 |
| 0x0F | pa1v2_cur | 1V2 PA domain current reference selection.<br>0b0 External current reference. In this case the user must provide 1mA reference | [0] | 0b1 |

| | | | | |
|---|---|---|---|---|
| | | current to the corresponding pin.<br>0b1 Internal current reference (default) | | |
| | sh1v2_cur | 1V2 SH and SUM domain current reference selection.<br>0b0 External current reference. In this case the user must provide 1mA reference current to the corresponding pin.<br>0b1 Internal current reference (default) | [1] | 0b1 |
| | pa2v5_cur | 2V5 PA domain current reference selection.<br>0b0 External current reference. In this case the user must provide 1mA reference current to the corresponding pin.<br>0b1 Internal current reference (default) | [2] | 0b1 |
| | unused | N/C. Does not affect chip operation. | [7:3] | 0x00 |

# Example control register configurations

After power up and I2C reset the ALFE2 I2C registers are set to their default values. Some register values must be changed in order to operate the chip as intended.
Two example configurations are given, for 25 Ohm and 50 Ohm input impedance. These example configurations are labeled as “25 Ohm mode” and “50 Ohm mode”.

| Control name | Default value (reset) | 50 Ohm mode | 25 Ohm mode |
|---|---|---|---|
| ch_pwr | 0x0 | 0x0 | 0x0 |
| pa_fb_r0 | 0b01 | 0b01 | 0b11 |
| pa_fb_c0 | 0b01 | 0b01 | 0b11 |
| pa_out_offset | 0x1 | 0x1 | 0xF |
| pa_fb_c1 | 0b01 | 0b01 | 0b11 |
| imped_coarse | 0b11 | 0b11 | 0b00 |
| imped_fine | 0x0000FF | 0x0007FF | 0x000FFF |
| pa_fb_r1 | 0b1 | 0b1 | 0b0 |
| pa_output_dc | 0x1F | 0x1F | 0x1F |
| sh_pt | 0x01F | 0x0F | 0x07 |
| en_sh_lg_gain_boost | 0b0 | 0b0 | 0b0 |
| sh_output_dc | 0x03FF | 0x03FF | 0x03FF |
| sh_sum_pwr | 0b0 | 0b0 | 0b0 |
| sh_sum_gain_ch0 | 0b001 | 0b001 | 0b001 |
| sh_sum_gain_ch1 | 0b001 | 0b001 | 0b001 |
| sh_sum_gain_ch2 | 0b001 | 0b001 | 0b001 |
| sh_sum_gain_ch3 | 0b001 | 0b001 | 0b001 |
| sh_sum_output | 0x03FF | 0x03FF | 0x03FF |
| dacn0_cur | 0x30 | 0x30 | 0x30 |
| dacn1_cur | 0x30 | 0x30 | 0x30 |
| dacp1_cur | 0x0F | 0x0F | 0x0F |

| | | | |
|---|---|---|---|
| bgr_sel | 0b11 | 0b01 | 0b01 |
| pa1v2_cur | 0b1 | 0b1 | 0b1 |
| sh1v2_cur | 0b1 | 0b1 | 0b1 |
| pa2v5_cur | 0b1 | 0b1 | 0b1 |