LAUROC1 working document

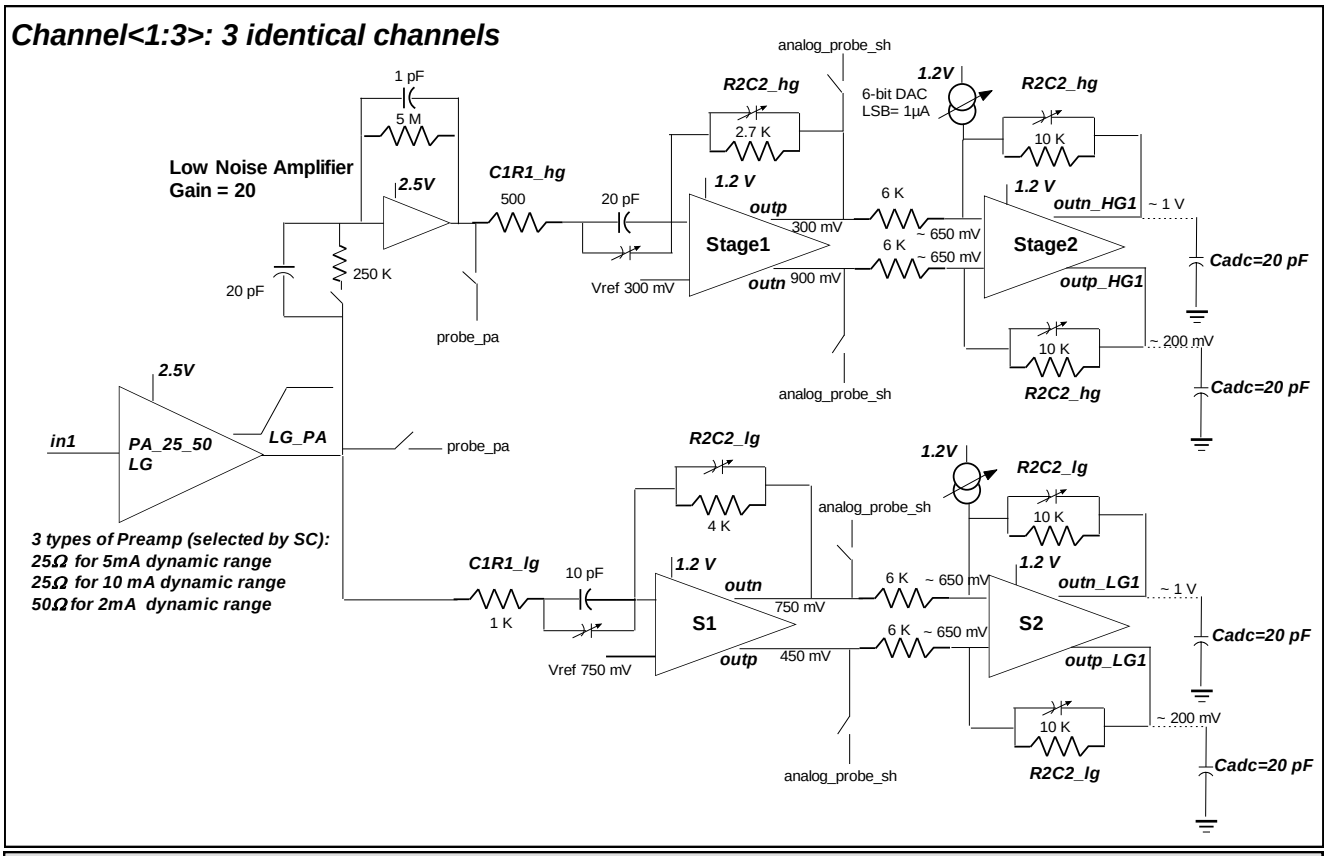
Last update: 6 May 2019

General description

Lauroc1 integrates 4 FE channels built around a preamp with a tune able input impedance (25 or 50 Ohm) using configuration parameters. The general architecture is shown in Figure 1.

Three channels (channel <1:3>) are identical. The preamp is followed by a High Gain and a Low Gain differential CRRC2 shaper (shaper amplifier designed by Mietek Dabrowski, BNL).

The fourth channel (channel<4>) integrates a different preamp from the one used for channel<1:3>. This preamp is the one used in the previous version of Lauroc. It has a HG output and a LG output which are followed respectively by a High Gain differential shaper and a Low Gain differential shaper. This channel also integrates a discriminator that is used to avoid the saturation of the High Gain preamp.



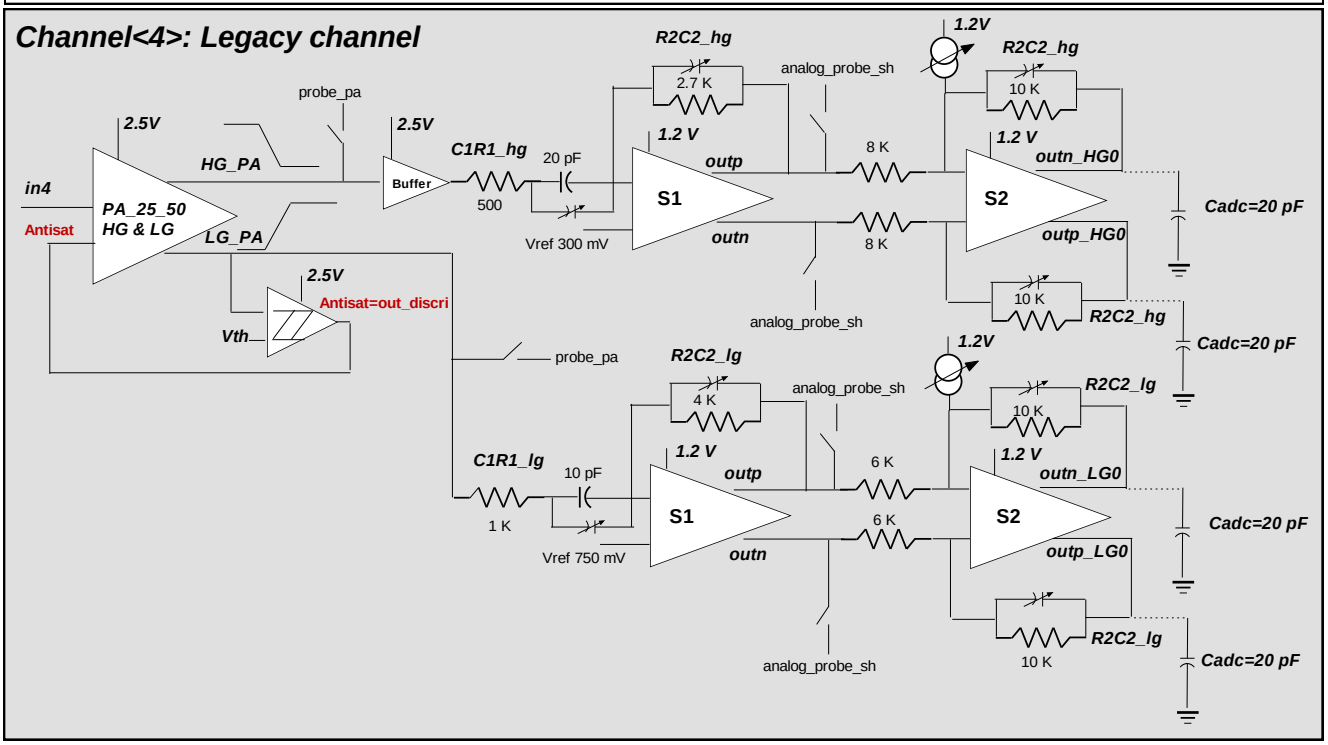


Figure 1: LAUROC1 general architecture

▪ The input preamplifier exhibits an input impedance Zin that is tune able using SC parameters (C2<8:0>). This line termination preamp is made around a resistor (R0) in series with a Super Common Gate amplifier (SCG) used in the feedback of a low noise voltage amplifier. The input impedance is then given by the following formula :

$$Z_{in}\,PA = \frac{R_0 + Zin(SCG)}{1 + |G|}$$

The R0 noise is given by: $4kTR0/(1+|G|)^2$

The two main advantages of this architecture are that the voltage gain is made using capacitors which are noiseless and the equivalent noise of R0 is divided by the square of the gain, while the input impedance is only R0 divided by the gain. The preamp input impedance can be precisely tuned to match the cable by adjusting the capacitor ratio. The feedback also ensures that the input impedance does not vary with the signal amplitude.

The preamp used for channel <4> is slightly different from the one used for channel<1:3> as it has 2 outputs: one output which corresponds to the HG preamp output and one output that corresponds to the LG output.

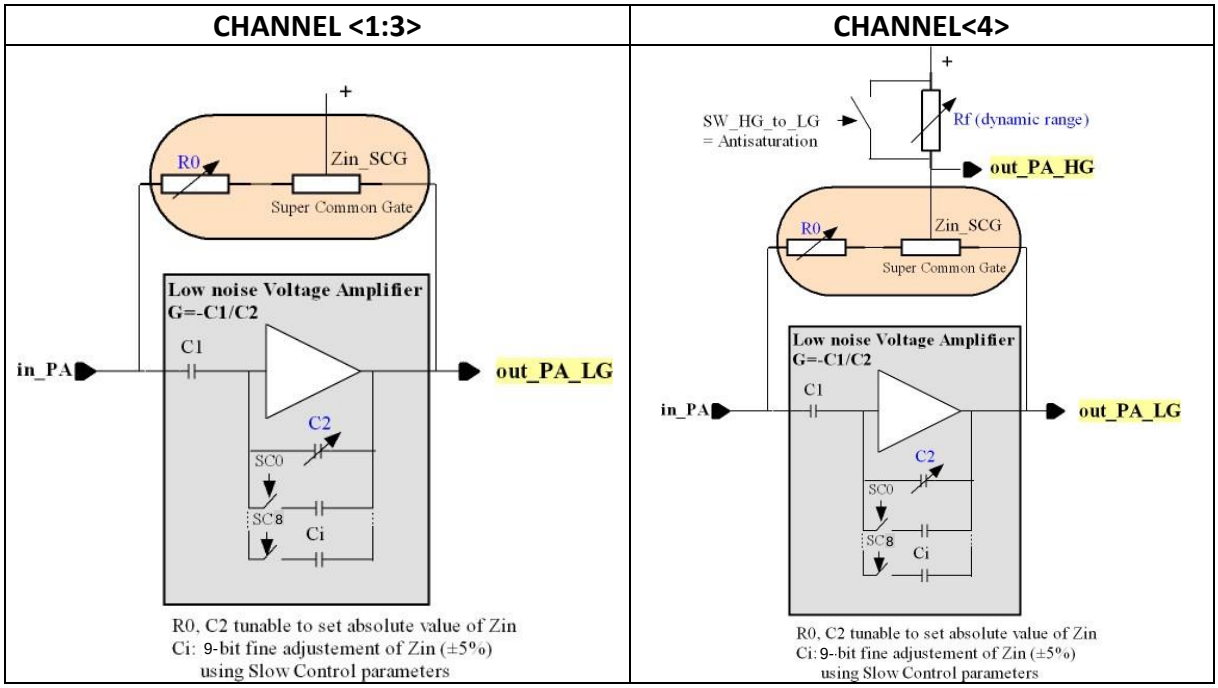


Figure 2: LAUROC1 preamp, LEFT = Channel <1:3> preamp, – RIGHT = channel<4> preamp

For channel <1:3>

	SW_R0_10m (SC@address1)	SW_R0_5m (SC@address2)	R0 equivalent	Gain (formula)	C2 (formula)	C2 (decimal) (SC bits: 9b)
50Ω 2mA	0	0	500 Ω	9	3,3pF	107
25Ω 5mA	0	1	400//500 = 222 Ω	7.9	3,80pF	122
25Ω 10mA	1	0	150//500= 115 Ω	3,6	8,30pF	266

For 25Ω 5mA configuration and Idet=5 mA, Vin=25*5mA= 125 mV which give Vout_pa = 7.8 * 125 mV = 975 mV
For 25Ω 10mA configuration Idet =10 mA, Vin=25*10 mA= 250 mV that give Vout_pa= 3.6* 250 mV= 900 mV

Other preamplifier SC parameters for channel <1:3>

ON_PA_1V2 (SC@address 5): when set to 1 all the preamps are ON. Preamps can then be set OFF using local SC parameters.

sw_ibi (SC@address 3): ibi is the bias current of the SCG. When set to 1, the bias input current of the input transistor is 200 µA (otherwise it is 20 µA). This parameter must be set to 1 (200 µA).

sw_ibo (SC@address 0): The minimum current that flows in the input transistor is 3.5 mA. When set to 1, the current that flows in the input transistor is increased by 2.5 mA.

ON_Rbleed (SC@address 4): For ch<1:3>. 6 mA additional current in the input preamp.

For channel 4:

	SW_R0_10m (SC@address1)	SW_R0_5m (SC@address2)	R0 equivalent	C2	
50Ω	0	X	500 Ω		
50Ω	0	X	500 Ω		
25Ω	1	X	150//500= 115 Ω		
25Ω	1	X	150//500= 115 Ω		

Sw_ibi,sw_ibo

- The preamp output of channel <1:3> is split into 2 path: one for the LG measurement and one for the HG measurement. The HG path is made of an amplifier with a gain of 20 followed by a HG CRRC2 shaper. LG path is made by a CRRC2 shaper.

- Both CRRC2 shapers with a variable τ : 4 bits (LSB= 1.25 ns) are CR tuning independent of RC tuning

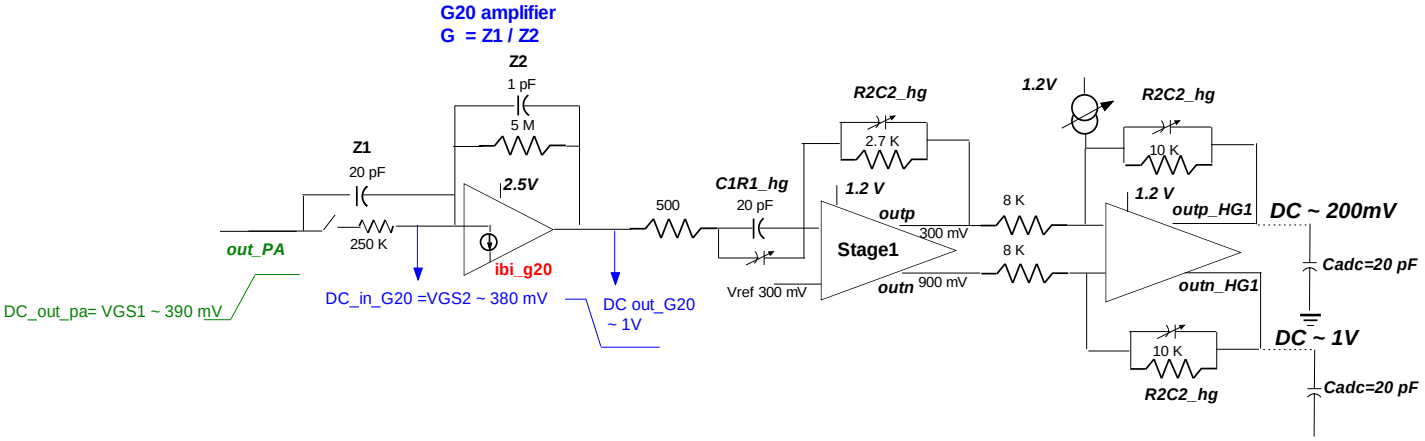


Figure 3: High Gain path: G20 amplifier + CRRC2

HG C1R1			
Code	C (pF)	R (Ohms)	Tau (ns)
0	20	500	10
1	22,5	500	11,25
2	25	500	12,5
3	27,5	500	13,75
4	30	500	15
5	32,5	500	16,25
6	35	500	17,5
7	37,5	500	18,75

HG R1C1			
Code	C (pF)	R (Ohms)	Tau (ns)
0	0	2700	0
1	0,462	2700	1,247
2	0,924	2700	2,495
3	1,386	2700	3,742
4	1,848	2700	4,99
5	2,31	2700	6,237
6	2,772	2700	7,484
7	3,234	2700	8,732
8	3,696	2700	9,979
9	4,158	2700	11,227
10	4,62	2700	12,474
11	5,082	2700	13,721
12	5,544	2700	14,969
13	6,006	2700	16,216
14	6,468	2700	17,464
15	6,93	2700	18,711

HG R2C2			
Code	C (pF)	R (Ohms)	Tau (ns)
0	0	10000	0
1	0,125	10000	1,25
2	0,25	10000	2,5
3	0,375	10000	3,75
4	0,5	10000	5
5	0,625	10000	6,25
6	0,75	10000	7,5
7	0,875	10000	8,75
8	1	10000	10
9	1,125	10000	11,25
10	1,25	10000	12,5
11	1,375	10000	13,75
12	1,5	10000	15
13	1,625	10000	16,25
14	1,75	10000	17,5
15	1,875	10000	18,75

Cmd_AC_DC link

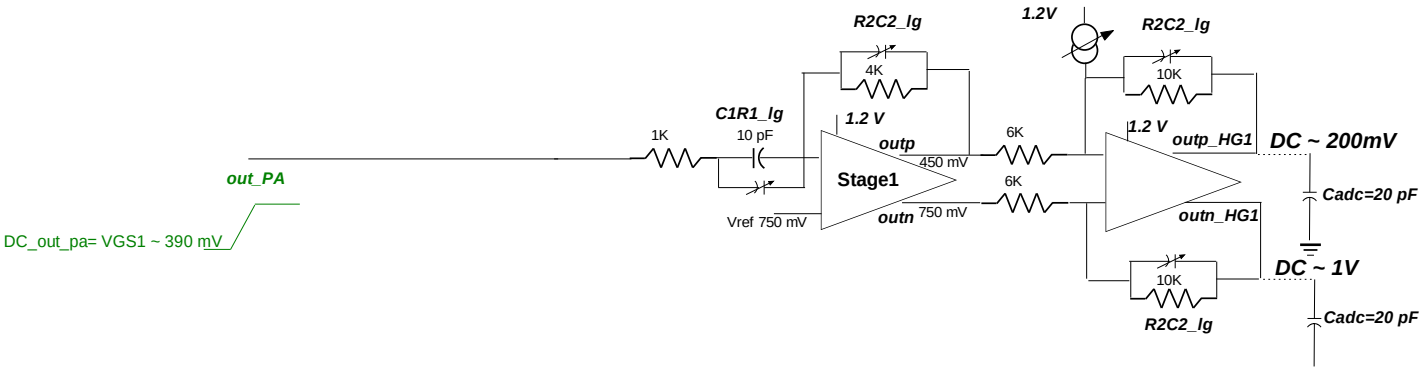


Figure 4: Low Gain path: only CRRC2

LG C1R1			
Code	C (pF)	R (Ohms)	Tau (ns)
0	10	1000	10
1	11,25	1000	11,25
2	12,5	1000	12,5
3	13,75	1000	13,75
4	15	1000	15
5	16,25	1000	16,25
6	17,5	1000	17,5
7	18,75	1000	18,75

LG R1C1			
Code	C (pF)	R (Ohms)	Tau (ns)
0	0	4000	0
1	0,462	4000	1,848
2	0,924	4000	3,696
3	1,386	4000	5,544
4	1,848	4000	7,392
5	2,31	4000	9,24
6	2,772	4000	11,088
7	3,234	4000	12,936
8	3,696	4000	14,784
9	4,158	4000	16,632
10	4,62	4000	18,48
11	5,082	4000	20,328
12	5,544	4000	22,176
13	6,006	4000	24,024
14	6,468	4000	25,872
15	6,93	4000	27,72

LG R2C2			
Code	C (pF)	R (Ohms)	Tau (ns)
0	0	10000	0
1	0,125	10000	1,25
2	0,25	10000	2,5
3	0,375	10000	3,75
4	0,5	10000	5
5	0,625	10000	6,25
6	0,75	10000	7,5
7	0,875	10000	8,75
8	1	10000	10
9	1,125	10000	11,25
10	1,25	10000	12,5
11	1,375	10000	13,75
12	1,5	10000	15
13	1,625	10000	16,25
14	1,75	10000	17,5
15	1,875	10000	18,75

The chip size is 2.8 mm x 2.5 mm. It is packaged in a LQFP 100 14*14 package.

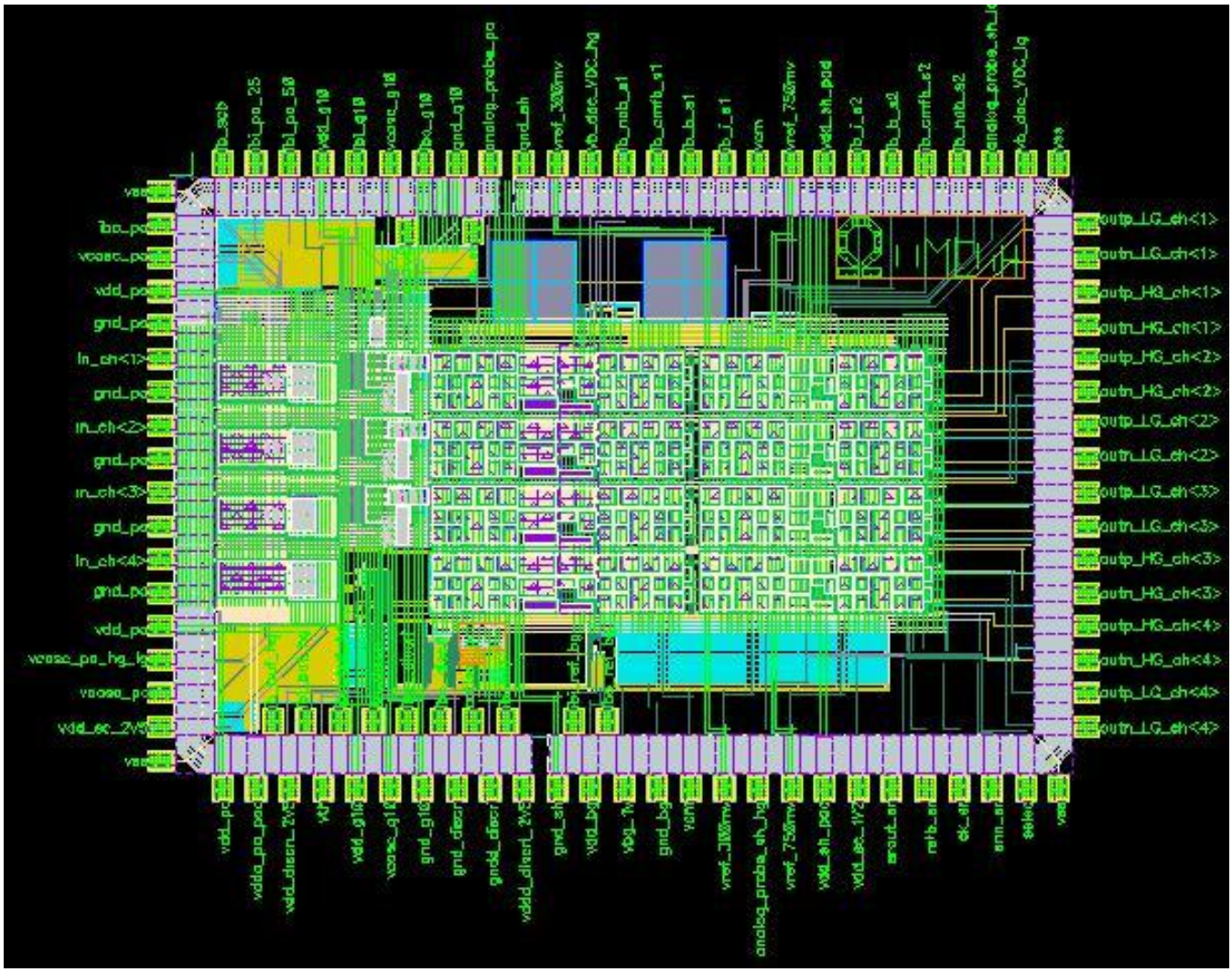


Figure 3: Layout of LAUROC1 (size 2.8 mm x 2.5 mm)

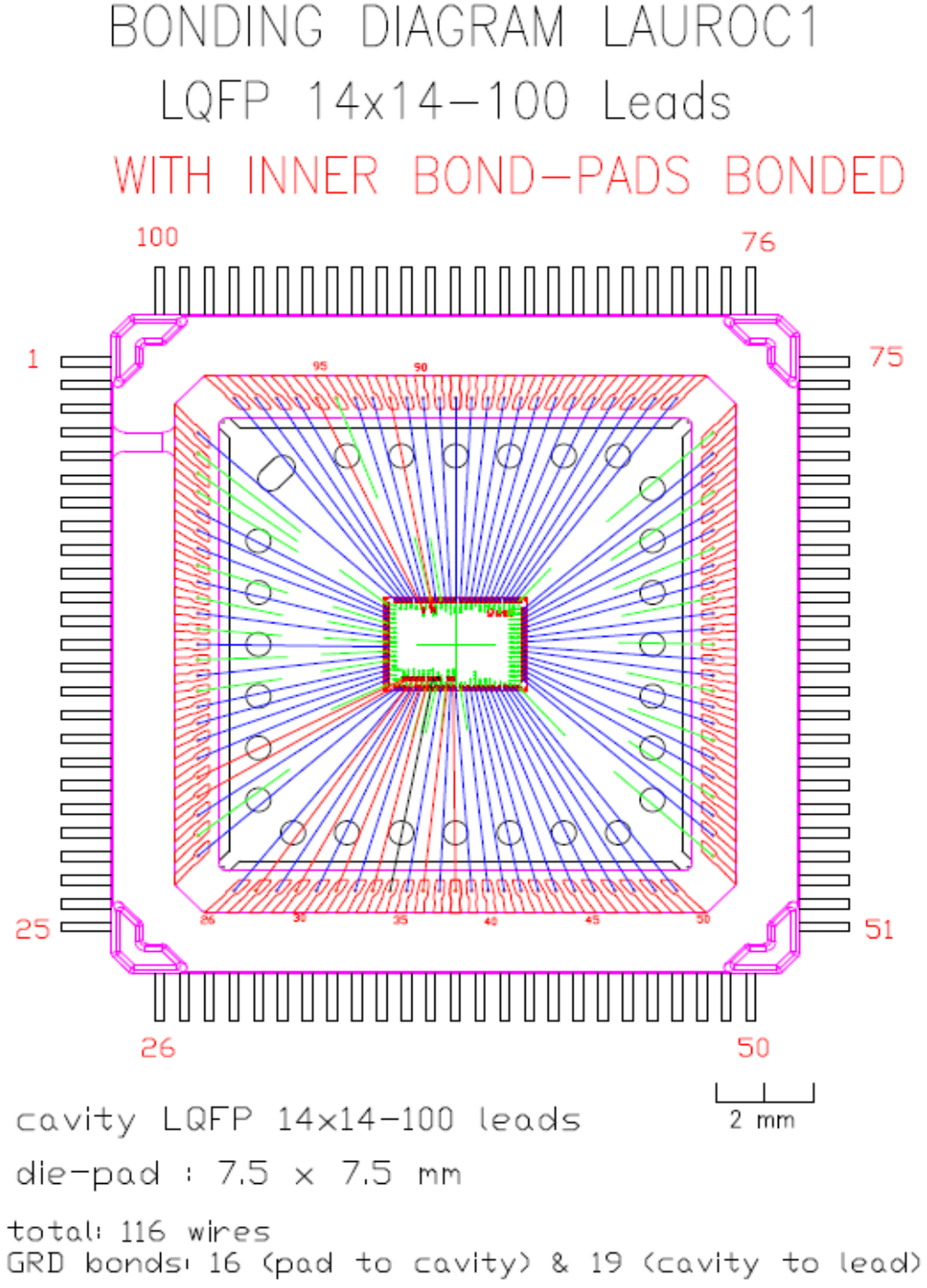


Figure 4: Bonding diagram of Lauroc1 in LQFP100 14x14

Pin list

Ground pins are in green

Power pins in red

Input pins in blue

Output pins in black

Input/output pins (Bias voltages and reference voltages) in grey

Pin_number	Pin_name	Pin_type	Comment
1	ib_scb	ANALOG	Bias 2V5
2	GND	GROUND	
3	GND	GROUND	
4	GND	GROUND	
5	ibo_pa	ANALOG	Bias 2V5
6	vcasc_pa	ANALOG	Bias 2V5
7	vdd_pa_2V5	POWER	
8	GND	GROUND	
9	in_ch<1>	INPUT	
10	GND	GROUND	
11	in_ch<2>	INPUT	
12	GND	GROUND	
13	in_ch<3>	INPUT	
14	GND	GROUND	
15	in_ch<4>	INPUT	
16	GND	GROUND	
17	vdd_pa_2V5	POWER	
18	vcasc_pa_hg_lg	ANALOG	Bias 2V5
19	vcasc_pa	ANALOG	Bias 2V5
20	vdd_sc_2V5	POWER	
21	ib_buf_hg *	ANALOG	Bias 2V5
22	ibi_buf_hg *	ANALOG	Bias 2V5
23	vdd_pa_2V5	POWER	
24	GND	GROUND	
25	vdda_pa_pad_2V5	POWER	
26	vdd_discri_2V5	POWER	
27	ibo_buf_hg *	ANALOG	Bias 2V5
28	vth	ANALOG	
29	ibi_discri *	ANALOG	Bias 2V5
30	vdd_g20_2V5	POWER	
31	ibm_discri *	ANALOG	Bias 2V5
32	vcasc_g20	ANALOG	Bias 2V5
33	ibo_discri *	ANALOG	Bias 2V5
34	antisat_pad	OUTPUT	
35	vddd_discri_2V5	POWER	
36	ibi_ref_bg *	ANALOG	Bias 1V2

37	vdd_bg_1V2	POWER	
38	ibo_ref_bg *	ANALOG	Bias 1V2
39	vbg_1V	ANALOG	
40	vcm	ANALOG	Bias 1V2
41	vref_300mV	ANALOG	Bias 1V2
42	analog_probe_sh_hg	OUTPUT	
43	vref_750 mV	ANALOG	Bias 1V2
44	vdd_sh_pad_1V2	POWER	
45	vdd_sc_1V2	POWER	
46	srout_sr	OUTPUT	
47	rstb_sr	INPUT	
48	ck_sr	INPUT	
49	srin_sr	INPUT	
50	select	INPUT	
51	GND	GROUND	
52	outn_LG_ch<4>	OUTPUT	
53	outp_LG_ch<4>	OUTPUT	
54	GND	GROUND	
55	outn_HG_ch<4>	OUTPUT	
56	outp_HG_ch<4>	OUTPUT	
57	GND	GROUND	
58	outn_HG_ch<3>	OUTPUT	
59	outp_HG_ch<3>	OUTPUT	
60	GND	GROUND	
61	outn_LG_ch<3>	OUTPUT	
62	outp_LG_ch<3>	OUTPUT	
63	GND	GROUND	
64	outn_LG_ch<2>	OUTPUT	
65	outp_LG_ch<2>	OUTPUT	
66	GND	GROUND	
67	outn_HG_ch<2>	OUTPUT	
68	outp_HG_ch<2>	OUTPUT	
69	GND	GROUND	
70	outn_HG_ch<1>	OUTPUT	
71	outp_HG_ch<1>	OUTPUT	
72	GND	GROUND	
73	outn_LG_ch<1>	OUTPUT	
74	outp_LG_ch<1>	OUTPUT	
75	GND	GROUND	
76	vb_dac_VDC_lg	ANALOG	Bias 1V2
77	analog_probe_sh_lg	OUTPUT	
78	ib_nab_s2	ANALOG	Bias 1V2
79	ib_cmfb_s2	ANALOG	Bias 1V2
80	ib_b_s2	ANALOG	Bias 1V2
81	ib_i_s2	ANALOG	Bias 1V2
82	vdd_sh_pad_1V2	POWER	

83	vref_750mv	ANALOG	Bias 1V2
84	vcm	ANALOG	Bias 1V2
85	ib_i_s1	ANALOG	Bias 1V2
86	ib_b_s1	ANALOG	Bias 1V2
87	ib_cmfb_s1	ANALOG	Bias 1V2
88	ib_nab_s1	ANALOG	Bias 1V2
89	vb_dac_VDC_hg	ANALOG	Bias 1V2
90	vref_300mV	ANALOG	Bias 1V2
91	analog_probe_pa	OUTPUT	
92	ib_sc *	ANALOG	Bias 2V5
93	ibo_g20	ANALOG	Bias 2V5
94	vcasc_g20	ANALOG	Bias 2V5
95	GND	GROUND	
96	ib_fol2 *	ANALOG	Bias 2V5
97	ibi_g20	ANALOG	Bias 2V5
98	vdd_g20_2V5	POWER	
99	ibi_pa_50	ANALOG	Bias 2V5
100	ibi_pa_25	ANALOG	Bias 2V5

*= inner pad ring

Table 1: Pin list

Bias, reference, cascode values

Pin number	Bias name	Comment/value
1	**ib_scb**	**1.8V, 1mA (preamp, preamp, all channels)**
5	**ibo_pa**	**1.4 V, 4.7 mA or 7 mA depending on sw_ibo, all channels**
6	**vcasc_pa**	**900 mV (channel<1:3>**
18	**vcasc_pa_hg_lg**	**600 mV (preamp HG-LG, channel <4>)**
19	**vcasc_pa**	**900 mV (preamp channel<1:3>)**
21	*ib_buf_hg (*)*	*NC - 770 mV, 50 µA (buffer channel<4>)*
22	*ibi_buf_hg (*)*	*NC - 1.9 V, 100 µA (buffer ch<4>)*
27	*ibo_buf_hg (*)*	*NC - 1.5 V, 400 µA (buffer ch<4>)*
29	*ibi_discri (*)*	*NC - 665 mV, 200µA (discri ch<4>)*
31	*ibm_discri (*)*	*NC - 1.7 V, 50 µA (discri ch<4>)*
32	**vcasc_g20**	**900 mV (ampli with a gain of 20)**
33	*ibo_discri (*)*	*NC - 1.9 V, 5 µA (discri ch<4>)*
	ib_fol1 (*)	*NC - 623 mV, 20 µA (discri follower)*
36	*ibi_ref_bg (*)*	*NC - 150 mV, 20 µA (bandgap)*
38	*ibo_ref_bg (*)*	*NC - 1 V, 100 µA (bandgap)*
39	**vbg_1V**	**920 mV (internal bandgap)**
40	**vcm**	**600 mV (shaper)**
41	**vref_300mV**	**300 mV (shaper)**
43	**vref_750 mV**	**750 mV (shaper)**
76	**vb_dac_VDC_lg**	**692 mV, 140 µA (Vref shaper stage 2)**
78	**ib_nab_s2**	**330 mV, 100 µA (shaper stage2)**
79	**ib_cmfb_s2**	**494 mV, 1 mA (shaper stage2)**
80	**ib_b_s2**	**777 mV, 1 mA (shaper stage2)**
81	**ib_i_s2**	**775 mV, 2.6 mA (shaper stage 2)**
83	**vref_750mv**	**750 mV (shaper)**
84	**vcm**	**600 mV (shaper)**
85	**ib_i_s1**	**775 mV, 2.5 mA (shaper stage1)**
86	**ib_b_s1**	**777 mV, 1 mA (shaper stage1)**
87	**ib_cmfb_s1**	**494 mV, 1 mA (shaper stage1)**
88	**ib_nab_s1**	**332 µA, 100µA (shaper stage1)**
89	**vb_dac_VDC_hg**	**692 mV, 140 µA (shaper stage1)**
90	**vref_300mV**	**300 mV (shaper)**
92	*ib_sc (*)*	*NC - 1.75V, 20 µA (bias for SC reg. , translation 2V5 to 1V2)*
93	**ibo_g20**	**1.6V, 2.7 mA or 5.4 mA (depending on sw_ibo_g20)**
94	**vcasc_g20**	**900 mV (amplifier with G=20, channel <1:3>**
96	*ib_fol2 (*)*	*NC - 623 mV, 20 µA (discri follower)*
97	**ibi_g20**	**380 mV (amplifier with G=20, channel <1:3>**
99	**ibi_pa_50**	**650 mV, 20 µA (preamp, all channels)**
100	**ibi_pa_25**	**730 mV, 200µA (preamp, preamp, all channels)**

Table 2: Bias values

Slow control (SC) register

It is based on Flip-Flops. There are n=*138* flip flops (first bit is B_0 = sw_ibo and last is B_{137} =DAC_VDC_lg<0>. B_{137} is the first bit seen on the scope on srin_sr (pin 49).

Slow Control bits are stored in flip flops on leading edge of the clock and are shifted at each clock cycle as shown in Figure 5.

The SC bits are "Write only". The only way to read them is to send twice the SC bits and to compare srout_sr bits to the srin_sr bits.

The Slow Control register is selected when "SELECT" = 1 (pin 50 of the ASIC). When SELECT= 0, the Probe register is selected.

Inputs: **srin_sr (pin 49), rstb_sr (Asynchronous) (pin 47), ck_sr (Frequency= 1 MHz)(pin 48)**

Outputs: **srout_sr (pin 46)**

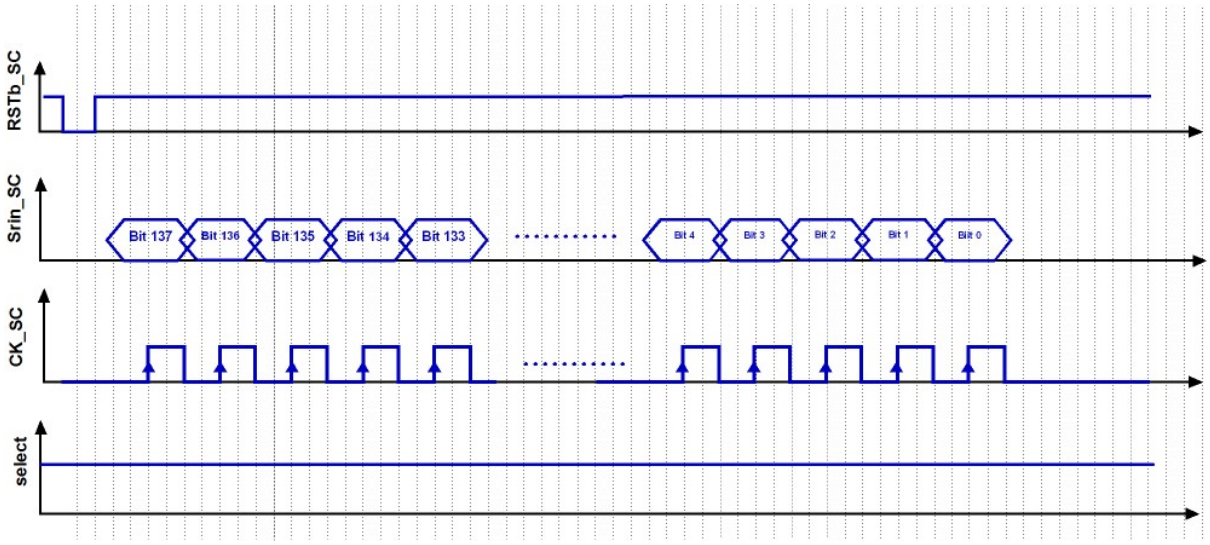


Figure 5: Shift registers for Slow Control (SC) parameters. B137 is the first bit seen on the scope on srin_sr

Between srout_sr and the output of the last slow control register's flip flop, there is another flip flop clocked on !clk so an additional falling edge is needed to send the data out on srout_sr.

!! B_{137} is the first bit of the srin_sr frame seen on the scope.

SC reg.			Add	Value	Description
srin_sc	**Bias_pa**	sw_ibo	B_0	1	For all channels. ibo_pa=5 mA when sw_ibo ON, 2.5 mA when sw_ibo OFF

		sw_R025_10mA	1	0	For ch<1:3>. 25 Ohms config only. When "1" R0= 150//500= 115 Ohms=> dyn range up to 10 mA
		sw_R025_5mA	2	1	For ch<1:3>. 25 Ohms config only. When"1", R0= 400//500= 220 Ohms => dyn range up to 5 mA
		sw_ibi	3	1	For all channels. Bias ibi_pa 200 µA when ON, 20 µA when OFF
		ON_Rbleed_1V2	4	1	For ch<1:3>. 6 mA additional current in the input preamp. 1V2 translated to 2V5 internally
		ON_pa_1V2	5	1	For all channels. ON pa. 1V2 translated to 2.5V internally
	Bias_ampliG20	dac_ibi_g20<5:0>	6	110000 =48	For ch<1:3>. Bias ampli G=20. ibi_pa_g20. DEF value=120 nA (ibias tuneable up to 600 nA)
		sw_ibo_g20	12	1	For ch<1:3>. ibo_g20=5 mA when sw_ibo ON, 2.5 mA when sw_ibo OFF
		ON_g20	13	1	For ch<1:3>
	channel<1> (srin_sc_pa)				
	input_pa_nvt	ON_ch<1>	14	1 (ON)	
		C2<**0**:8>	15	:000011100 = 112	DEF value for PA25 Ohms 5 mA, LSB= 31,25 fF, MSB c2<8>=8 pF => 3.5 pF

	channel<2> (srin_sc_pa)				
	input_pa_nvt	ON_ch<2>	24	1 (ON)	
		C2<0:8>	25	:000011100 =112	DEF value for pa25 Ohms 5 mA, LSB= 31.25 fF, MSB c2<8>=8 pF => c2= 3,5 pF
	channel<3> (srin_sc_pa)				
	input_pa_nvt	ON_ch<3>	34	1 (ON)	
		C2<0:8>	35	:000011100 =112	DEF value for pa25 Ohms 5 mA, LSB= 31,25 fF, MSB c2<8>=8 pF => c2=3,5 pF
	channel<4> HG/LG (srin_sc_pa)	ON_ch<4>	44	1 (ON)	
		Rf<0:3>	45	:0100	
		C2<0:8>	49	:000100001	C2=8.250 pF
	bias_buffer	ON	58	1 (ON)	
	bias_discri	ON	59	0 (OFF)	
		EN_discri	60	0	When "1" out_pa_LG of ch<4> connected to the discri
		EN_antisat_pad	61	0	When "1", out_dscri of ch<4> is sent to the PAD
	bias_damp_sdc_stage1	ON_HG_s1	62	1(ON)	ON/OFF of HG shaper stage 1
		ON_LG_s1	63	1(ON)	ON/OFF of LG shaper stage 1
	Channel<1>	dac_VDC_hg<5:0>	64	:010000 =16	tuning of DC ref voltage of inn stage 2 (~600mV)
	Channel<2>	dac_VDC_hg<5:0>	70	:010000	tuning of DC ref voltage of inn stage 2 (~600mV)
	Channel<3>	dac_VDC_hg<5:0>	76	:010000	tuning of DC ref voltage of inn stage 2 (~600mV)
	Channel<4>	dac_VDC_hg<5:0>	82	:001000	Tuning of DC ref voltage of inn stage 2 (~600mV)

	Bandgap_and_Ampli	ON_ref_bg	88	1	ON/OFF bandgap reference
	Bias_SW_CRRC2	sw_DC_g20	89	0	For ch<1:3> only. When "1" DC connection between out_pa and ampli_g20. When "0", AC connection
		RC_hg_s1<3:0>	90	:1010 =10 and so 12.5 ns	for all channels. Fixed R=2.7K, C<0>=462,5 fF, C<1>=925 fF, C<2>=1,85 pF, C<3>=3,7 pF
		CR_hg_s1<2:0>	94	:010 =2 and so 12.5 ns	Fixed R=500 and fixed C= 20 pF C<0>=2.5pF, C<1>=5 pF, C<2>=10 pF
		RC_hg_s2<3:0>	97	:1010 =10 and so 12.5 ns	for all channels. Fixed R=10 K, C<0>=125 fF, C<1>=250 fF, C<2>=500 fF, C<3>=1 pF
		RC_lg_s1<3:0>	101	:1001 =9 and so 16.6 ns	for all channels. Fixed R = 4 K, C<0>=462,5 fF, C<1>=925 fF, C<2>=1,85 pF, C<3>=3,7 pF
		CR_lg_s1<2:0>	105	:100 =4 and so 15 ns	Fixed R=1K and fixed C= 10 pF C<0>=1,25pF, C<1>=2,5 pF, C<2>=5 pF
		RC_lg_s2<3:0>	108	:1001 =9 and so 16.25 ns	for all channels. Fixed R=10 K, C<0>=125 fF, C<1>=250 fF, C<2>=500 fF, C<3>=1 pF
	Bias_damp_sdc_stage 2	ON_HG_s2	112	1	ON/OFF of HG shaper stage 2
		ON_LG_s2	113	1	ON/OFF of LG shaper stage 2

	Channel<1>	dac_VDC_lg<5:0>	114	:011000 =24	Tuning of DC ref voltage of inp stage 2 (~600 mV)
	Channel<2>	dac_VDC_lg<5:0>	120	:011000	Tuning of DC ref voltage of inp stage 2 (~600 mV)
	Channel<3>	dac_VDC_lg<5:0>	126	:011000	Tuning of DC ref voltage of inp stage 2 (~600 mV)
	Channel<4>	dac_VDC_lg<5:0>	B_{132} to B_{137}	:011100 =28	Tuning of DC ref voltage of inn stage 2 (~600 mV)
	Total of SC bits		138		

Table 3: Configuration (SC) parameters

Probe register

There are 3 analog probes: analog_probe _pa (Pin 91), analog_probe_sh_lg (pin 77)and analog_probe_sh_hg (pin 42). They are used only for debug.

The probe register is based on Flip-Flops. There are *25* flip flops (first bit is B_0 = en_probe_pa<1> and last is B_{24} = en_probe_outn_lg_s1<4>. Probe bits are stored in flip flops on leading edge of the clock and are shifted at each clock cycle as shown in Table 4

The probe bits are "Write only". The only way to read them is to send twice the probe bits and to compare srout_probe bits to the srin_probe bits.

PADs for probe registers:
SELECT signal on PAD (50) to choose between SC register and Probe register. **The probe register is selected when "SELECT" = 0 (pin 50 of the ASIC). When SELECT= 1, the SC register is selected.**

Inputs: srin_sr, rstb_sr (Asynchronous), ck_sr (Frequency 1 MHz)
Outputs: srout_sr,

PROBES: all OFF (0)		**Address**
channel<1>	en_probe_pa<1>	0
	en_probe_g20<1>	1
channel<2>	en_probe_pa<2>	2
	en_probe_g20<2>	3
channel<3>	en_probe_pa<3>	4
	en_probe_g20<3>	5
channel<4>	en_probe_pa_hg	6
	en_probe_pa_lg	7
	en_probe_buf_hg	8
channel<1>	en_probe_outn_hg_s1<1>	9
	en_probe_outp_hg_s1<1>	10
channel<2>	en_probe_outn_hg_s1<2>	11
	en_probe_outp_hg_s1<2>	12
channel<3>	en_probe_outn_hg_s1<3>	13
	en_probe_outp_hg_s1<3>	14
channel<4>	en_probe_outn_hg_s1<4>	15
	en_probe_outp_hg_s1<4>	16
channel<1>	en_probe_outp_lg_s1<1>	17
	en_probe_outn_lg_s1<1>	18
channel<2>	en_probe_outp_lg_s1<2>	19
	en_probe_outn_lg_s1<2>	20
channel<3>	en_probe_outp_lg_s1<3>	21

	en_probe_outn_lg_s1<3>	22
channel<4>	en_probe_outp_lg_s1<4>	23
	en_probe_outn_lg_s1<4>	24

Table 4: Probe register

Input/outputs and cells description

Preamp for channel <1:3>

Power: 2.5 V= vdd_pa

Common SC parameters:

"1" logic level corresponds to 1.2V even for cells powered with 2.5V (1.2V to 2.5V translation made internally)

sw_ibo (SC0): The minimum current that flows in the input transistor is 3.5 mA. When set to 1, the current that flows in the input transistor is increased by 2.5 mA.

sw_R025_5mA (SC1) and SC_R025_10 mA (SC2): Tuning of the dynamic range for the 25 Ohms configuration only: depending on R0 choice, the dynamic range for the 25 Ohm PA is 5 mA or 10mA.

When "SW_R025_5 mA" (SC@address 2) is equal to 1 and SW_R025_10mA is set to 0, R0 is equal to 400//500= 220 Ohms. The R0 choice also impacts the dynamic range. The input impedance is indeed given by : Zin = R0/(G+1) . If R0=220 Ohms => G= R0/Zin - 1= 220/25 -1 = 7.8 and so C2 = 30 pF/7.8 =3.8 pF which corresponds to decimal code = 3.8 pF/0.0316 pF= 120. For Idet=5 mA, Vin=25*5mA= 125 mV which give Vout_pa = 7.8 * 125 mV = 975 mV

When "SW_R025_5 mA" (SC@address 2) is set to 0 and SW_R025_10mA is set to 1, R0 is equal to 150//500= 115 Ohms. The gain G is then equal to 3.6 and C2 = 8.3 pF which corresponds to decimal code = 8.3/0.0316= 263. For Idet =10 mA, Vin=25*10 mA= 250 mV that give Vout_pa= 3.6* 250 mV= 900 mV

sw_ibi: ibi is the bias current of the SCG. When set to 1, the bias input current of the input transistor is 200 µA (otherwise it is 20 µA). This parameter must be set to 1 (200 µA).

ON_PA_1V2: when set to 1 all the preamps are ON. Preamps can then be set OFF using local SC parameters.

Local SC for the preamp (SC per channel):

ON_ch<i> (SC 14, 24, 34): When set to 1, channel is ON

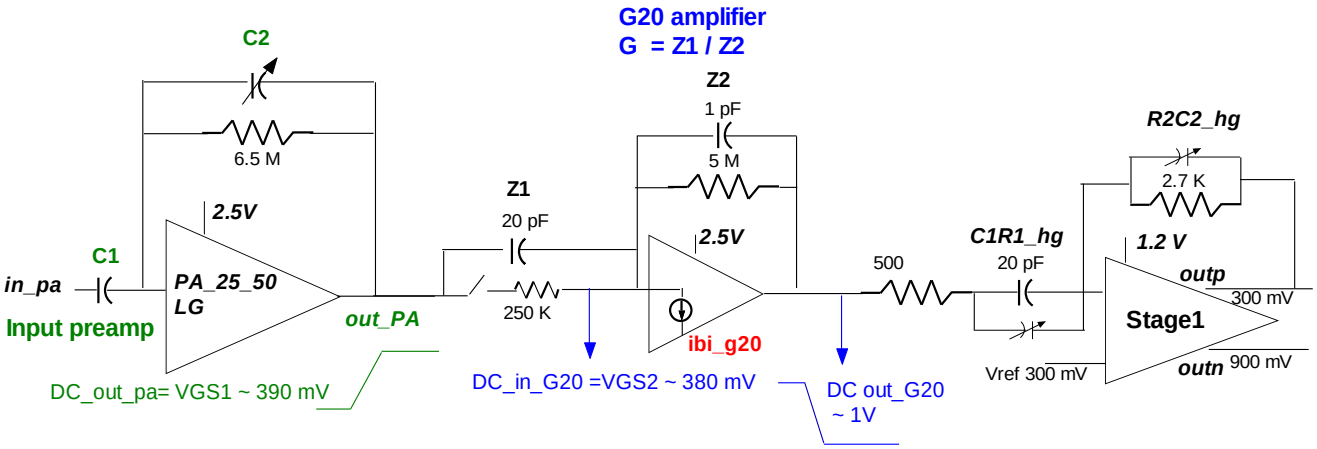
c2<0:8> of each channel (SC 15, 25,35): tuning of the input impedance.

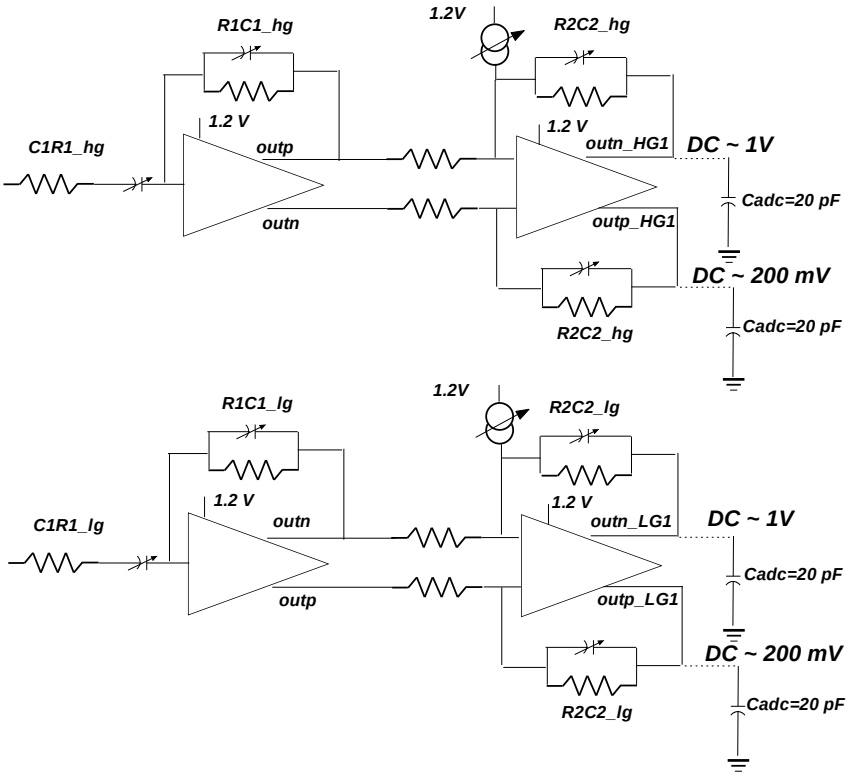
To get Zin= 25 Oms and for a dynamic range = 5 mA (cf SW_R025_5mA and 10 mA settings), c2<0:8> should be equal to 000011100= 112, which corresponds to c2= 1*500 fF + 1*1pF + 1*2 pF = 3.5 pF. The gain of the voltage amplifier is then G=c1/c2= 30 pF / 3.5 pF = 8.5 and Zin = R0/(G+1)= 220/9.5 = 23 Ohms

To get Zin= 25 Oms and for a dynamic range = 10 mA (cf SW_R025_5mA and 10 mA settings), c2<0:8> should be equal to

To get Zin= 50 Ohms (dynamic range is 2mA, not tune able), c2<0:8> should be equal to

Ampli G=20 (channel<1:3>)





Common SC:

dac_ibi_g20<5:0> (SC 6-11): DEF value = 110000 which corresponds to . Tuning of the bias input current of the amplifier used after the preamp (gain=20) for the HG path.

sw_DC_g20 (SC 76): when set to « 1 » DC connection between out_preamp and G20_amplifier input. If "0", AC connection

ON_g20: When "1", Gain 20 amplifier is ON.

Preamp for channel <4>

Power: vdda_pa and vdd_pa, 2.5V

Common SC parameters

sw_ibo (SC@ 0): Same as for channel <1:3>. The minimum current that flows in the input transistor is 3.5 mA. When set to 1, the current that flows in the input transistor is increased by 2.5 mA.

sw_ibi: Same as for channel <1:3>. When set to 1, the bias input current of the input transistor is 200 µA

Rf<0:3> (SC 45-48): Tuning of HG dynamic range. Rf<0>= 1K, Rf<1>=2K, Rf<2>= 5K, Rf<3>= 10K

c2<0:8> to tune the input impedance.

To get Zin= 25 Oms and for a dynamic range = 10 mA, c2<0:8> should be equal to 000100001, which correspond to c2= 1*250 fF + 1*8 pF = 8.250 pF. The gain of the voltage amplifier is then G=c1/c2= 30 pF / 8.25 pF = 3.6 and Zin = R0/(G+1)= 100/4.6 = 22 Ohms

To get Zin= 50 Ohms (dynamic range is 2mA, not tune able), c2<0:8> should be equal to

Buffer for channel <4>

ON_buffer

Discri for channel <4>

ON_discri

EN_discri

EN_discri_pad

CRRC2 shaper

One LG shaper and one HG shaper, both made of two stages: Stage 1 (s1) and stage 2(s2)

Stage 1: CR + RC stage, Stage 2: RC stage

Shaper amplifier @BNL

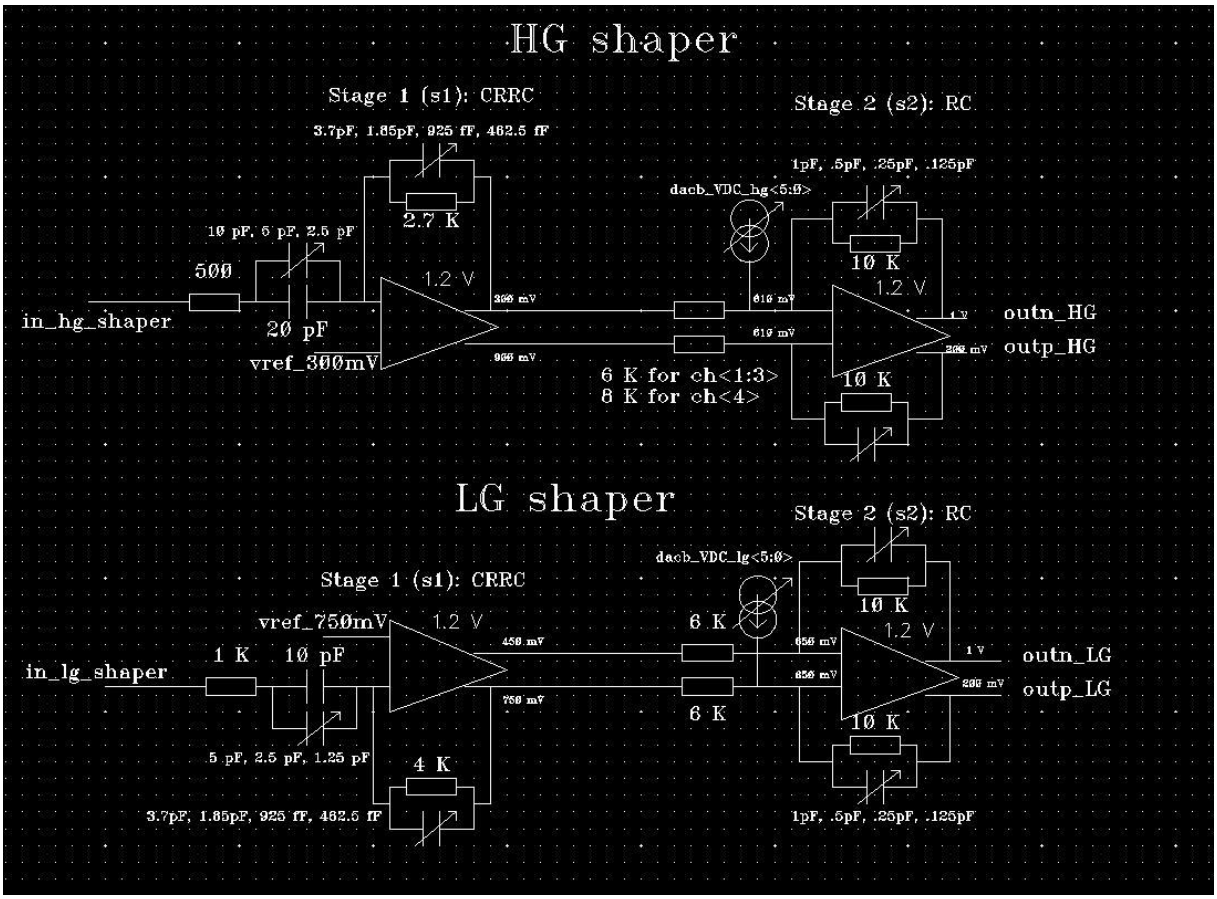
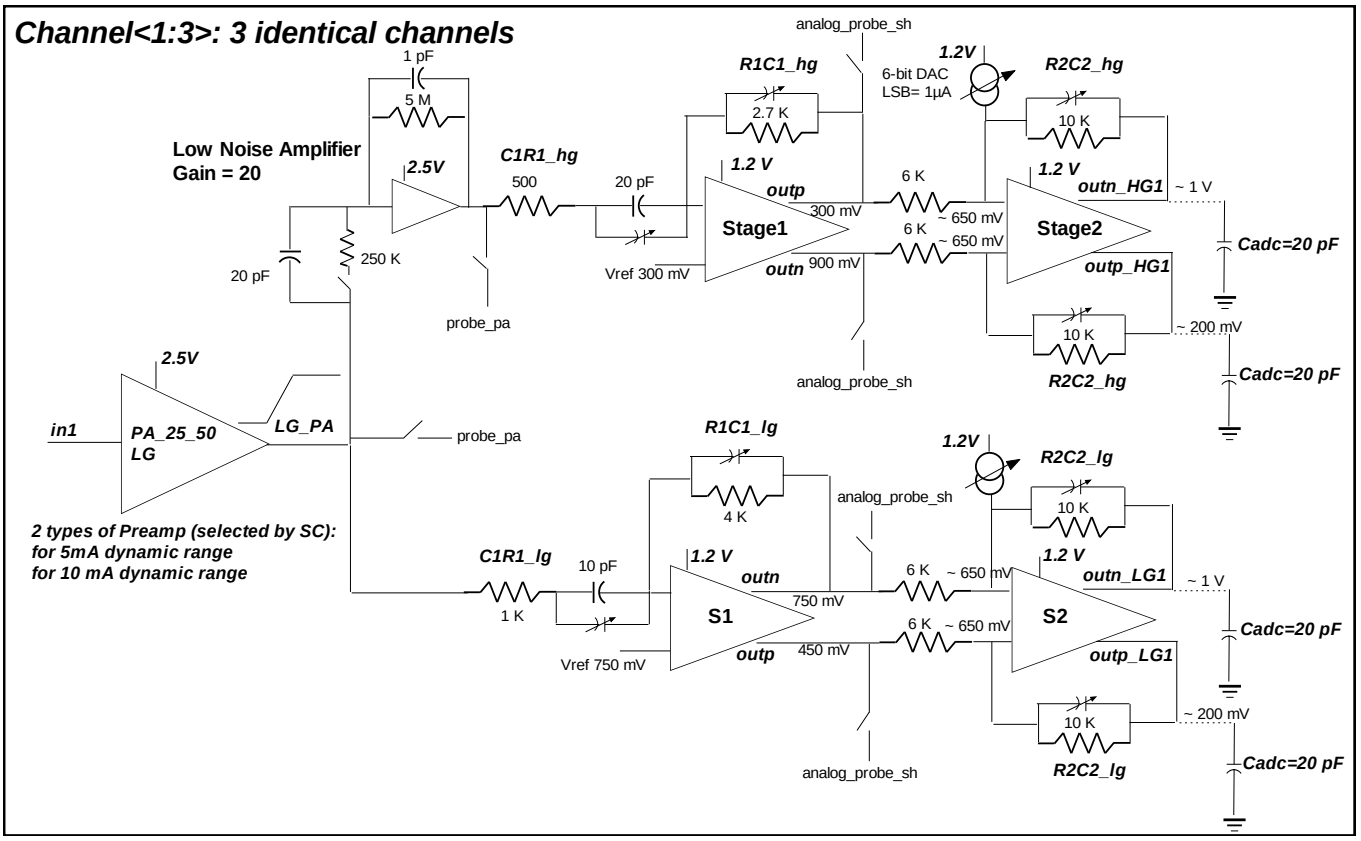


Figure 6: CRRC2 shapers (HG and LG)



HG CRRC settings

ON_HG_s1

rc_hg_s1<3:0>

cr_hg_s1<2:0>

ON_HG_s2

rc_hg_s2<3:0>

DAC_VDC_HG <i>: 6 bits DAC to tune DC output level (around 100 -200 mV for P output, 1 – 1.1V for N output

dac_VDC_hg<5:0>_ch<1>

dac_VDC_hg<5:0>_ch<2>

dac_VDC_hg<5:0>_ch<3>

dac_VDC_hg<5:0>_ch<4>

LG CRRC settings

ON_LG_s1

cr_lg_s1<2:0>

rc_lg_s1<3:0>

ON_LG_s2
rc_lg_s2<3:0>

DAC_VDC_LG <i>: 6 bits DAC to tune DC output level (around 100 -200 mV for P output, 1 – 1.1V for N output)

dac_VDC_lg<5:0>_ch<1>
dac_VDC_lg<5:0>_ch<2>
dac_VDC_lg<5:0>_ch<3>
dac_VDC_lg<5:0>_ch<4>= srout_sc

Bandgap and ampli

ON_Ref_BG: internal bandgap

Threshold setting (vth)

External 10bit-DAC to set the threshold of the discriminator of channel 4 (legacy channel)