COLUTAV2

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Revision History

Revision	Date	Author(s)	Description
0.0	March 14, 2018	RX	Created
0.1	September 1, 2018	RX	Name changed from “COLUTAV2” to “COLUTAV2”

Contents

1 Description

The COLUTAV2 device is a multi-channel, precision analog-to-digital converter (ADC) intended for instrumentation readout in radiation-prone areas. The device features two production ADC channels and one ADC channel for internal R&D. Each channel features a dynamic range enhancer (DRE) amplifier followed by a 12-bit ADC.

2 Physical Interface

Figure 1 and table 1 highlight the physical interconnections to the COLUTAV2 device.

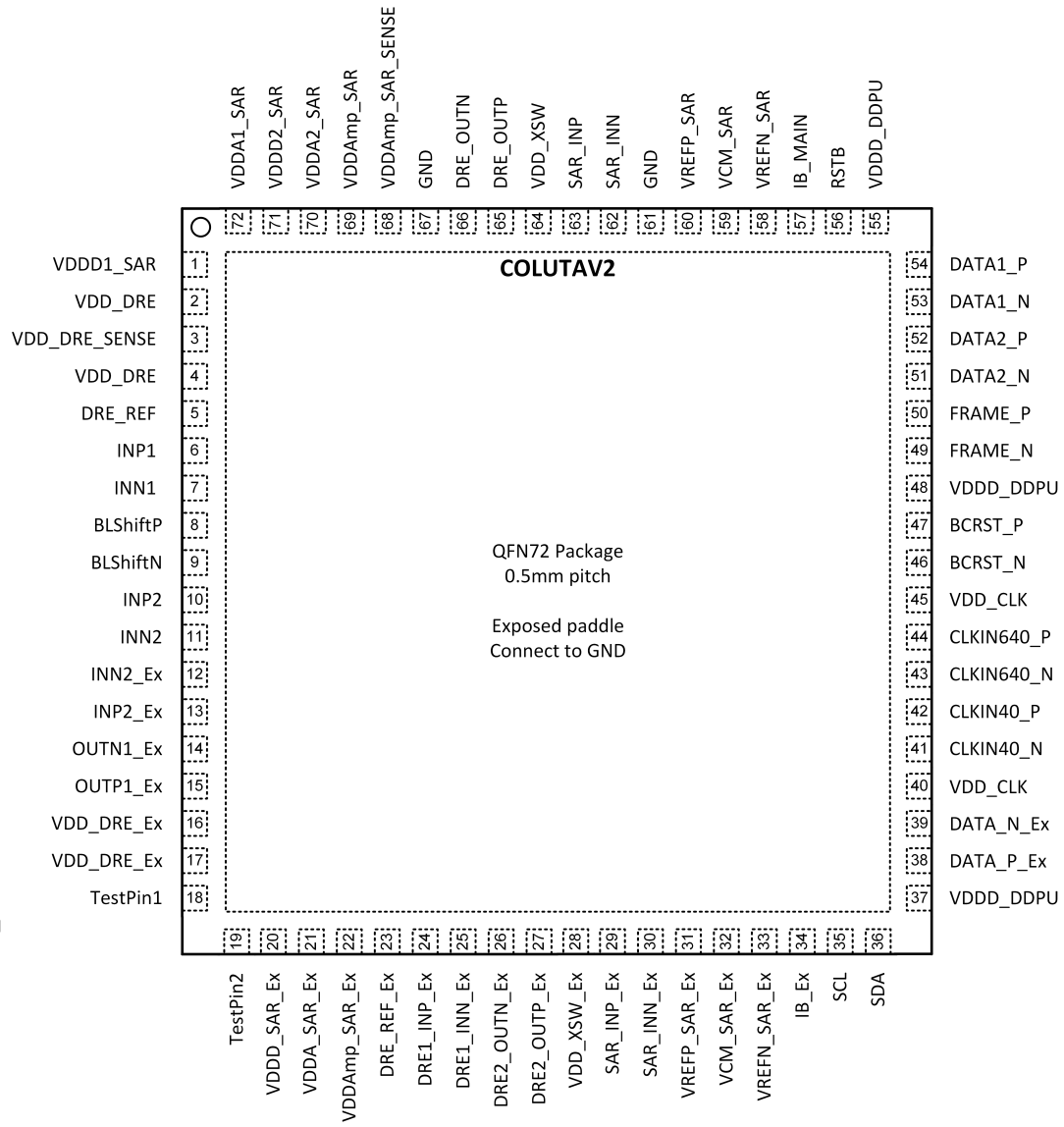

Figure 1: COLUTAV2 pin diagram

Table 1: Pin Mapping

Pin	Name	Direction	Description
1	VDDD1_SAR	Power	Channel 1 and 2 ADC first-stage digital 1.2V VDD
2	VDDD_DRE	Power	Channel 1 and 2 DRE digital 1.2V VDD
3	VDDA_DRE_SENSE	Analog Out	Channel 1 and 2 DRE digital VDD sense Out, at point-of-load
4	VDDA_DRE	Power	Channel 1 and 2 DRE analog 1.2V VDD
5	DRE_REF	Analog In	Channel 1 and 2 DRE reference voltage
6	INP1	Analog In	Channel 1 positive In
7	INN1	Analog In	Channel 1 negative In
8	BLShiftP	Analog In	Baseline offset positive In
9	BLShiftN	Analog In	Baseline offset negative In
10	INP2	Analog In	Channel 2 positive In
11	INN2	Analog In	Channel 2 negative In
12	INP1_Ex	Analog In	Experimental channel positive In
13	INN1_Ex	Analog In	Experimental channel negative In
14	DRE_REF_Ex	Analog In	Experimental channel DRE reference voltage
15	VDDA_DRE_Ex	Power	Experimental channel DRE analog 1.2V VDD
16	VDDA_DRE_SENSE_Ex	Power	Experimental channel DRE digital VDD sense Out, at point-of-load
17	VDDD_DRE_Ex	Power	Experimental channel DRE digital 1.2V VDD
18	TestPin1	Analog I/O	Test structure I/O
19	TestPin2	Analog I/O	Test structure I/O

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
20	VDDD_SAR_Ex	Power	Experimental channel SAR digital 1.2V VDD
21	VDDA_SAR_Ex	Power	Experimental channel SAR analog 1.2V VDD
22	VDDAmp_SAR_Ex	Power	Experimental channel SAR amplifier analog 1.2V VDD
23	VDDAmp_SAR_SENSE_Ex	Analog Out	Experimental channel SAR amplifier VDD sense Out, at point of load
24	GND	Power	Ground
25	DRE_OUTP_Ex	Analog Out	Experimental channel DRE testpoint, positive
26	DRE_OUTN_Ex	Analog Out	Experimental channel DRE testpoint, negative
27	VDD_XSW_Ex	Power	Experimental channel 1.2V global analog VDD
28	SAR_INP_Ex	Analog In	Experimental channel ADC positive testpoint
29	SAR_INN_Ex	Analog In	Experimental channel ADC negative testpoint
30	GND	Power	Ground
31	VREF_SAR_Ex	Analog In	Experimental channel ADC positive voltage reference
32	VCM_SAR_Ex	Analog In	Experimental channel ADC common-mode voltage reference
33	VREFN_SAR_Ex	Analog In	Experimental channel ADC negative voltage reference
34	IB_Ex	Analog In	Experimental channel master bias current
35	SCL	Digital In	I2C clock
36	SDA	Digital I/O	I2C data
37	VDDD_DDPU	Power	Global digital 1.2V VDD
38	DATA_N_Ex	Digital Out	Experimental channel sLVDS data Out, negative
39	DATA_P_Ex	Digital Out	Experimental channel sLVDS data Out, positive

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
40	VDD_CLK	Power	Global 1.2V VDD for clock sync/division/distribution
41	CLKIN40_N	Digital In	40MHz clock sLVDS In, negative
42	CLKIN40_P	Digital In	40MHz clock sLVDS In, positive
43	CLKIN640_N	Digital In	640MHz clock sLVDS In, negative
44	CLKIN640_P	Digital In	640MHz clock sLVDS In, positive
45	VDD_CLK	Power	Global 1.2V VDD for clock sync/division/distribution
46	BCRST_N	Digital In	Bunch crossing reset signal, negative
47	BCRST_P	Digital In	Bunch crossing reset signal, positive
48	VDDD_DDPU	Power	Global digital 1.2V VDD
49	FRAME_N	Digital Out	Frame synchronization signal, negative
50	FRAME_P	Digital Out	Frame synchronization signal, positive
51	DATA2_N	Digital Out	Channel 2 sLVDS data Out, negative
52	DATA2_P	Digital Out	Channel 2 sLVDS data Out, positive
53	DATA1_N	Digital Out	Channel 1 sLVDS data Out, negative
54	DATA1_P	Digital Out	Channel 1 sLVDS data Out, positive
55	VDDD_DDPU	Power	Global digital 1.2V VDD
56	RSTB	Digital In	I2C reset
57	IB_MAIN	Analog In	Channel 1 and 2 master bias current
58	VREFN_SAR	Analog In	Channel 1 and 2 ADC negative voltage reference
59	VCM_SAR	Analog In	Channel 1 and 2 ADC common-mode voltage reference

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
60	VREFP_SAR	Analog In	Channel 1 and 2 ADC positive voltage reference
61	GND	Power	Ground
62	SAR_INN	Analog In	Channel 1 ADC negative testpoint
63	SAR_INP	Analog In	Channel 1 ADC positive testpoint
64	VDD_XSW	Power	Channel 1 and 2 global analog 1.2V VDD
65	DRE_OUTN	Analog Out	Channel 1 DRE testpoint, negative
66	DRE_OUTP	Analog Out	Channel 1 DRE testpoint, positive
67	GND	Power	Ground
68	VDDAmp_SAR_SENSE	Analog Out	Channel 1 and 2 ADC amplifier analog VDD sense Out, at farthest point of load
69	VDDAmp_SAR	Power	Channel 1 and 2 ADC amplifier analog 1.2V VDD
70	VDDA2_SAR	Power	Channel 1 and 2 ADC second stage analog 1.2V VDD
71	VDDD2_SAR	Power	Channel 1 and 2 ADC second stage digital 1.2V VDD
72	VDDA1_SAR	Power	Channel 1 and 2 ADC first stage analog 1.2V VDD

3 Electrical Interface

The COLUTAV2 device must be driven according to the specifications described within this section for optimal performance. Two independent pairs of differential analog inputs exist for the two production channels, and a single pair of differential analog input exist for internal R&D purposes. All analog inputs are DC-coupled to the CMOS circuitry within the chip. Electrical interfacing to the COLUTAV2 analog inputs are summarized in table 2.

Temp=entire range, all corners, VDD=1.2V

Specification	Notes	Min	Typ	Max	Units
R_S Source resistance	C_L is fixed. Single-ended values.			20	Ohms
C_L Capacitive load			16		pF
V_{FS} Full-scale swing	Differential			2.0	Volts pk-pk
$V_{FS[U,L]}$ Input range	Single-ended. With respect to ground.	0.1		1.1	Volts
V_{CM} Common-mode input voltage	VDD/2		0.6		Volts
Target Peak SNDR		69			dBV
Target Dynamic Range		80			dBV

Table 2: Requirements for driving the INP1, INN1, INP2, INN2, BLShiftP, and BLShiftN inputs.

3.1 Driver Impedance Considerations

The combination of the preceding amplifier and the COLUTAV2 input can be abstracted to a finite-resistance source, a sampling switch, and a sampling capacitor, as shown in figure 2. To satisfy the target SNDR and dynamic range of the COLUTAV2, the source resistance of the driving amplifier (R_S) must be 20 Ohms or less. The maximum permissible source resistance was derived by subtracting the switch on-resistance (R_{SW}) from the maximum time constant that is able to satisfy settling to the target accuracy. The sampling switch is closed for a duration of 12.5nS with a periodicity of 25nS to achieve 40MSPS operation.

3.2 Analog Waveform Considerations

In addition to a differential input signal, a DC differential baseline input (BLShiftP and BLShiftN) is required to properly DC-couple the differential analog input signal within the COLUTAV2 chip. The driving requirements for the baseline inputs are the same as the analog input signal. It is recommended to have off-chip decoupling to provide a clean DC baseline value. The baseline value is shared amongst all channels in the COLUTAV2 chip. The definition of the analog input waveform and the baseline is presented in figures 3 and 4. In the provided example, the positive baseline would be +0.3V and the negative baseline would be +0.9V, with respect to ground.

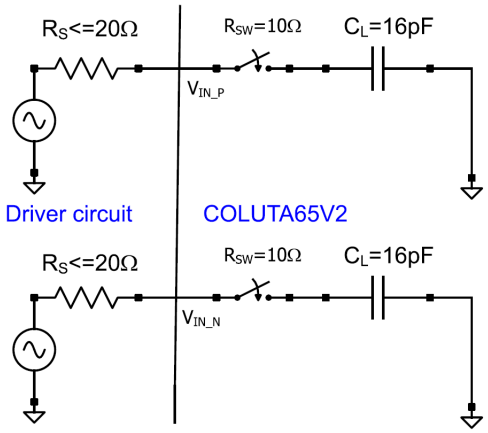

Figure 2: Differential equivalent input circuit of the COLUTAV2.

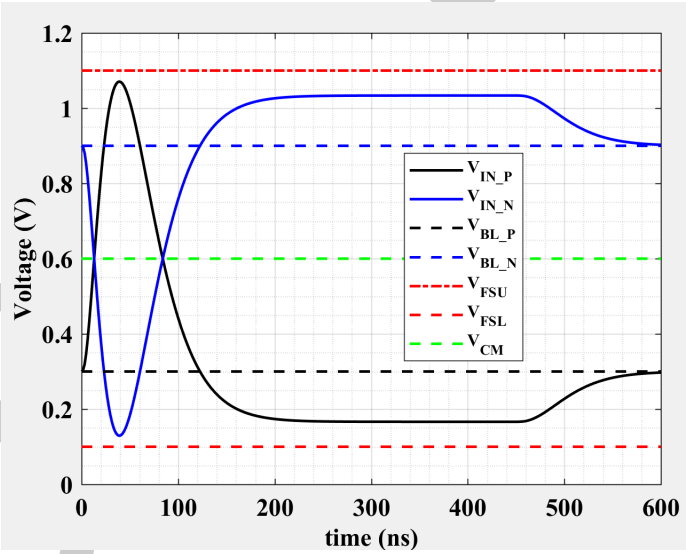

Figure 3: Example of a differential physics signal, as it would be presented to the VINP and VINN inputs, with the common-mode voltage and input range annotated.

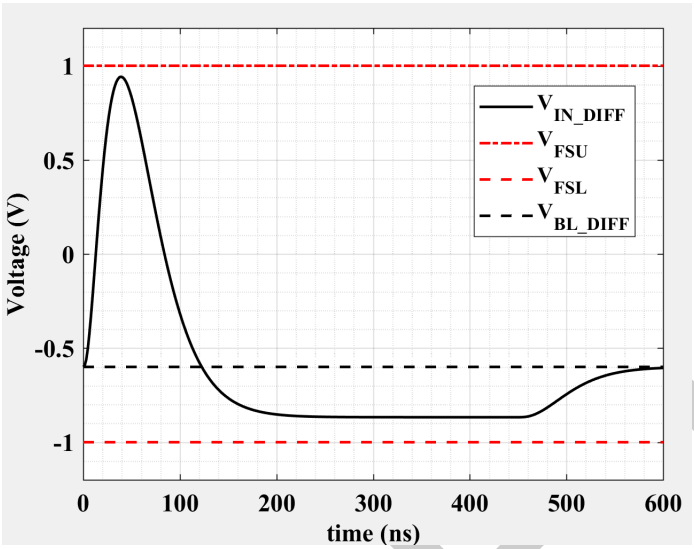

Figure 4: Example of a differential physics signal, where $V_{IN\_DIFF} = V_{INP} - V_{INN}$ and $V_{BL\_DIFF} = V_{BLShiftP} - V_{BLShiftN}$, with the baseline and input range annotated. The common-mode voltage is removed by the differential nature.

4 I²C Control Interface

The COLUTAV2 is intended to be used as an I²C slave device. The control structure of the chip features independently addressable write-only bits, where these bits are partitioned on a per-channel basis (“slow-control") and a set of general-purpose use bits (“global-control"). The on-chip I²C controller addresses uses one-hot encoding to address the slow-contorl blocks, thus all slow-control bits may either by address individually or simultaneously according to 3. The I²C slave controller can independently address up to eight slow-control regions and a single general-purpose region.

Address	Destination
8'h01	Channel 1
8'h02	Channel 2
8'h04	Experimental channel DRE1 only
8'h08	Experimental channel
8'h10 - 8'h80	Unused

Table 3: Slow-control addressing.

4.1 Slow-control Control Bits

Table 4 detail the assignments of the slow-control bits. The highest bit position indicates the most-significant bit. The bit assignments for each slow-control block (channel) are identical, unless otherwise noted.

Table 4: Slow-control bit mapping

Bit position	Description
<223>	**TX:Drive Strength** Default: `1'b1`
<222:215>	**SAR:PBoost VREF** Default: `8'h37`
<214:207>	**SAR:NBoost VREF** Default: `8'h37`
<206:199>	**SAR:Main Amplifier VREF** Default: `8'h37`
<198:194>	**SAR:PBoost Bias** Default: `5'h06`
<193:189>	**SAR:NBoost Bias** Default: `5'h06`
<188:184>	**SAR:Main Bias** Default: `5'h06`
<183:176>	**SAR:FStage Delay** Default: `8'hFF`
<175:168>	**SAR:CStage Delay** Default: `8'hFF`
<167>	**SAR:Decision width** Default: `1'b0` 1'b0: 50% Decision duty cycle 1'b1: 25% Decision duty cycle
<166:158>	**SAR:Cal Reg B** Default: `9'h000`
<157:149>	**SAR:Cal Reg A** Default: `9'h000`
<148>	**SAR:Enable Cal FStage** Default: `1'b0` 1'b0: Normal conversion mode 1'b1: Calibration mode
<147>	**SAR:Enable Cal CStage** Default: `1'b0` 1'b0: Normal conversion mode 1'b1: Calibration mode

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Table 4 – *Continued from previous page*

Bit position	Description
<146>	**SAR:Enable DRE-to-SAR** Default: `1'b0` 1'b0: Path disabled 1'b1: Path enabled
<145>	**SAR:Enable Ext-to-SAR** Default: `1'b0` 1'b0: Path disabled 1'b1: Path enabled
<146>	**DRE-Ex:DRE2DRE_EN** Default: `1'b1` Only applies to Experimental channel DRE1. Bits <223:147> are unassigned in Experimental channel DRE1 slow-control block.
<145>	**DRE-Ex:EXT2DRE_EN** Default: `1'b0` Only applies to Experimental channel DRE1. Bits <223:147> are unassigned in Experimental channel DRE1 slow-control block.
<144>	**DRE:MS** Default: `1'b1` Manual select 1'b0: Auto-gain 1'b1: Gain determined by DRE:GS
<143>	**DRE:GS** Default: `1'b1` Gain select 1'b0: 4x gain 1'b1: 1x gain
<142>	**DRE:ENSARIN** Default: `1'b1` Enable DRE-to-SAR path
<141>	**DRE:ENASD** Default: `1'b1` Enable DRE-to-Ext path
<140>	**DRE:OUTEXTERNALEN** Default: `1'b0` Enable DRE-to-Ext path
<139:132>	**DRE:IDAC** Default: `8'hA8`
<131>	**DRE:CLK_EN** Default: `1'b1`

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Table 4 – *Continued from previous page*

Bit position	Description
<130:128>	**DRE:AmpSt2** Default: `3'h0`
<127:125>	**DRE:REFDAC** Default: `3'h1`
<124:120>	**DRE:CAPGAIN** Default: `5'h00`
<119>	**DRE:BLShiftSA** Default: `1'b0`
<118>	**DRE:MilSt2CMFB_EN** Default: `1'b0`
<117>	**DRE:BLPol** Default: `1'b1`
<116>	**DRE:BLShift** Default: `1'b0`
<115:104>	**DDPU: Gain-4 Pedestal** Default: 2106 Pedestal needed to correctly compute gain-4 ADC value.
<103:92>	**DDPU: Gain Offset** Default: –
<91:78>	**DDPU: SAR CStage[5]** Default: 14'h2000 (14'd8192) SAR CStage bit [5] weight.
<77:65>	**DDPU: SAR CStage[4]** Default: 13'h1000 (13'd4096) SAR CStage bit [4] weight.
<64:53>	**DDPU: SAR CStage[3]** Default: 12'h800 (12'd2048) SAR CStage bit [3] weight.
<52:42>	**DDPU: SAR CStage[2]** Default: 11'h400 (11'd1024) SAR CStage bit [2] weight.
<41:32>	**DDPU: SAR CStage[1]** Default: 10'h200 (10'd512) SAR CStage bit [1] weight.
<31:23>	**DDPU: SAR CStage[0]** Default: 9'h100 (9'd256) SAR CStage bit [0] weight.
<22:13>	**DDPU: SAR FStage[9]** Default: 10'h200 (10'd512) SAR FStage bit [9] weight.

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Table 4 – *Continued from previous page*

Bit position	Description
<12:4>	**DDPU: SAR FStage[8]** Default: 9'h100 (9'd256) SAR FStage bit [8] weight.
<3>	**DDPU: Serializer Mode** Default: 1'b0 1'b0: Data output mode 1'b1: Test pattern output 16'h8EF0
<2>	**DDPU: Correction mode Mode** Default: 1'b1 1'b0: SAR bits uncorrected; no DRE correction 1'b1: SAR bits corrected; DRE corrected
<1:0>	**DDPU: Arithmetic mode** Default: 2'b11 2'b00: raw data mode 2'b01: SAR cal mode 2'b10: DRE cal mode 2'b11: normal data mode

For the DDPU, the data output register assignments for the four artihmetic modes are as follows:

- `assign normal_mode_data = 2'b00, overflow, dre_r6[0], SAR_corr[11:0];`
- `assign SAR_calib_data = sar1_r2, sar2_r2;`
- `assign DRE_calib_data = 1'b0, dre_r6[1], dre_r6[2], dre_r6[0], SAR_sum[11:0];`
- `assign raw_mode_data = dre_r2[2], dre_r2[0], sar1_r2, sar2_r2[9:2];`

4.2 Global Control Bits

The global control bits (table 5) are allocated to shared resources, including the BCID transmitter control and dosimeter/test structures control.

Table 5: Global-control bit mapping

Bit position	Description
<63:54>	**Unused** Default:

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Table 5 – *Continued from previous page*

Bit position	Description
<53>	**SAR_ENABLE, Experimental channel** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<52>	**SAR_ENABLE, Channel 1** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<51>	**SAR_ENABLE, Channel 2** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<50:48>	**Test Struct: switch-cap voltage select** Default: `3'h4` 3'h0: not used 3'h1: 1/8 VDD 3'h2: 2/8 VDD 3'h3: 3/8 VDD 3'h4: 4/8 VDD 3'h5: 5/8 VDD 3'h6: 6/8 VDD 3'h7: 7/8 VDD

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Table 5 – *Continued from previous page*

Bit position	Description
<47:43>	**Test Struct: cap select** Default: `5'h10` 5'h00: LCAP-8D 5'h01: LCAP-7 5'h02: LCAP-7D 5'h03: LCAP-6 5'h04: LCAP-6D 5'h05: LCAP-5 5'h06: LCAP-5D 5'h07: LCAP-4 5'h08: LCAP-4D 5'h09: LCAP-3 5'h0A: LCAP-3D 5'h0B: LCAP-2 5'h0C: LCAP-2D 5'h0D: LCAP-1 5'h0E: LCAP-1D 5'h0F: LCAP-0 5'h10: SCAP-0 5'h11: SCAP-1D 5'h12: SCAP-1 5'h13: SCAP-2D 5'h14: SCAP-2 5'h15: SCAP-3D 5'h16: SCAP-3 5'h17: SCAP-4D 5'h18: SCAP-4 5'h19: SCAP-5D 5'h1A: SCAP-5 5'h1B: SCAP-6D 5'h1C: SCAP-6 5'h1D: SCAP-7D 5'h1E: SCAP-7 5'h1F: SCAP-8

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Table 5 – *Continued from previous page*

Bit position	Description
<42:40>	**Test Struct: SK device select** Default: `3'h0` 3'h0: TP2=PLVT1; TP1=NLVT1 3'h1: TP2=PLVT2; TP1=NLVT2 3'h2: TP2=RPWO1; TP1=RNWO1 3'h3: TP2=RPWO2; TP1=RNWO2 3'h4: TP2=P1; TP1=N1 3'h5: TP2=P2; TP1=N1 3'h6: TP2=RPW1; TP1=NHVT1 3'h7: TP2=RPW2; TP1=NHVT2
<39>	**Test Struct: IOA unity gain** Default: `1'b0` 1'b0: Opened circuit (nonunity gain) 1'b1: Closed circuit (unity gain)
<38:36>	**Test Struct: IOA front-end resistor-ratio Rf/Rg** Default: `3'h0` 3'h0: x4/8 3'h1: x4/7 3'h2: x4/6 3'h3: x4/5 3'h4: x4/4 3'h5: x4/3 3'h6: x4/2 3'h7: x4/1
<35:33>	**Test Struct: IOA back-end resistor-ratio Rf/Rg** Default: `3'h7` 3'h0: x8 3'h1: x7 3'h2: x6 3'h3: x5 3'h4: x4 3'h5: x3 3'h6: x2 3'h7: x1
<32>	**Test Struct: IOA offset enable** Default: `1'b0` 1'b0: Disabled 1'b1: Enabled

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Table 5 – *Continued from previous page*

Bit position	Description
<31>	**Test Struct: IOA Enable First-Stage N** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<30>	**Test Struct: IOA Enable First-Stage P** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<29>	**Test Struct: IOA Enable Second-Stage** Default: `1'b1` 1'b0: Disabled 1'b1: Enabled
<28:24>	**Test Struct: IOA bias DAC** Default: `5'h0A`
<23:20>	**Test Struct: dosiemeter select** Default: `4'h0` 4'h0: DI: PLG4 vs PIO4 4'h1: DI: PLG8 vs PIO8 4'h2: DI: NLG4 vs NIO4 4'h3: DI: NLG8 vs NIO8 4'h4: DICAL: PLG4 vs PLG4_REF 4'h5: DICAL: PIO4 vs PIO4_REF 4'h6: DICAL: PLG8 vs PLG8_REF 4'h7: DICAL: PIO8 vs PIO8_REF 4'h8: DICAL: NLG4 vs NLG4_REF 4'h9: DICAL: NIO4 vs NIO4_REF 4'hA: DICAL: NLG8 vs NLG8_REF 4'hB: DICAL: NIO8 vs NIO8_REF 4'hC: TEMP: VREF vs PLG4 4'hD: TEMP: VREF vs NLG4 4'hE: AUXCAL: VREF vs VREF 4'hF: AUXCAL: INREF vs IPREF
<19:15>	**Test Struct: dosiemeter bias DAC** Default: `5'h0B`
<14:10>	**Test Struct: spare DAC** Default: `5'h00`

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Table 5 – *Continued from previous page*

Bit position	Description
<9:8>	**Test Struct: MUXOUT select** Default: `2'h0` 2'h0: Instrumentation amplifier to TP 2'h1: Dosimeter bypass to TP 2'h2: SK test structure to TP 2'h3: Monitor (TP1=VTOP_SET; TP2=spare DAC
<7:6>	**Test Struct: MUXAMP select** Default: `2'h0` 2'h0: Direct IN to amplifier (MUXAMP) 2'h1: Dosimeter to amplifier 2'h2: LCAP to amplifier 2'h3: SCAP to amplifier
<5:4>	**Test Struct: MUXIN select** Default: `2'h0` 2'h0: Direct IN to amplifier (MUXIN) 2'h1: IN to amplifier offset 2'h2: IN to SWCAP (VINP=VBOT; VINN=VRST) 2'h3: No connect
<3>	**Unused** Default:
<2>	**BCID_TX: drive strength** Default: `1'b1`
<1:0>	**CLK: sync mode** Default: `2'h1` 2'h0: Sync to CP40 input 2'h1: Sync to BC_Reset 2'h2: No sync 2'h3: No sync (illegal)