

6

5

4

3

2

1

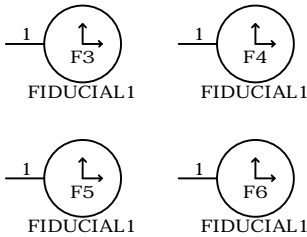
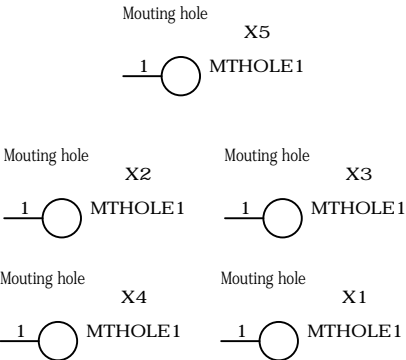
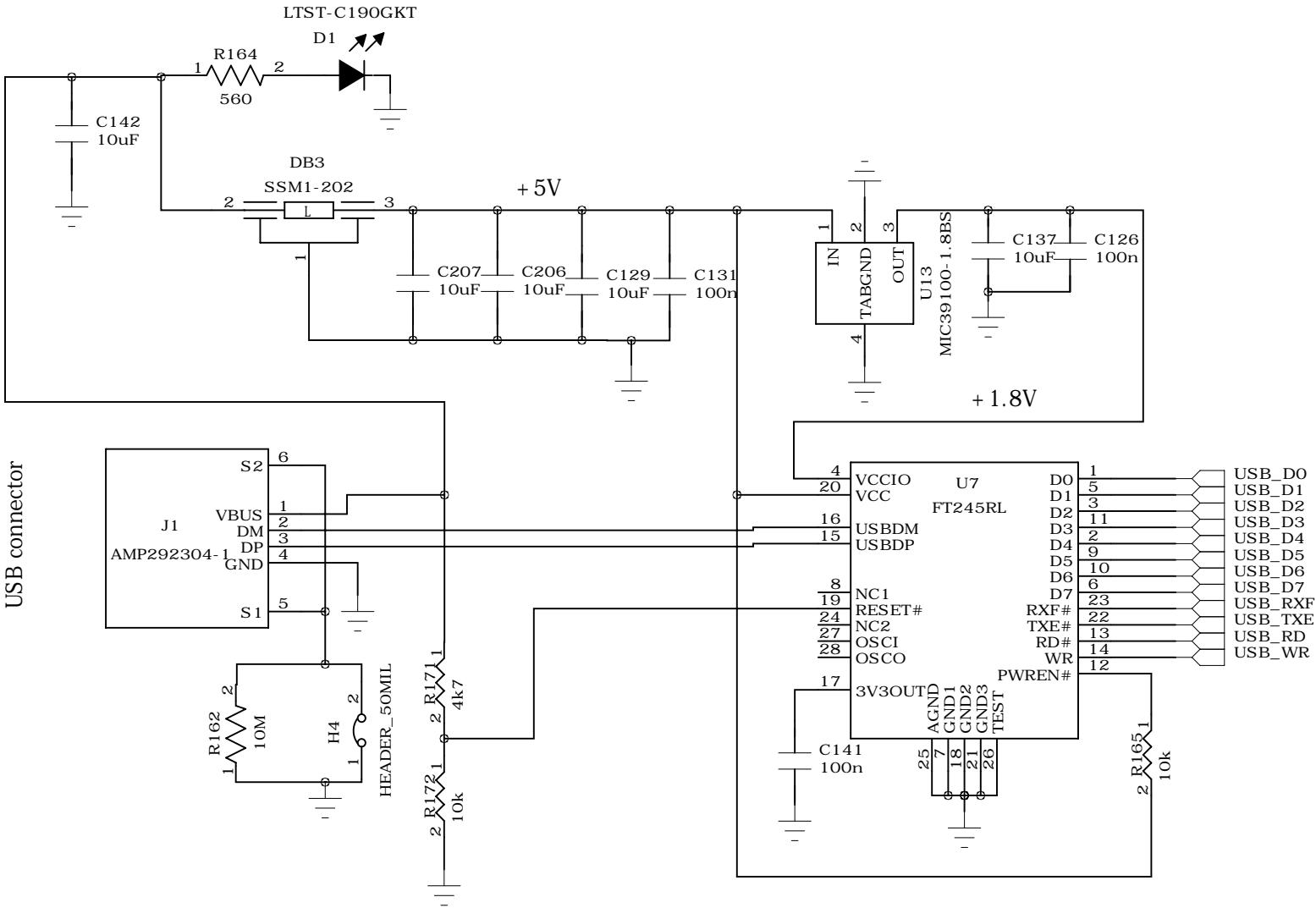
D

C

B

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:	< Checked By >	DATED:	< Checked Date >
QUALITY CONTROL:	< QC By >	DATED:	< QC Date >
RELEASED:	jb	DATED:	< Release Date >

CODE:	SIZE:	DRAWING NO:	REV:
< Code >	B	v0	0
SCALE: < Scale >			SHEET: 1 of 27

D

C

B

A

6

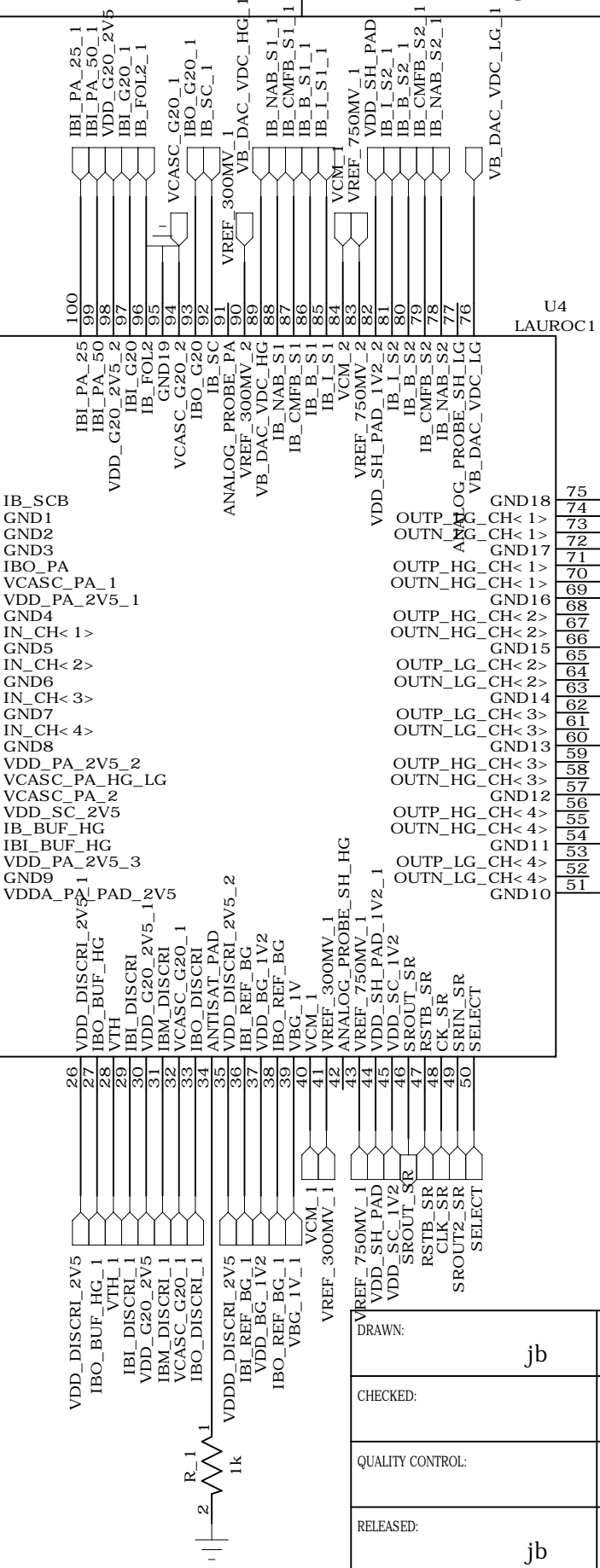
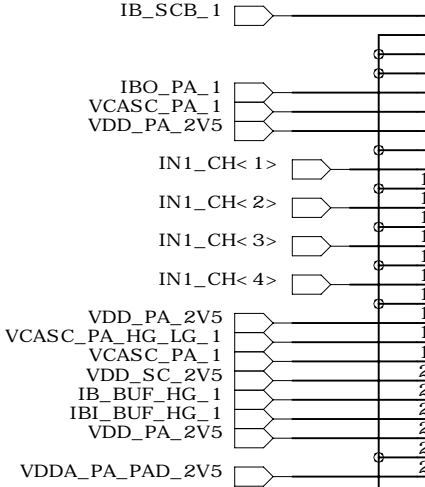
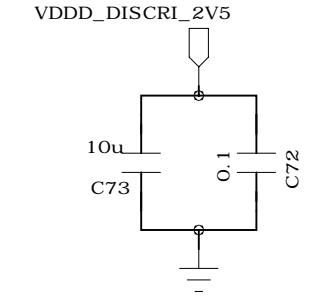
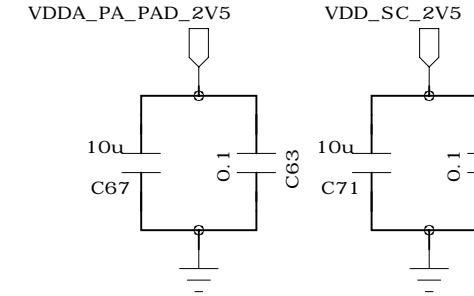
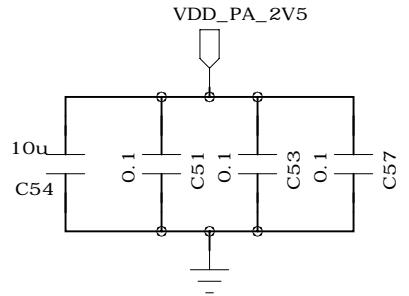
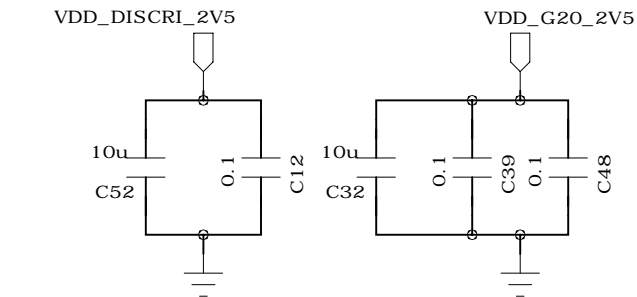
5

4

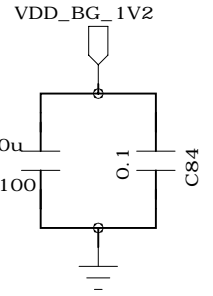
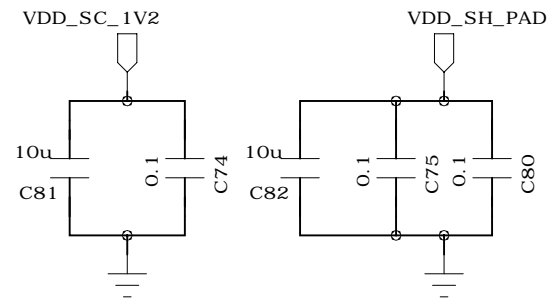
3

2

1



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:		SHEET: 20F 27	

DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

D

C

B

A

D

C

B

A

6

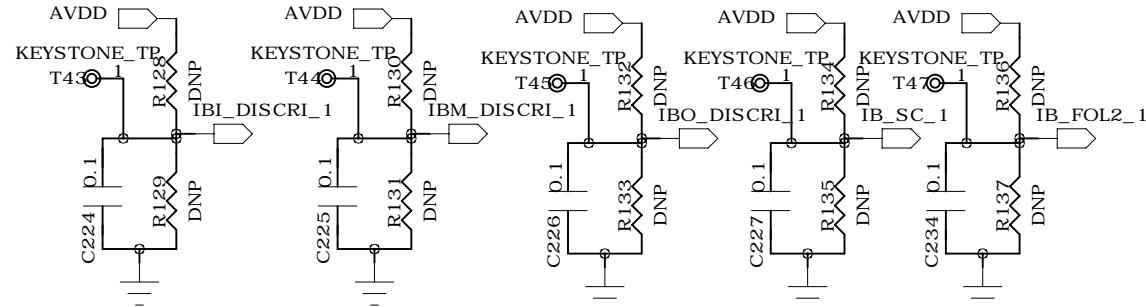
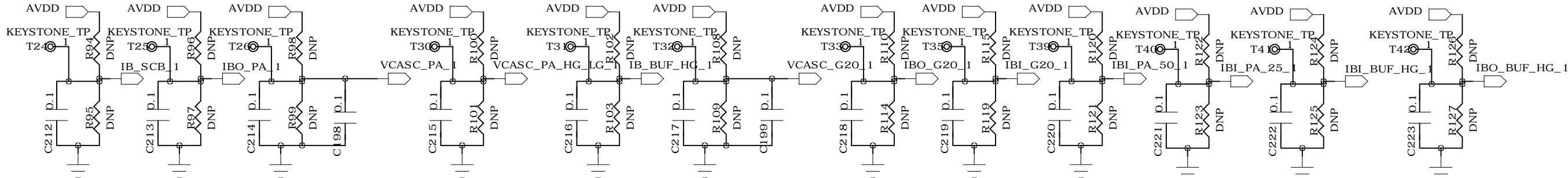
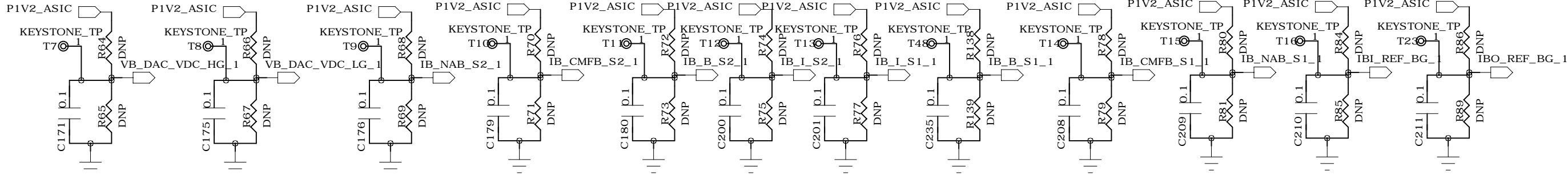
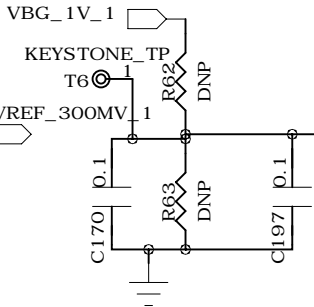
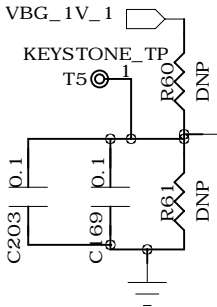
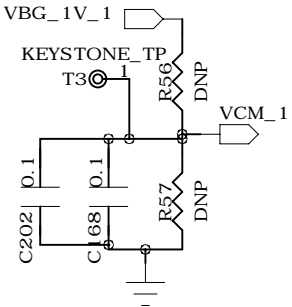
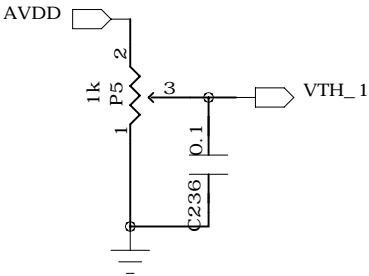
5

4

3

2

1



REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

D

C

B

A

COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:	jb	DATED:	

CODE:	SIZE:	DRAWING NO:	REV:
	B	v0	0
SCALE:	SHEET: 3F 27		

D

C

B

A

6

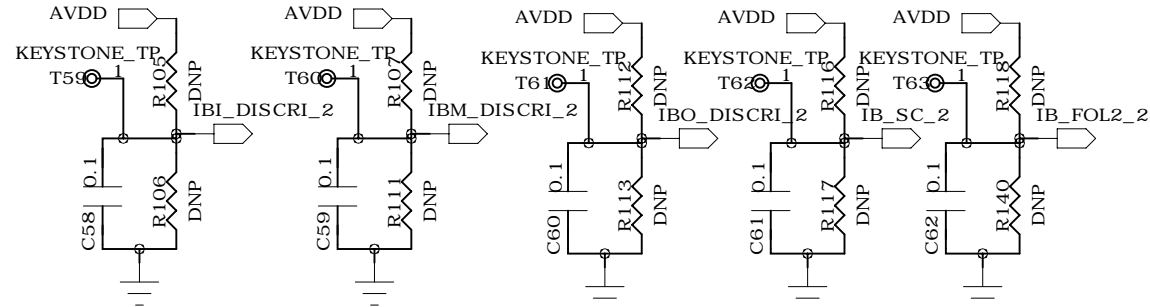
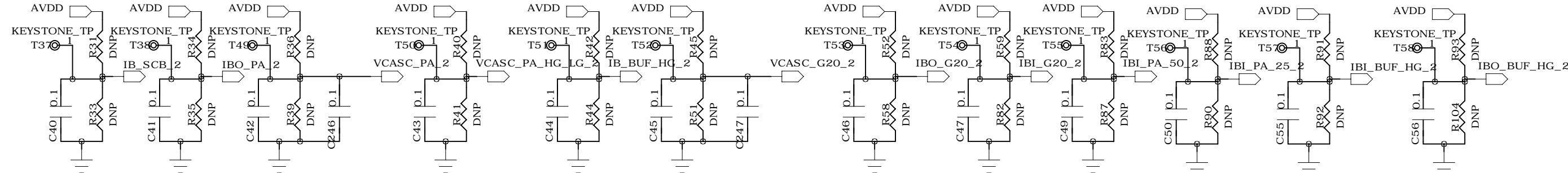
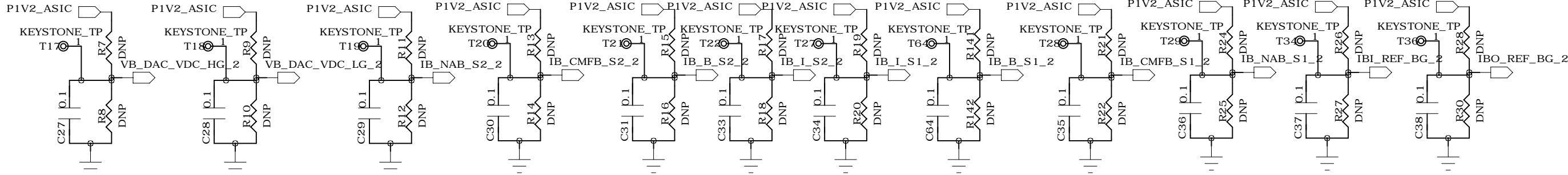
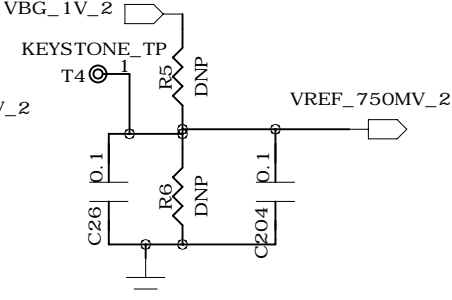
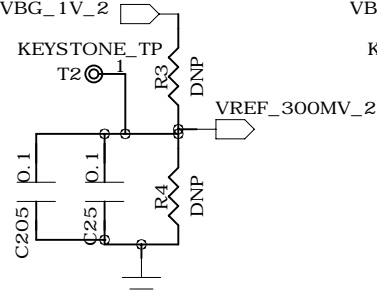
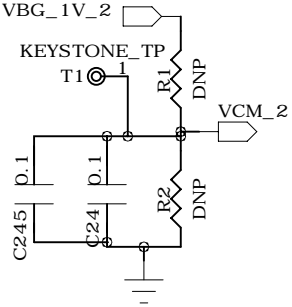
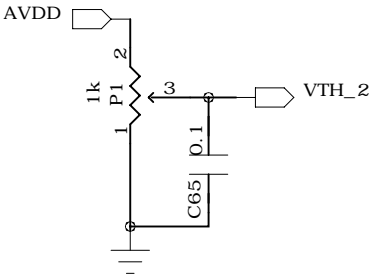
5

4

3

2

1



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

C

B

A

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:			SHEET: 5F 27

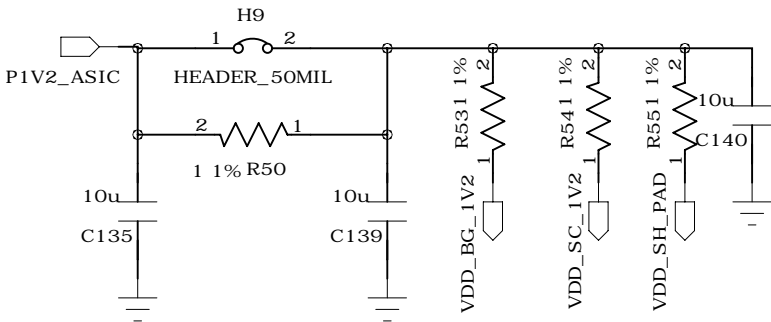
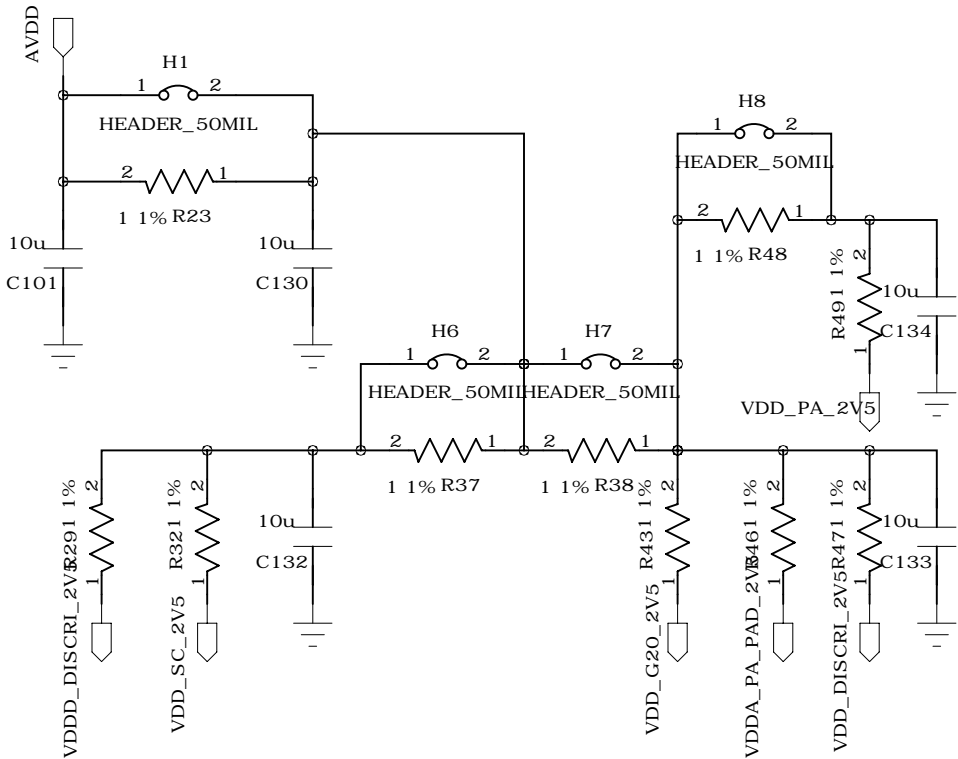
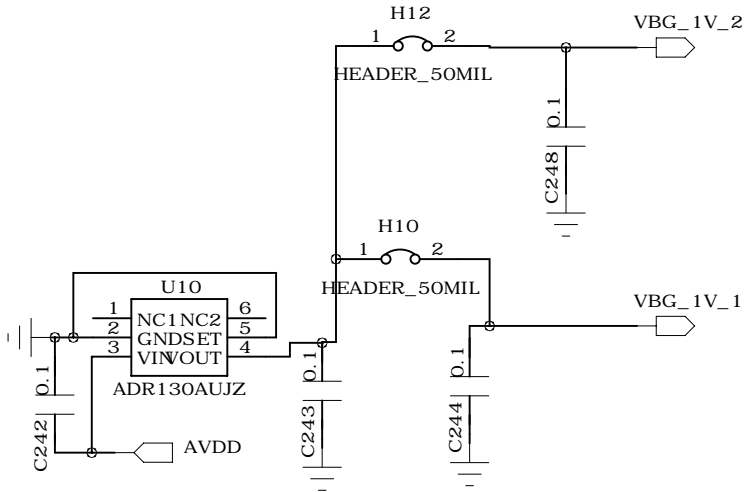
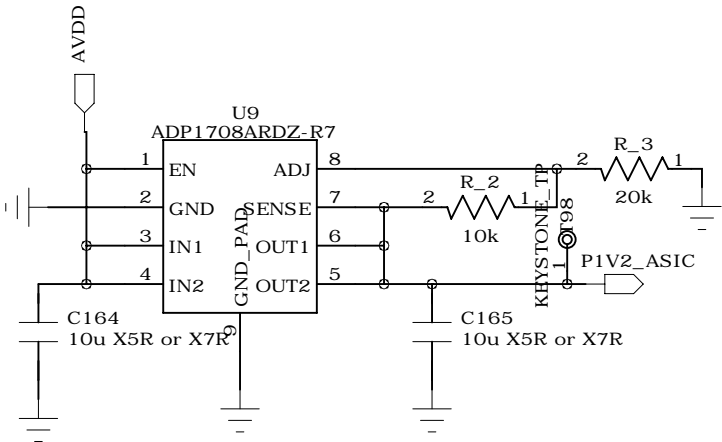
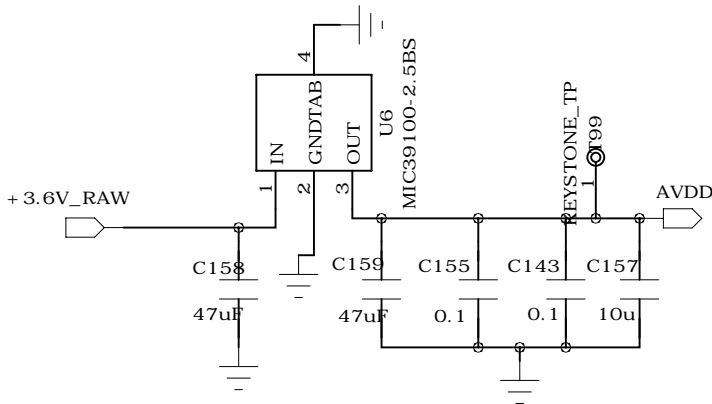
DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

D

C

B

A



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

C

B

A

DRAWN:	jb	DATED:	Jan 2019
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:	jb	DATED:	

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:		SHEET: 6 OF 27	

D

C

B

A

6

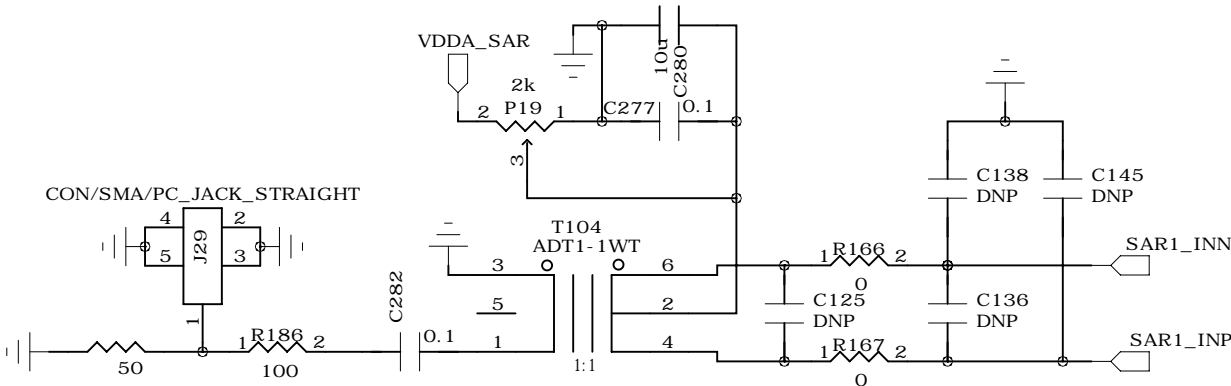
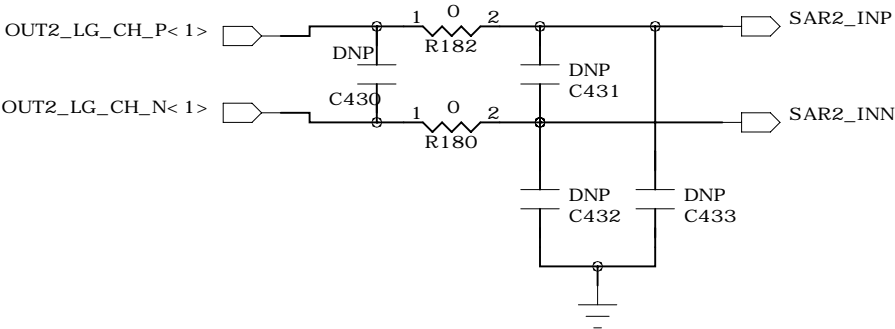
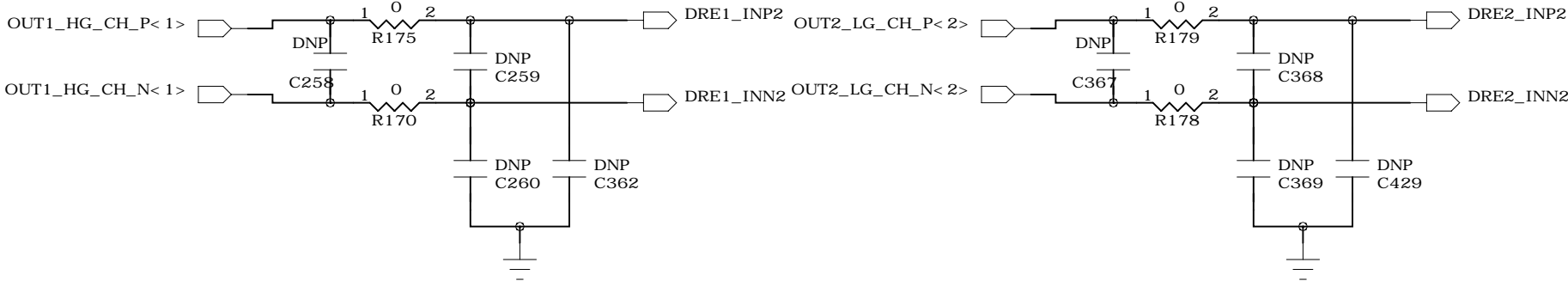
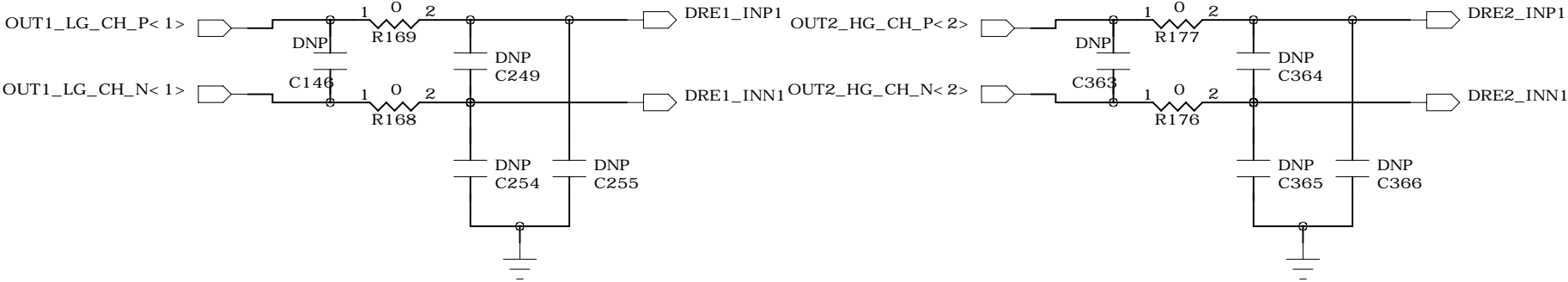
5

4

3

2

1



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

C

B

A

COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:	< Checked By >	DATED:	< Checked Date >
QUALITY CONTROL:	< QC By >	DATED:	< QC Date >
RELEASED:	jb	DATED:	< Release Date >

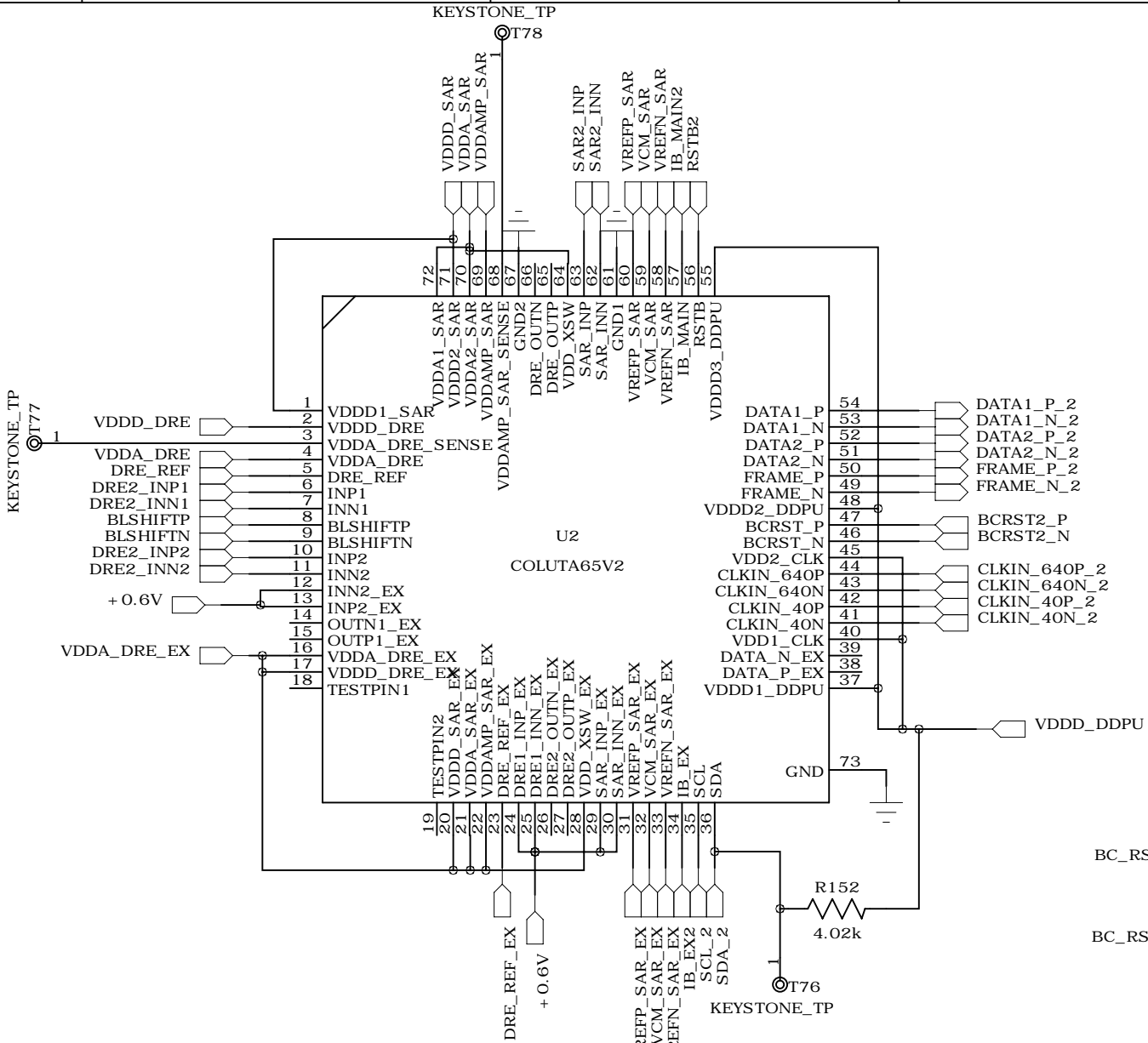
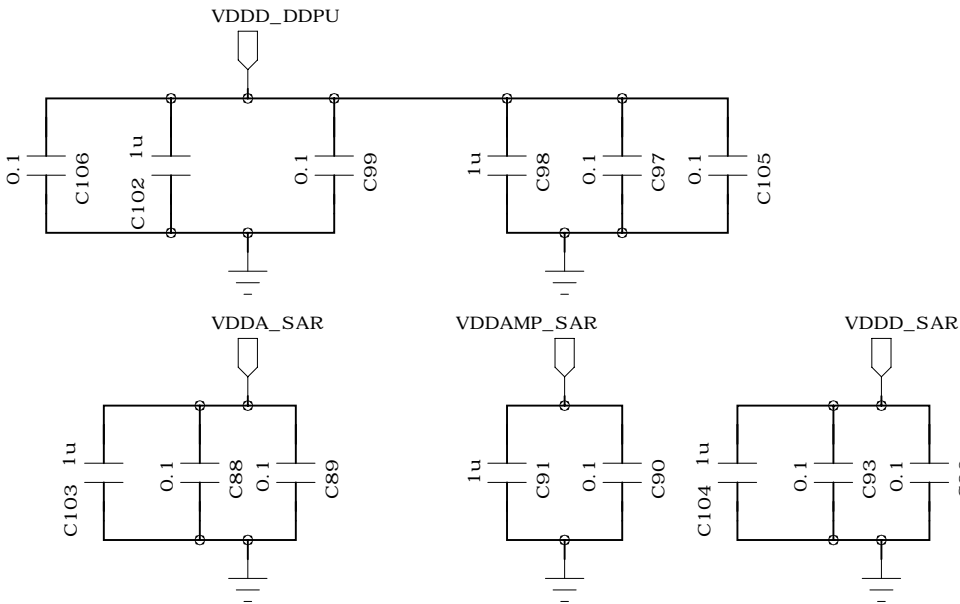
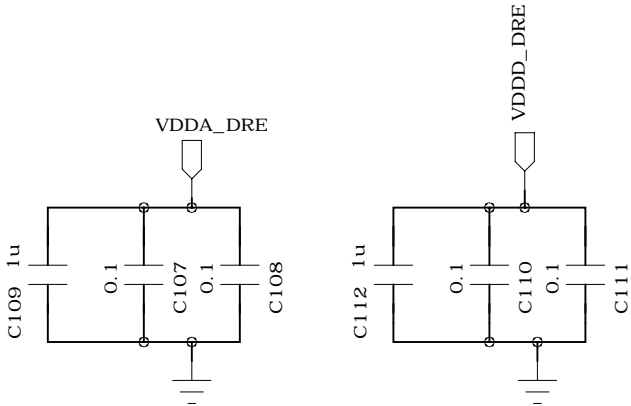
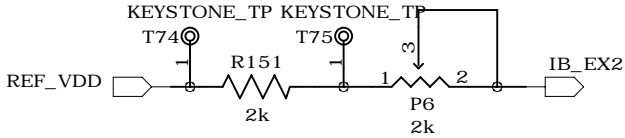
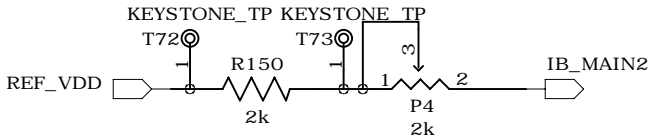
CODE:	SIZE:	DRAWING NO:	REV:
< Code >	B	v0	0
SCALE: < Scale >			SHEET: 7 of 27

D

C

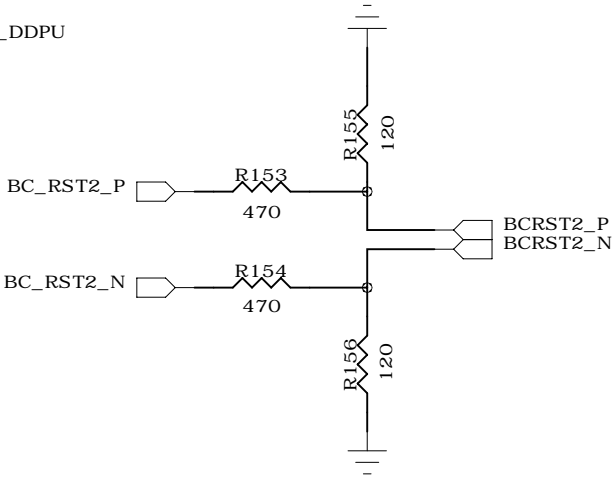
B

A



1

LVDS_E_3R to SLVS convertor



D

C

B

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE: < Scale >		SHEET: 27	

DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

6

5

4

3

2

1

D

D

C

C

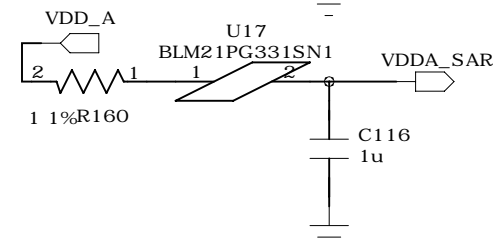
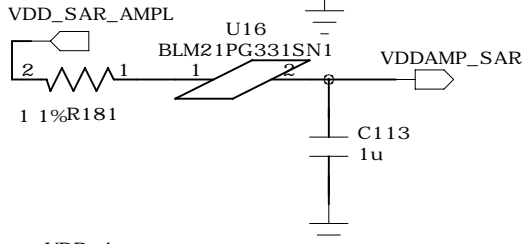
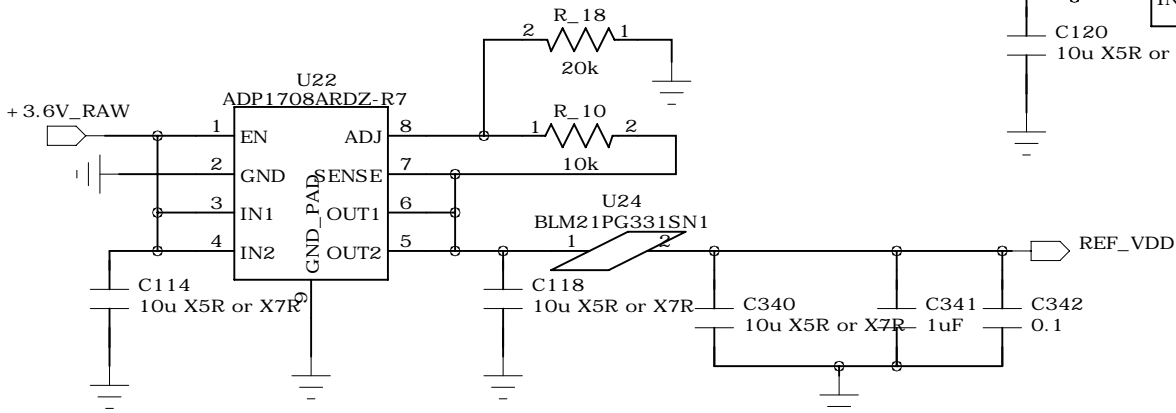
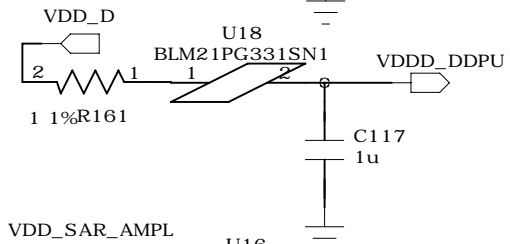
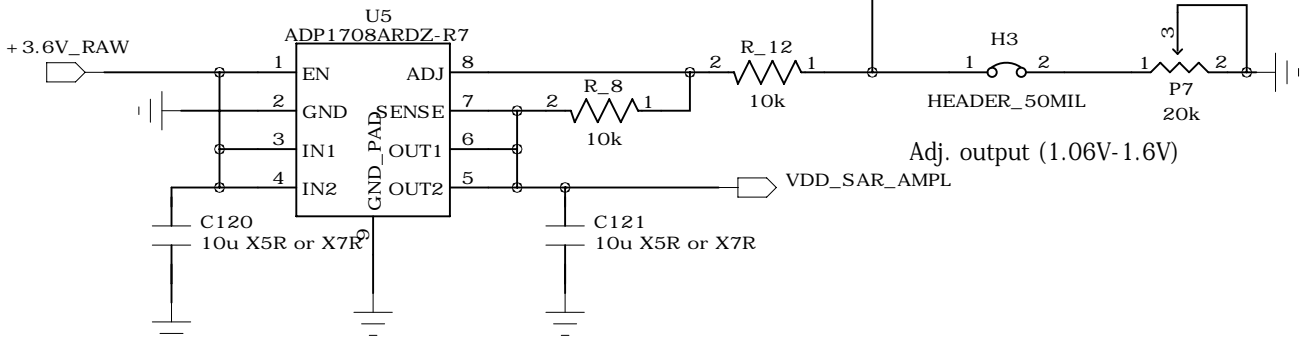
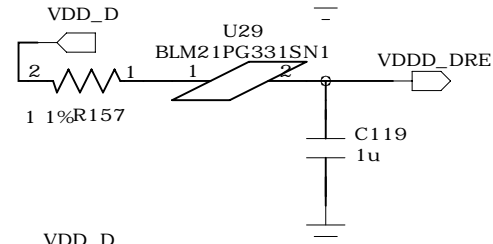
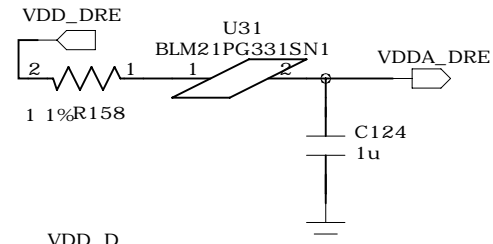
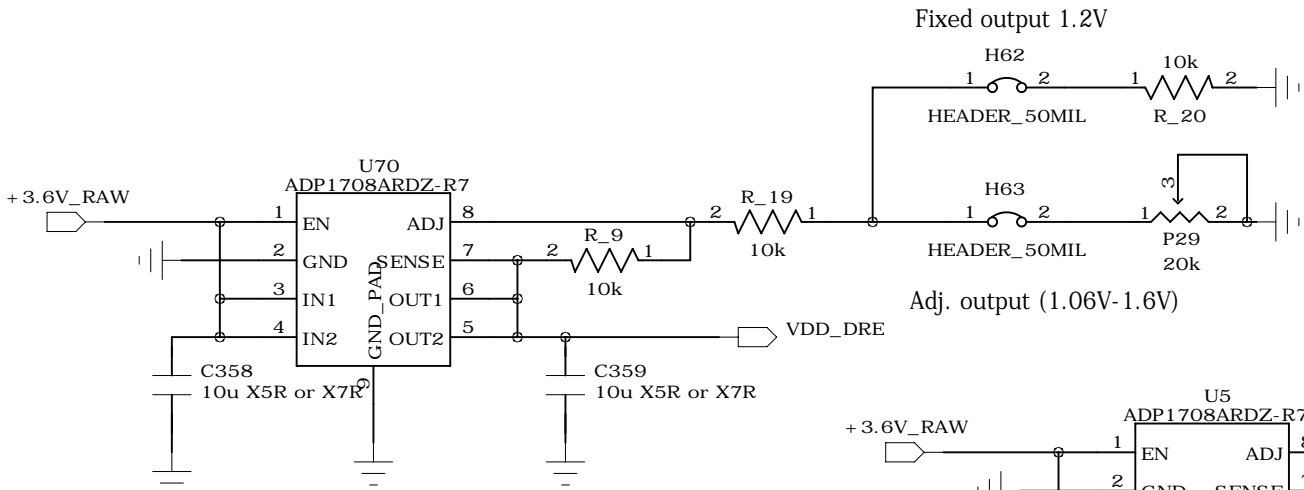
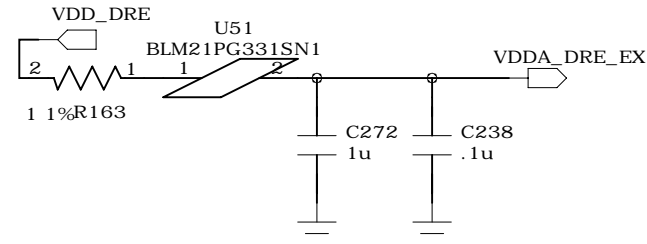
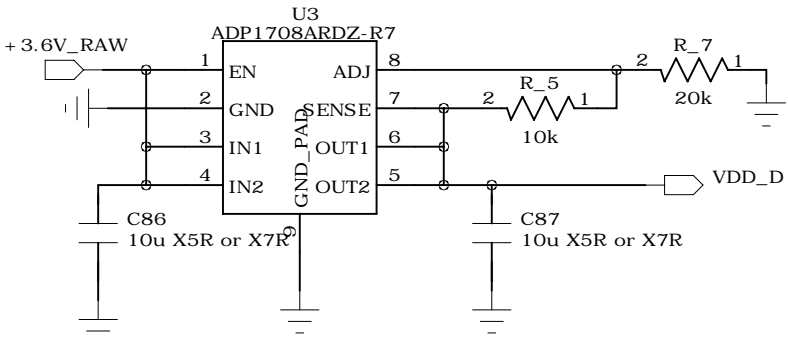
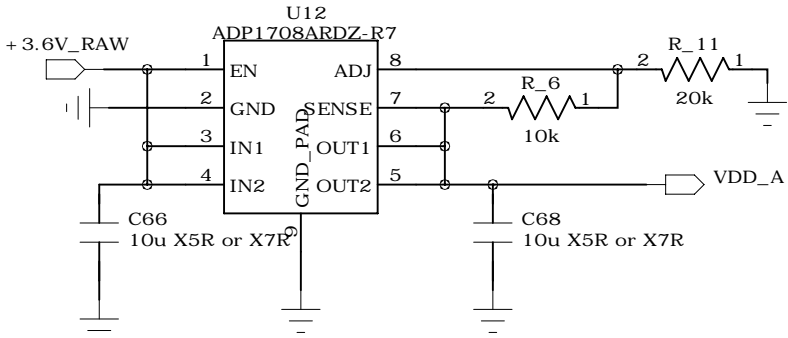
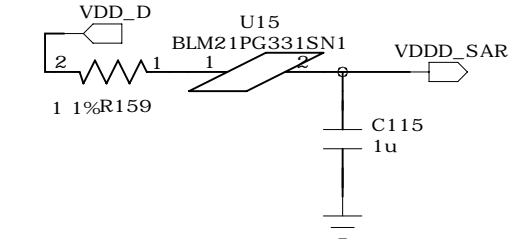
B

B

A

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE: < Code >	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:		SHEET: 01 27	

DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

6

5

4

3

2

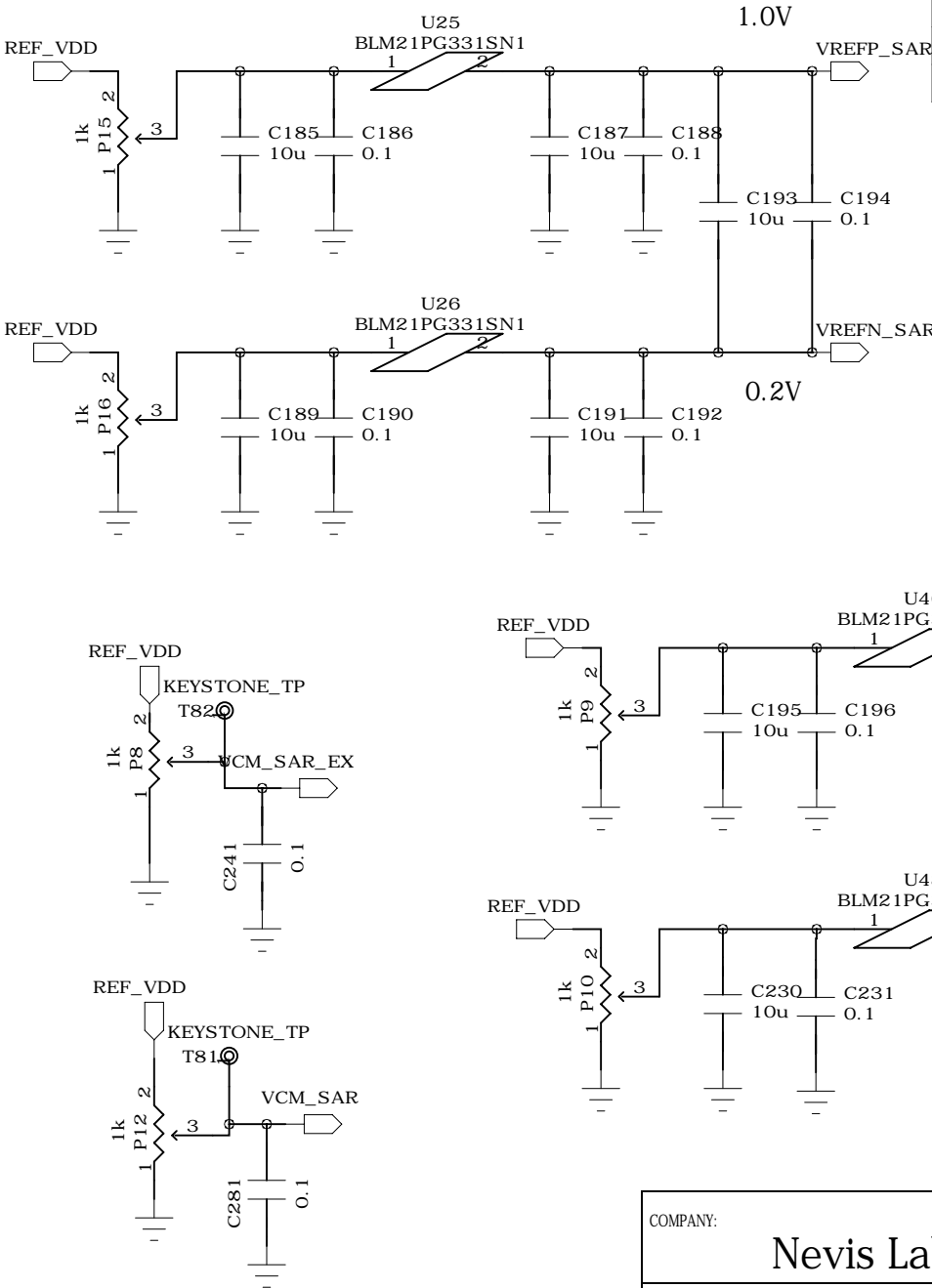
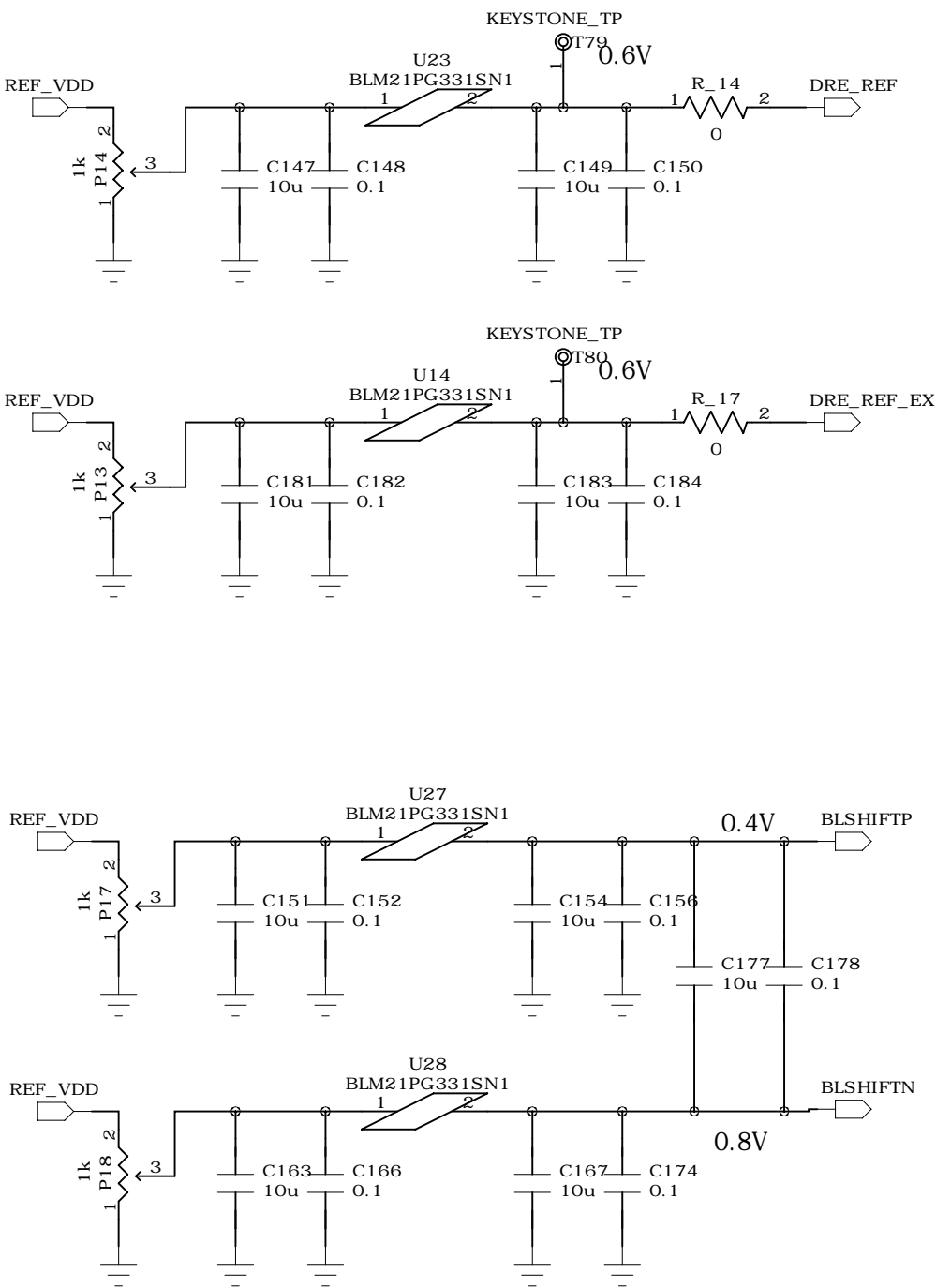
1

D

C

B

A



REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

D

C

B

A

COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:	jb	DATED:	

CODE:	SIZE:	DRAWING NO:	REV:
	B	v0	0
SCALE:	SHEET: of 1 27		

D

C

B

A

6

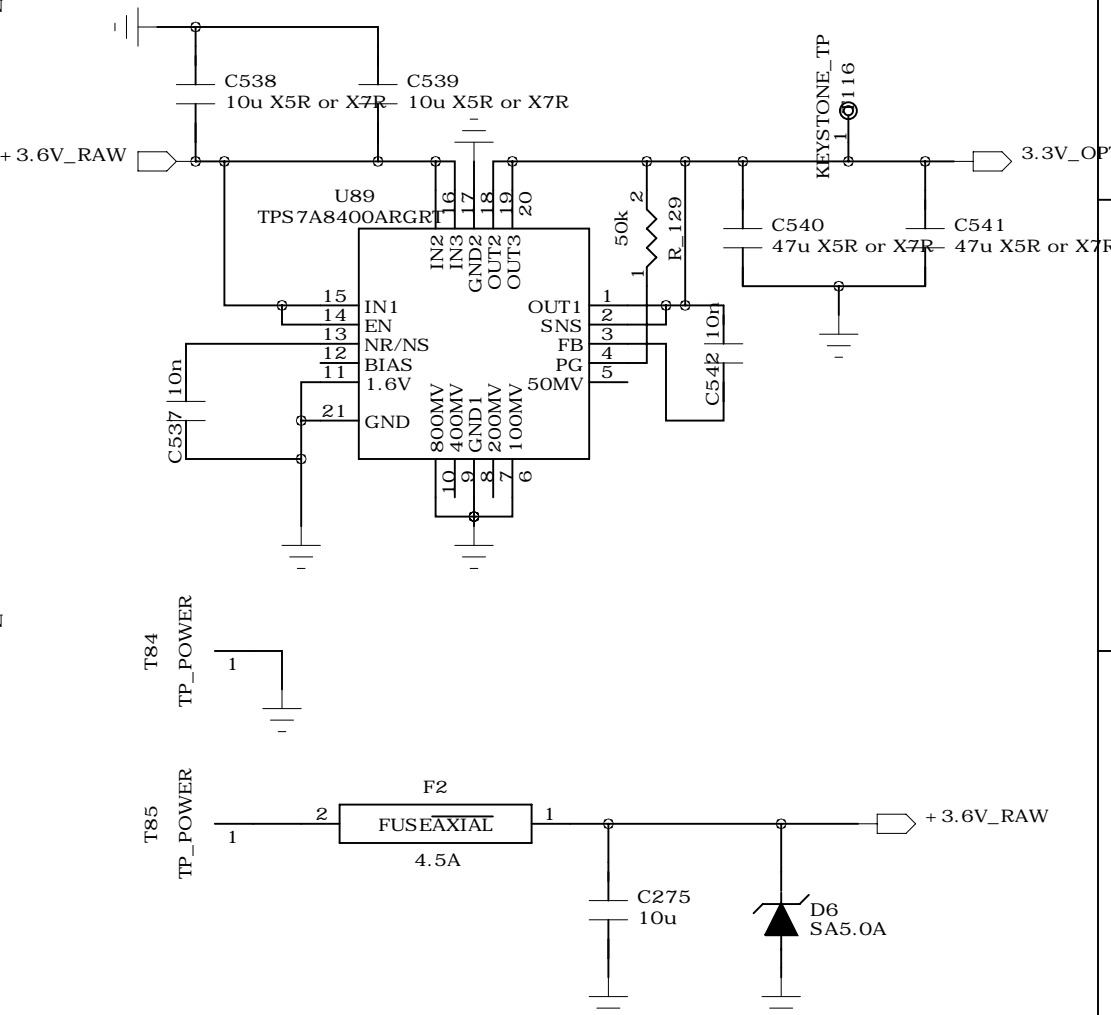
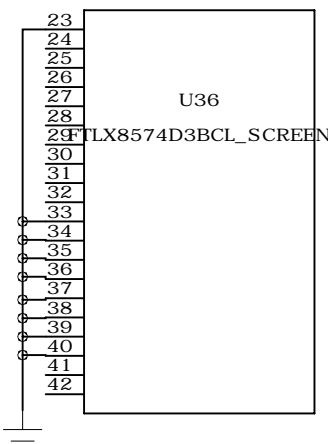
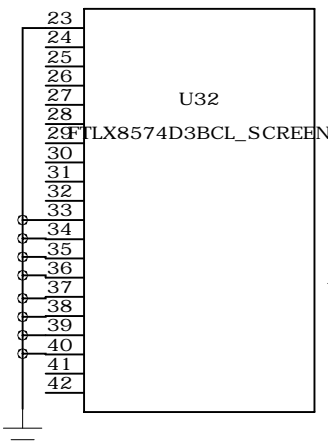
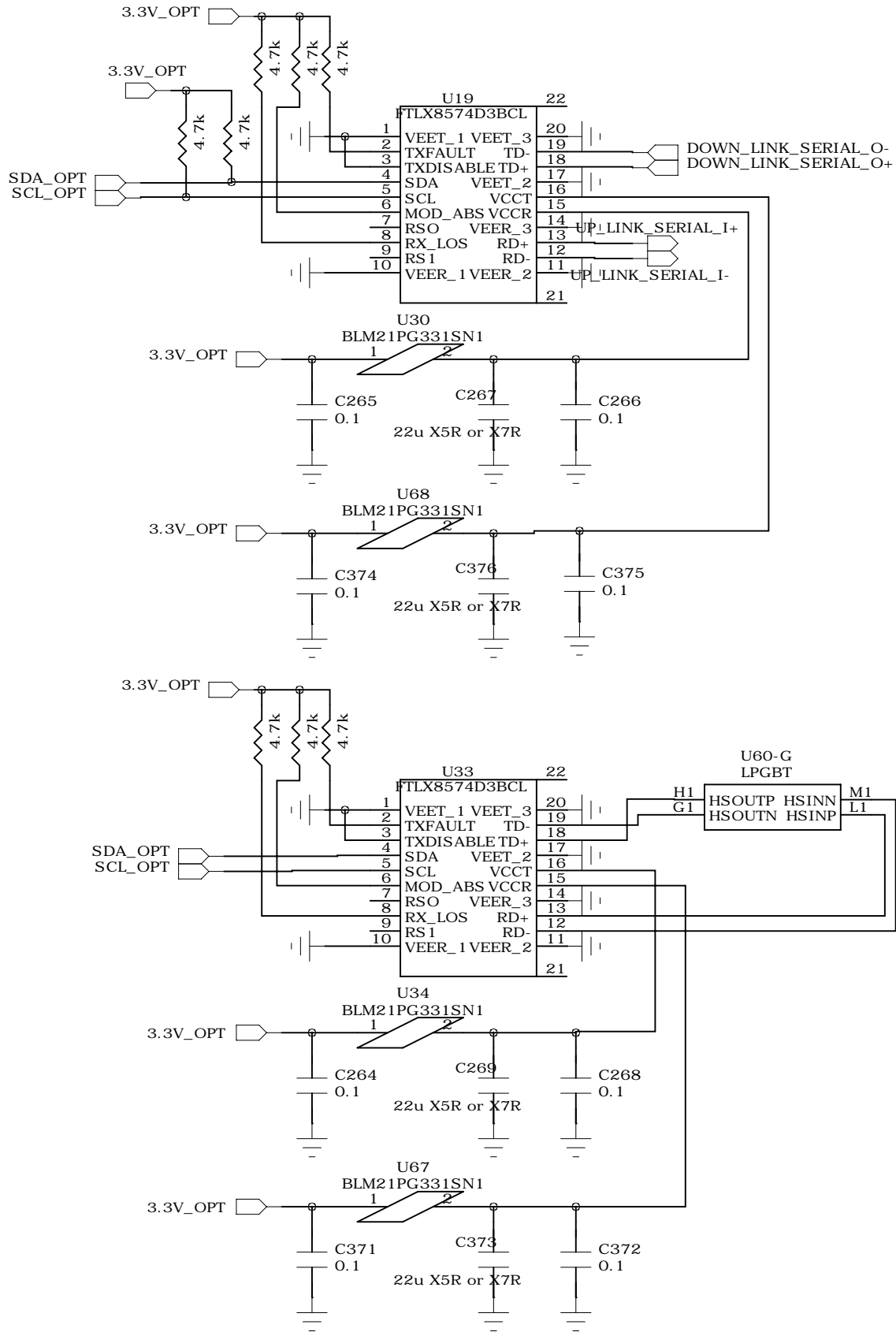
5

4

3

2

1



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE: < Scale >		SHEET: 14 27	

DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED: < Release Date >

6

5

4

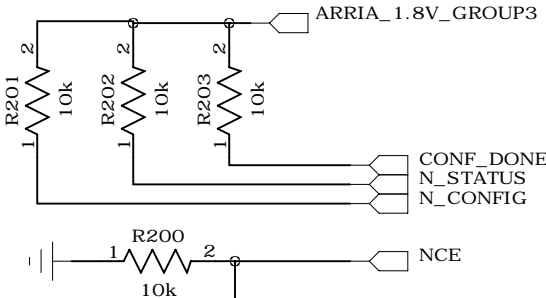
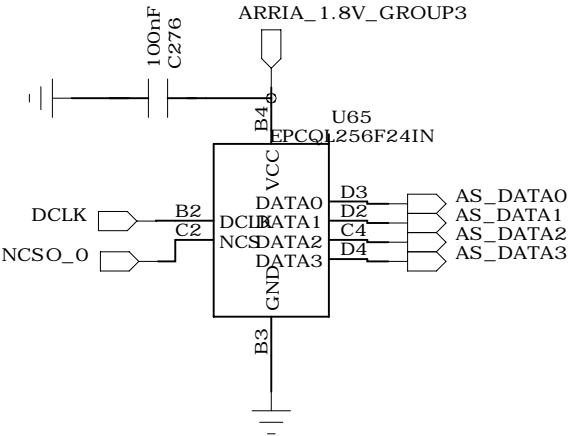
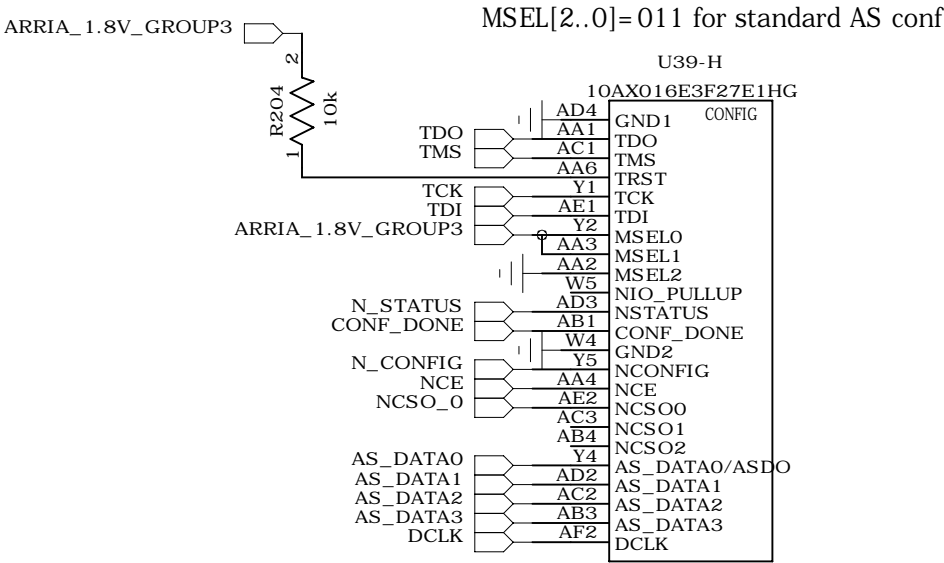
3

2

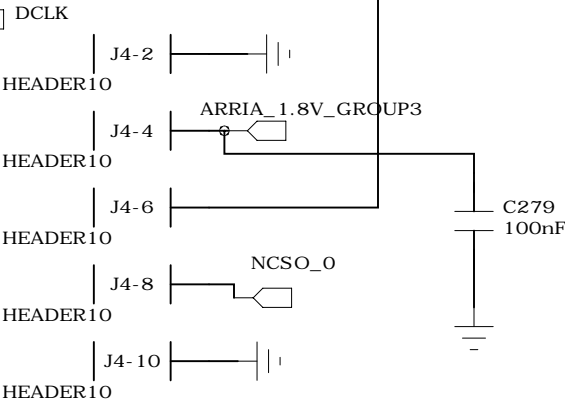
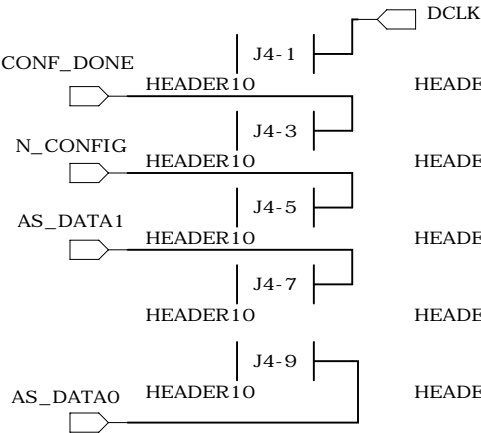
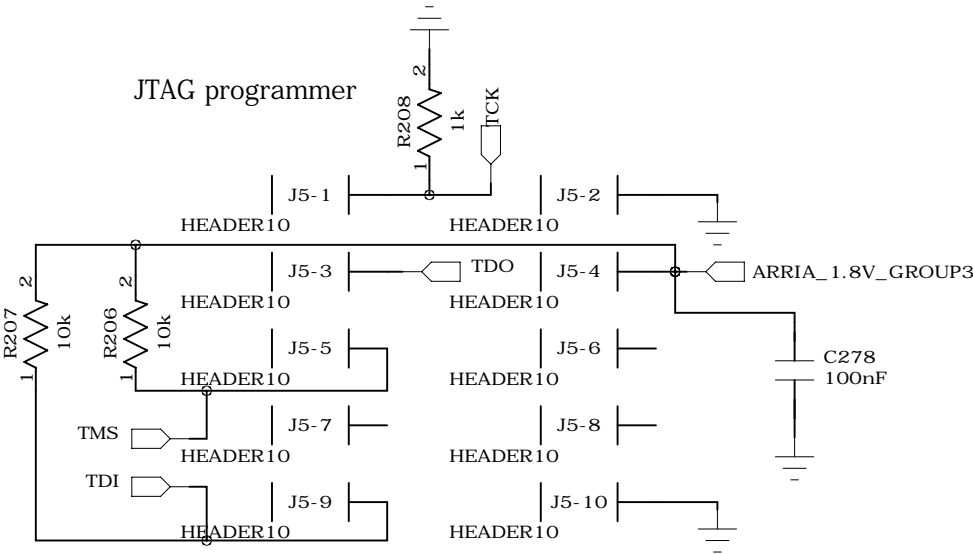
1

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:



JTAG programmer

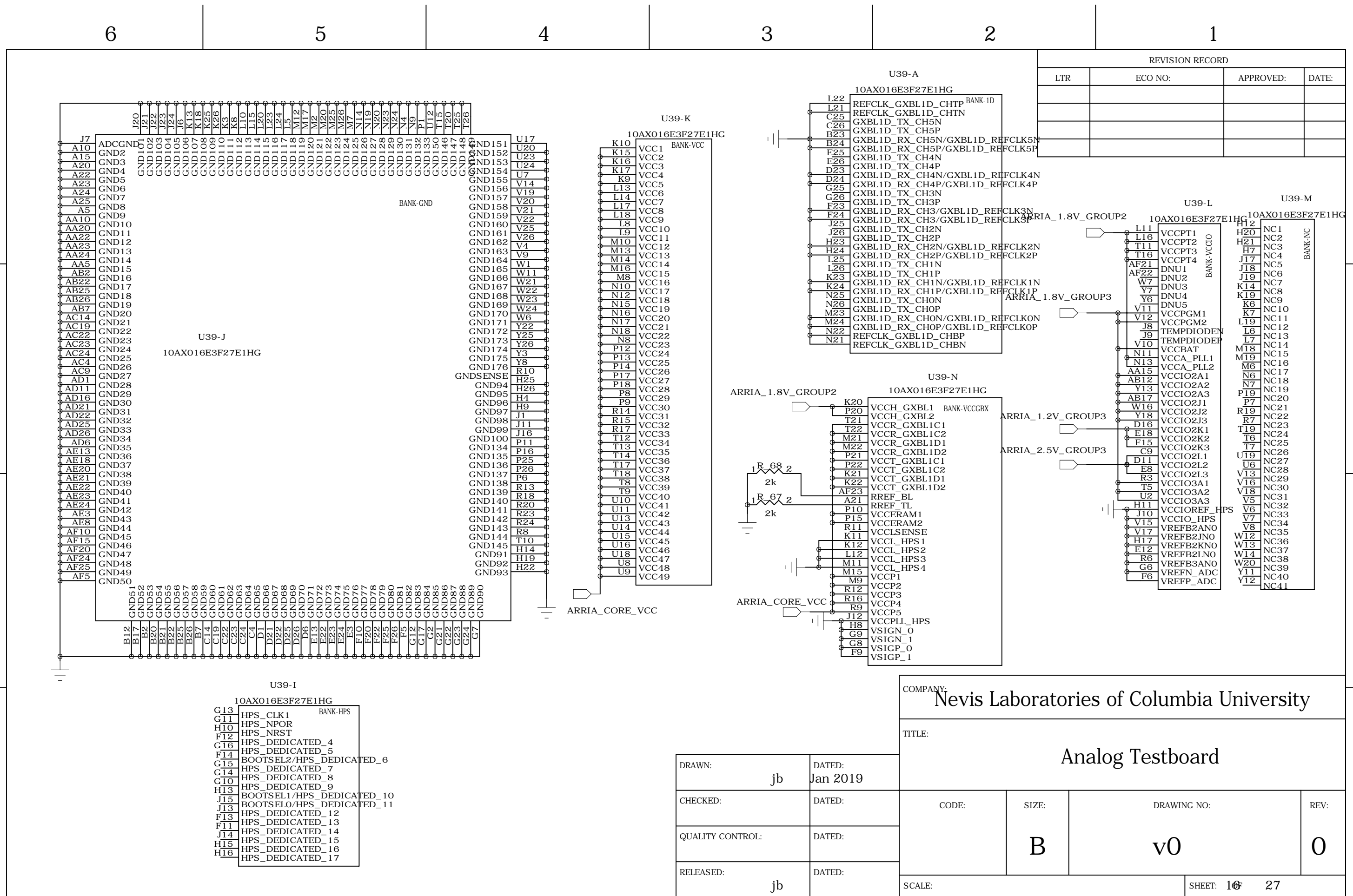


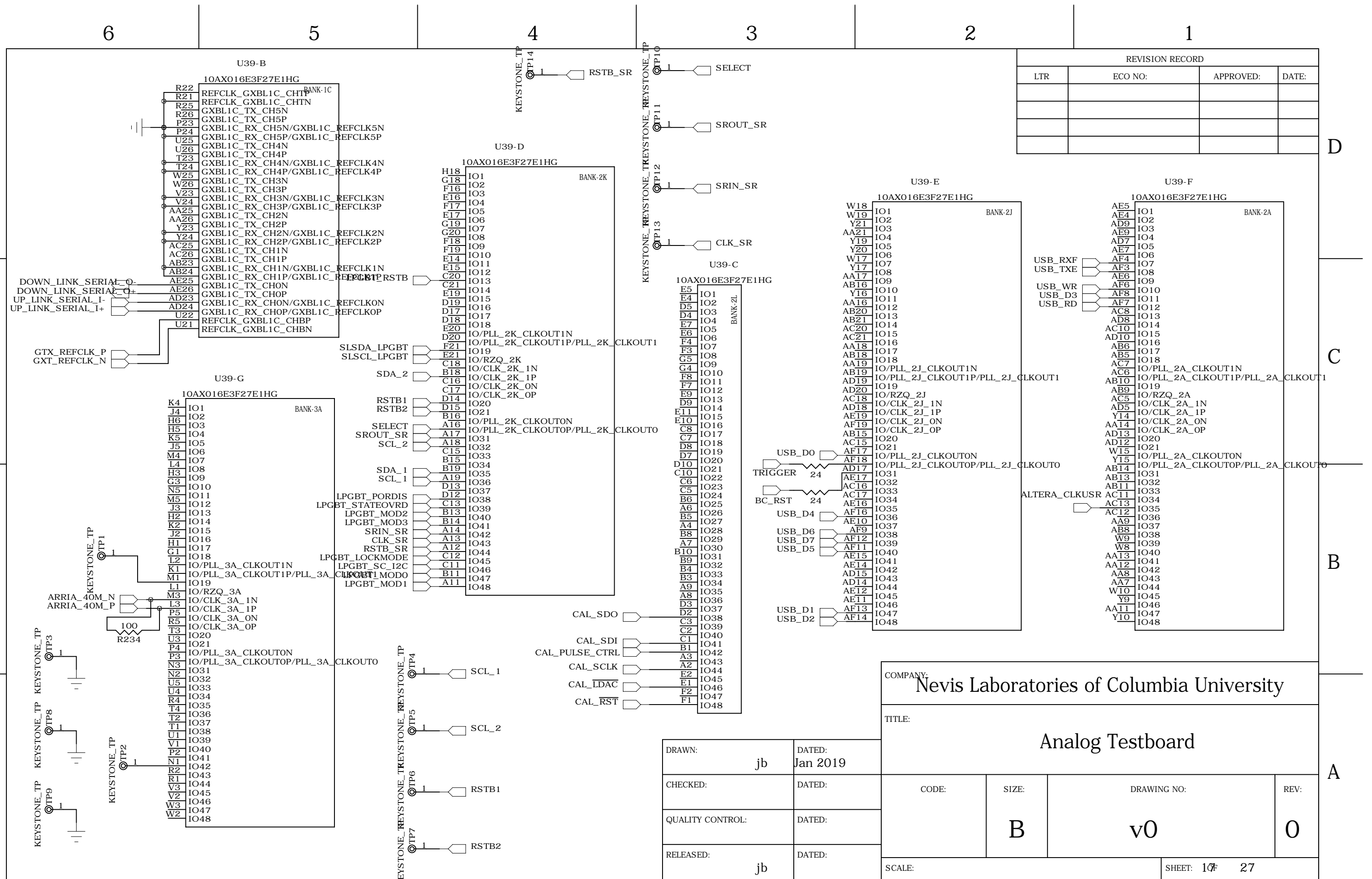
COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:	jb	DATED:	

CODE:	SIZE:	DRAWING NO:	REV:
	B	v0	0
SCALE:			SHEET: 15 27



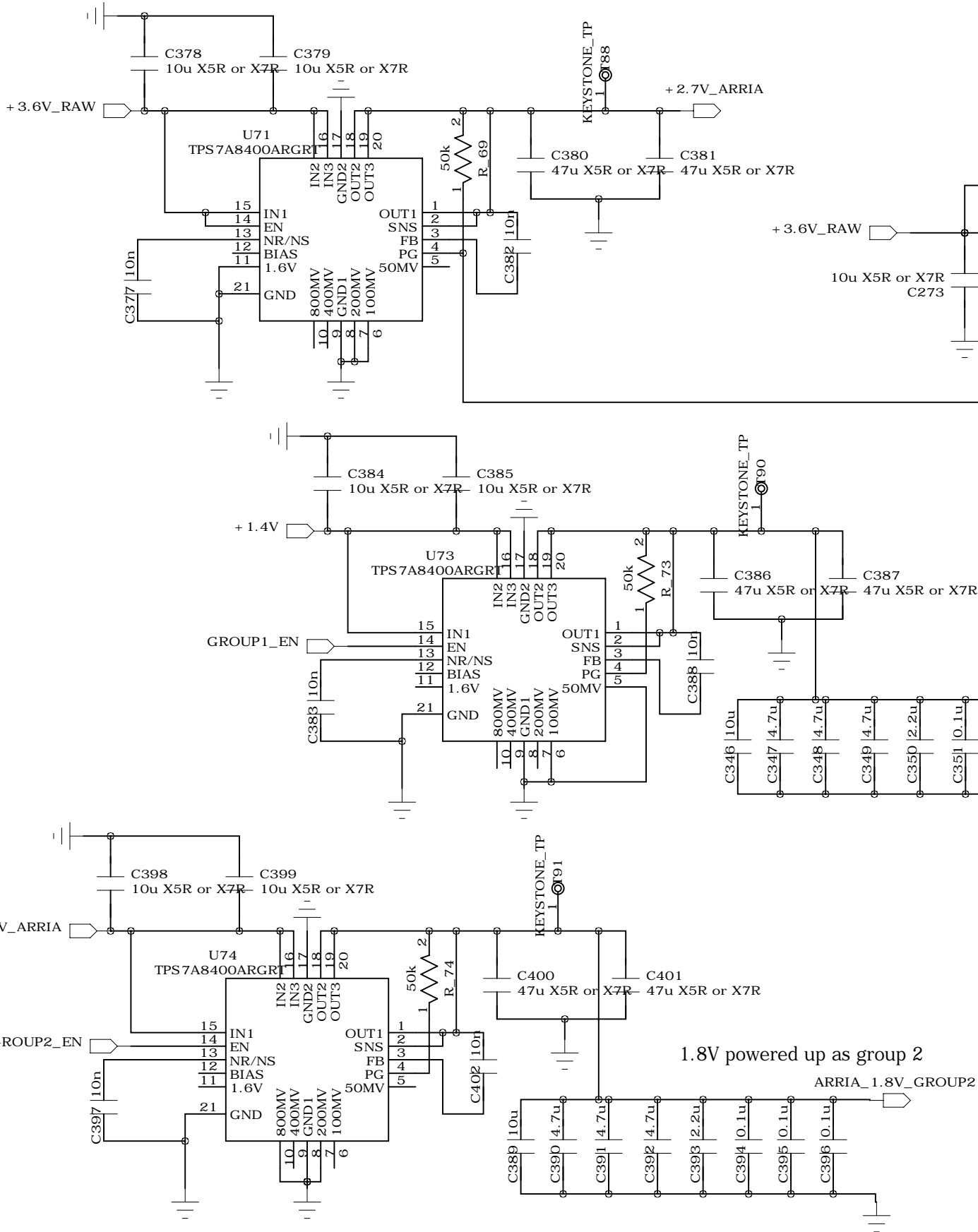


D

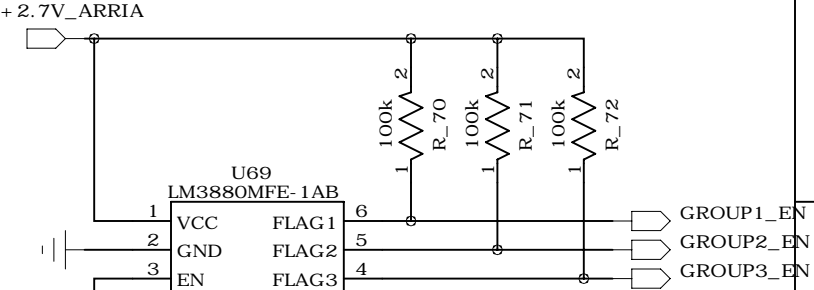
C

B

A



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN:	jb	DATED:	Jan 2019
CHECKED:	< Checked By >	DATED:	< Checked Date >
QUALITY CONTROL:	< QC By >	DATED:	< QC Date >
RELEASED:	jb	DATED:	< Release Date >

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE: < Code >	SIZE: B	DRAWING NO: v0	REV: 0
SCALE: < Scale >			SHEET: 18 27

D

C

B

A

6

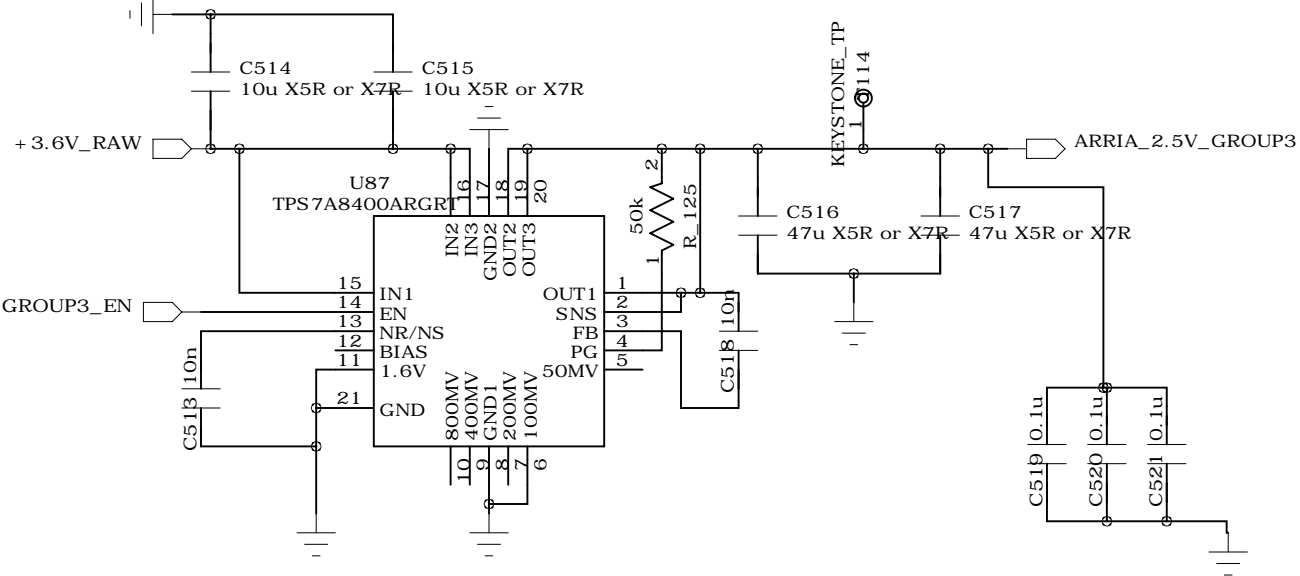
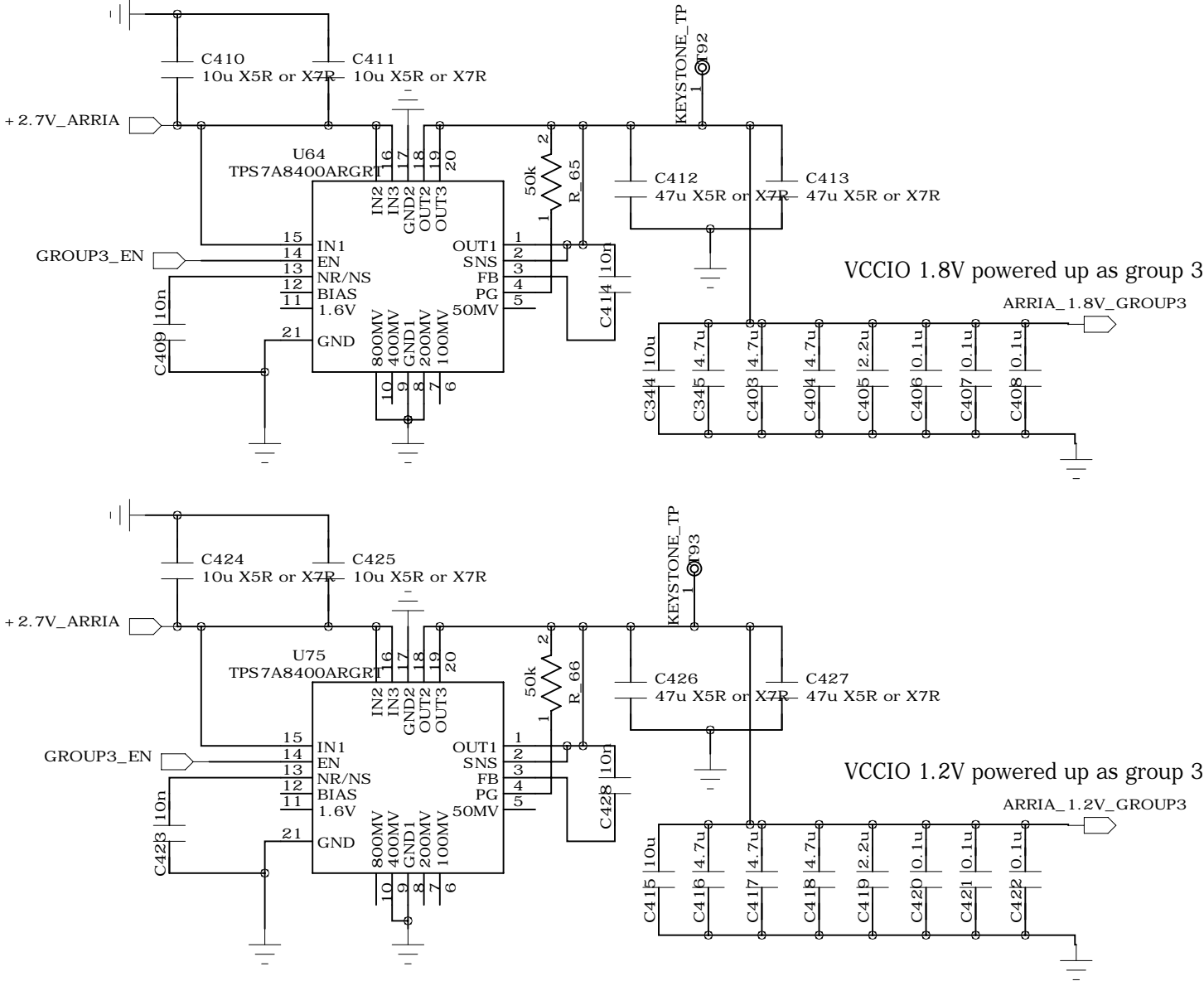
5

4

3

2

1



COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE: < Code >	SIZE: B	DRAWING NO: v0	REV: 0
SCALE: < Scale >		SHEET: 10 27	

DRAWN: jb	DATED: Jan 2019
CHECKED: < Checked By >	DATED: < Checked Date >
QUALITY CONTROL: < QC By >	DATED: < QC Date >
RELEASED: jb	DATED: < Release Date >

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

C

B

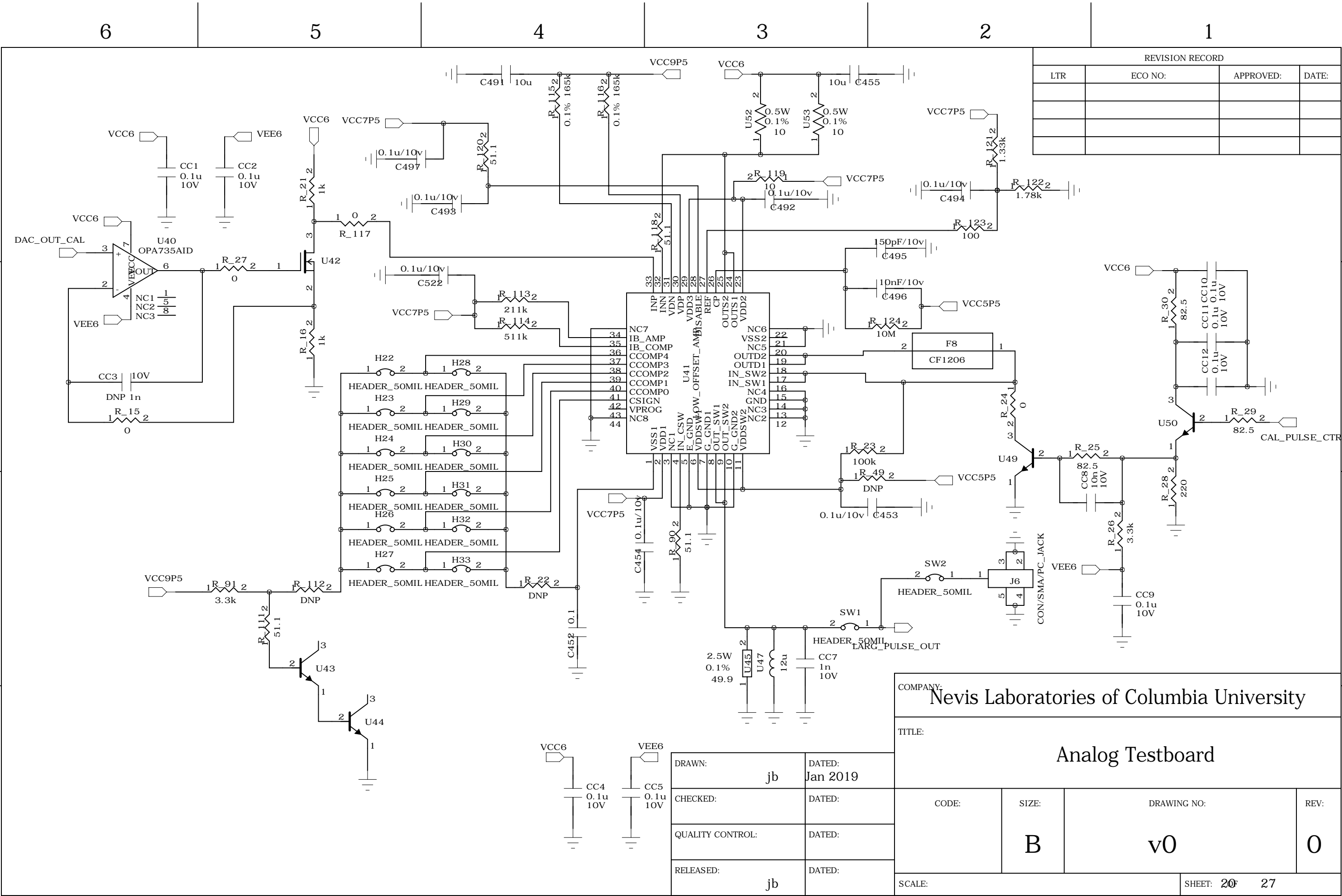
A

D

C

B

A



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:			SHEET: 20 27

6

5

4

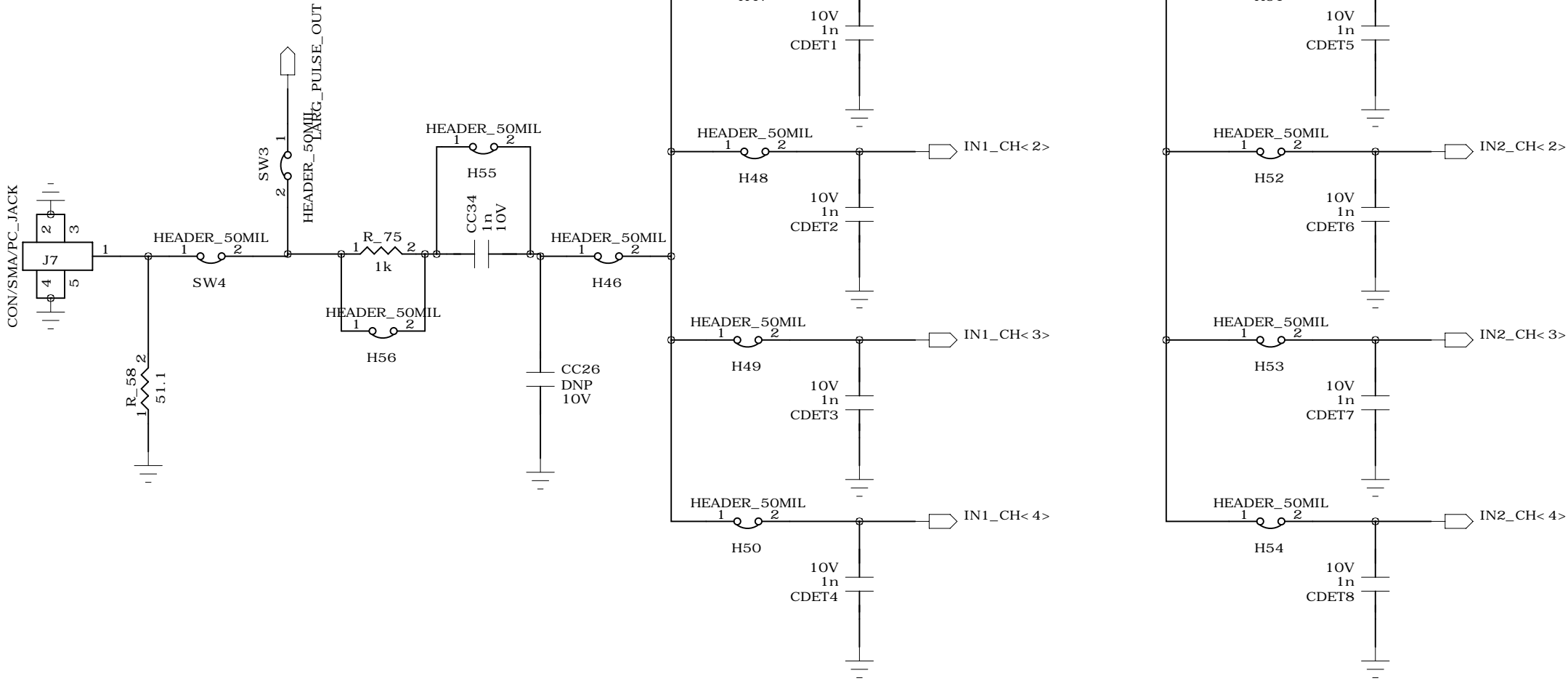
3

2

1

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:



COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN:	jb	DATED:	Jan 2019
CHECKED:		DATED:	
QUALITY CONTROL:		DATED:	
RELEASED:	jb	DATED:	

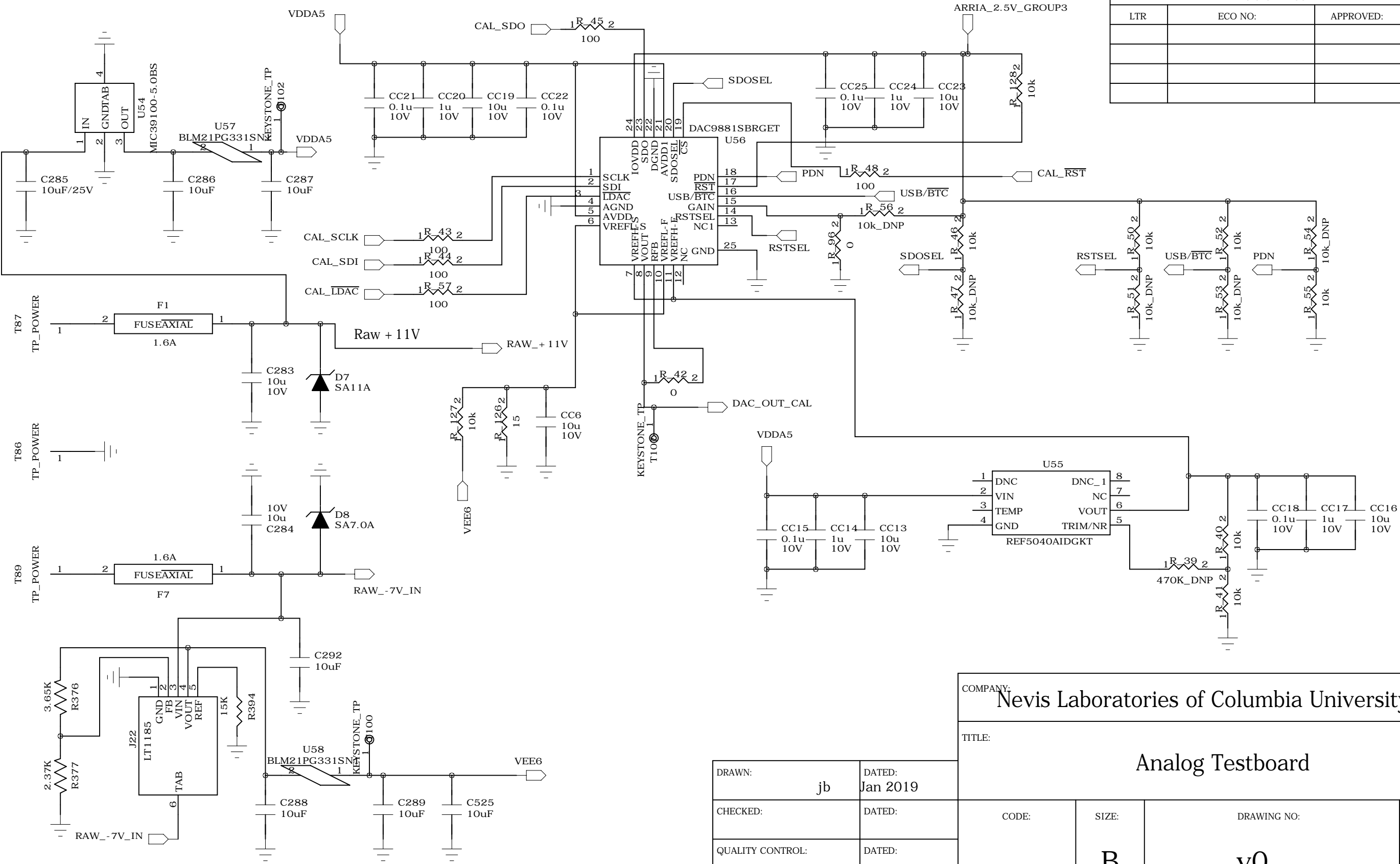
CODE:	SIZE:	DRAWING NO:	REV:
< Code >	B	v0	0
SCALE:		SHEET: 21 of 27	

D

C

B

A



D

C

B

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:		SHEET: 20 27	

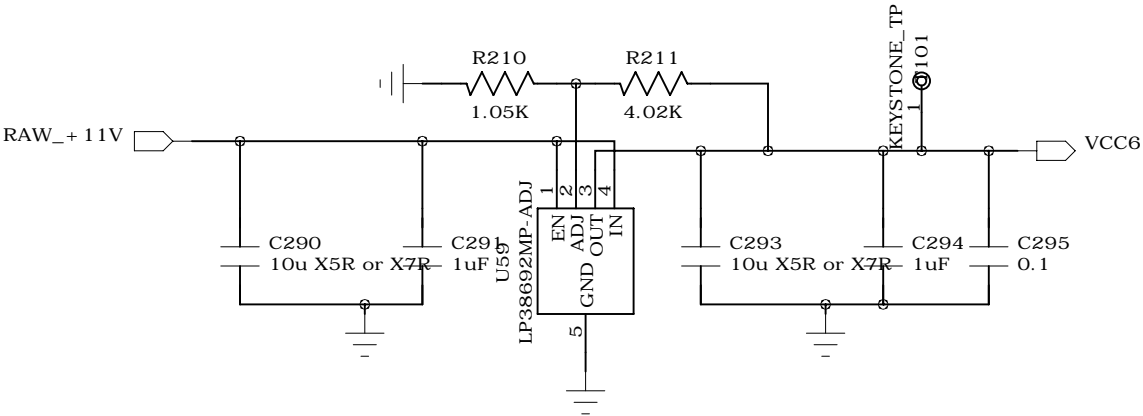
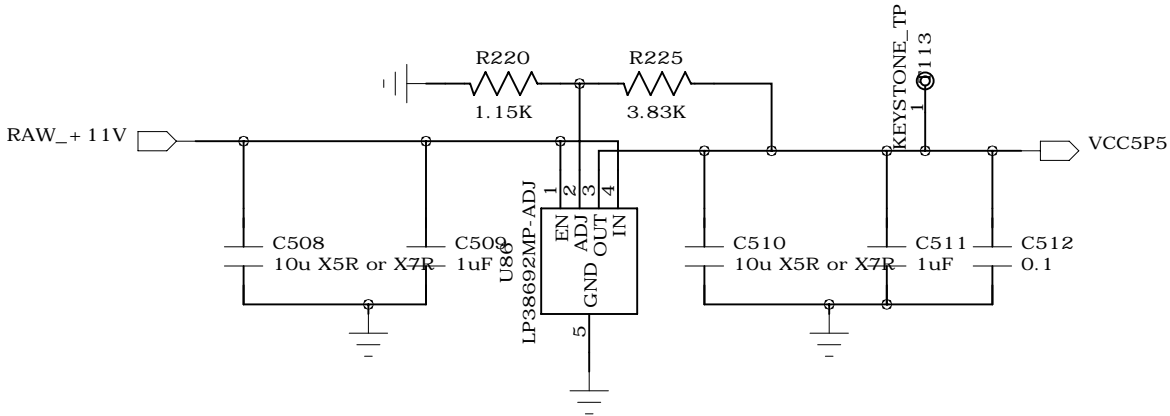
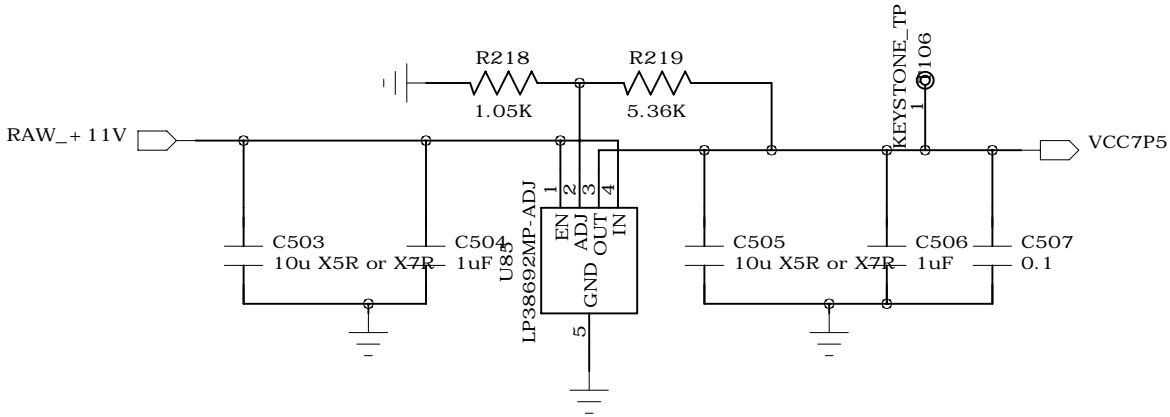
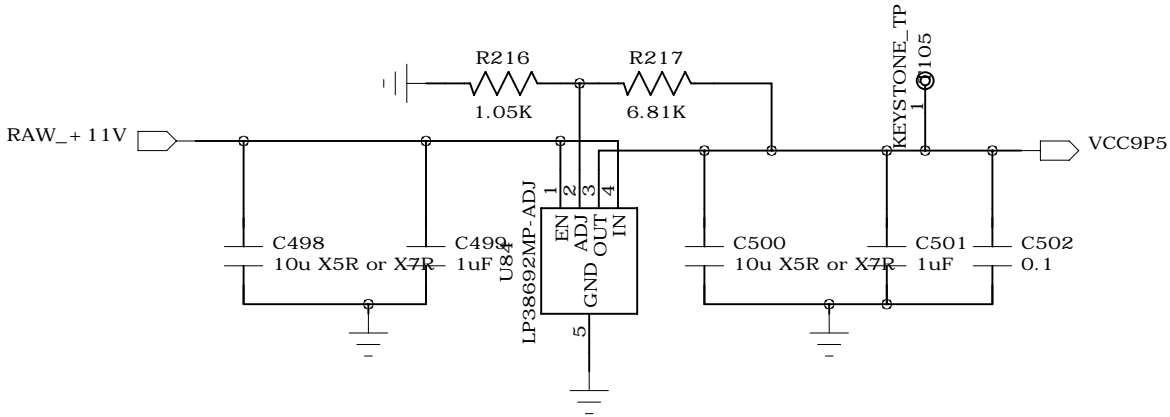
DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

D

C

B

A



REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

D

C

B

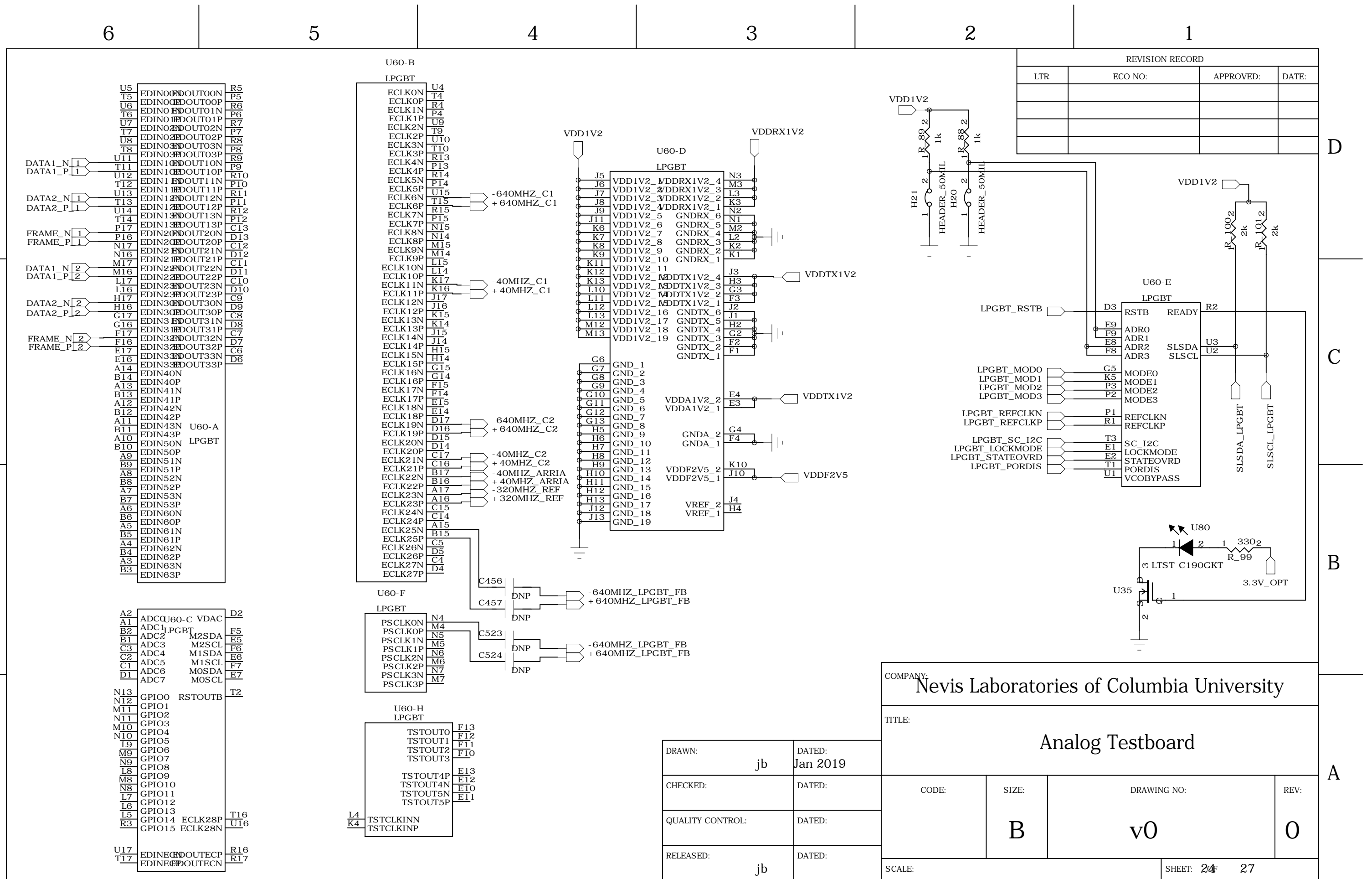
A

COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN: jb	DATED: Jan 2019
CHECKED: < Checked By>	DATED: < Checked Date>
QUALITY CONTROL: < QC By>	DATED: < QC Date>
RELEASED: jb	DATED: < Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
< Code>	B	v0	0
SCALE: < Scale>			SHEET: 26 27



6

5

4

3

2

1

D

C

B

A

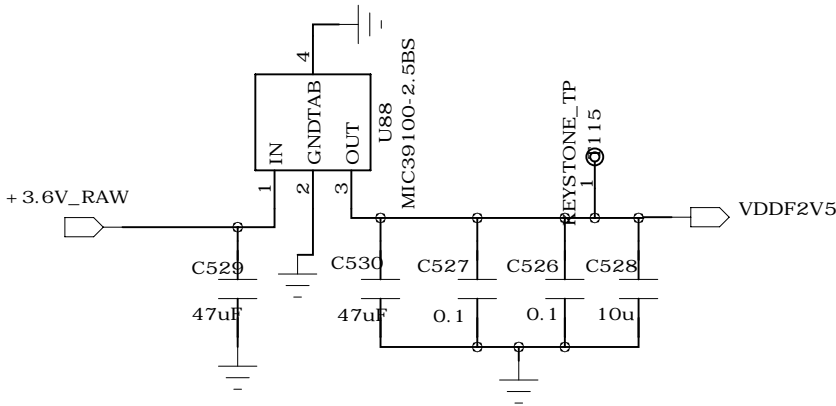
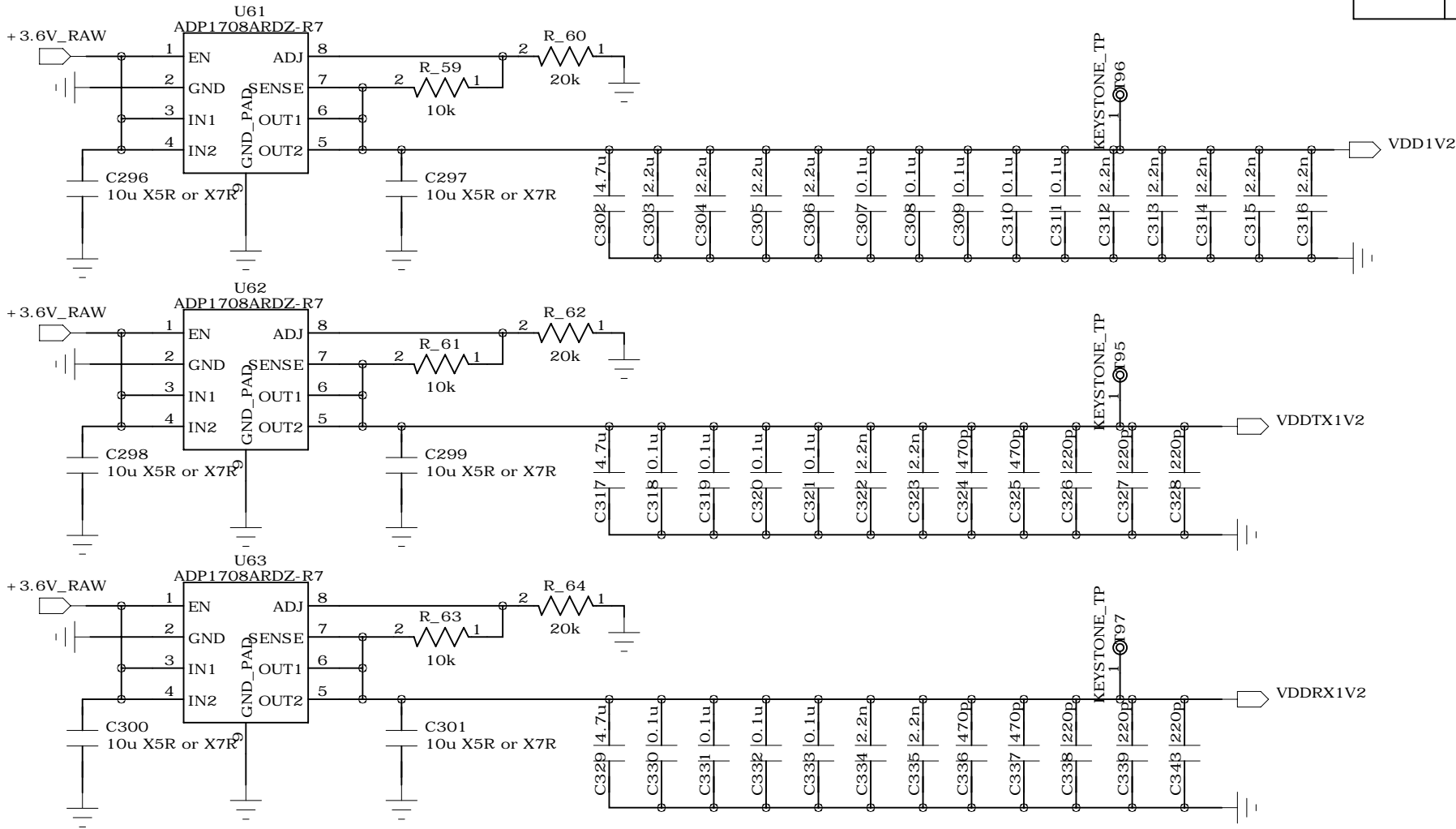
D

C

B

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: Nevis Laboratories of Columbia University			
TITLE: Analog Testboard			
CODE:	SIZE: B	DRAWING NO: v0	REV: 0
SCALE:		SHEET: 25 27	

DRAWN: jb	DATED: Jan 2019
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED: jb	DATED:

D

C

B

A

6

5

4

3

2

1

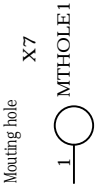
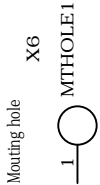
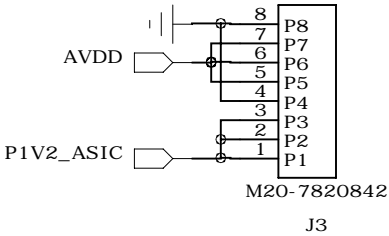
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

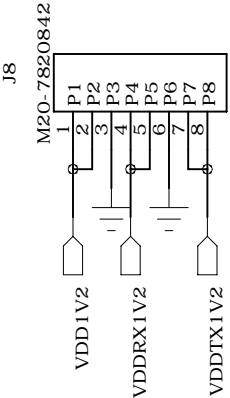
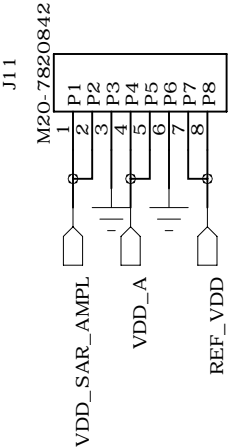
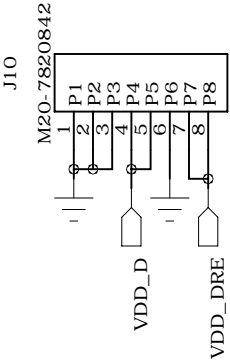
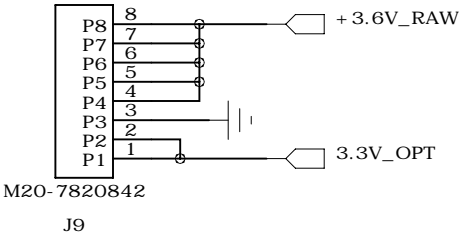
C

B

A



These connectors are to be used
to replace the board power regulator with radiation hard ones
Position/pins of the connectors corresponds 1: 1 to the PCB board connectors



COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN: jb	DATED: Jan 2019
CHECKED: < Checked By>	DATED: < Checked Date>
QUALITY CONTROL: < QC By>	DATED: < QC Date>
RELEASED: jb	DATED: < Release Date>

CODE:	SIZE:	DRAWING NO:	REV:
< Code>	B	v0	0
SCALE: < Scale>			SHEET: 26 27

6

5

4

3

2

1

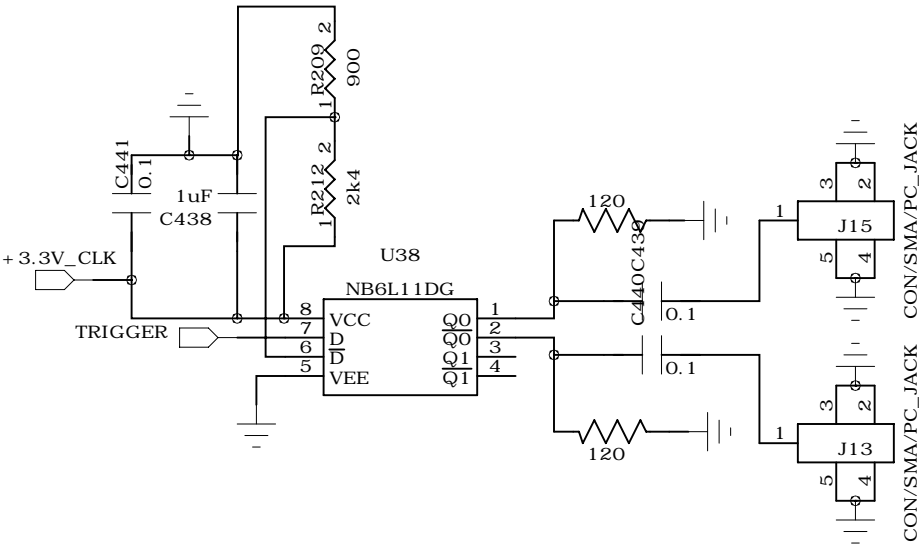
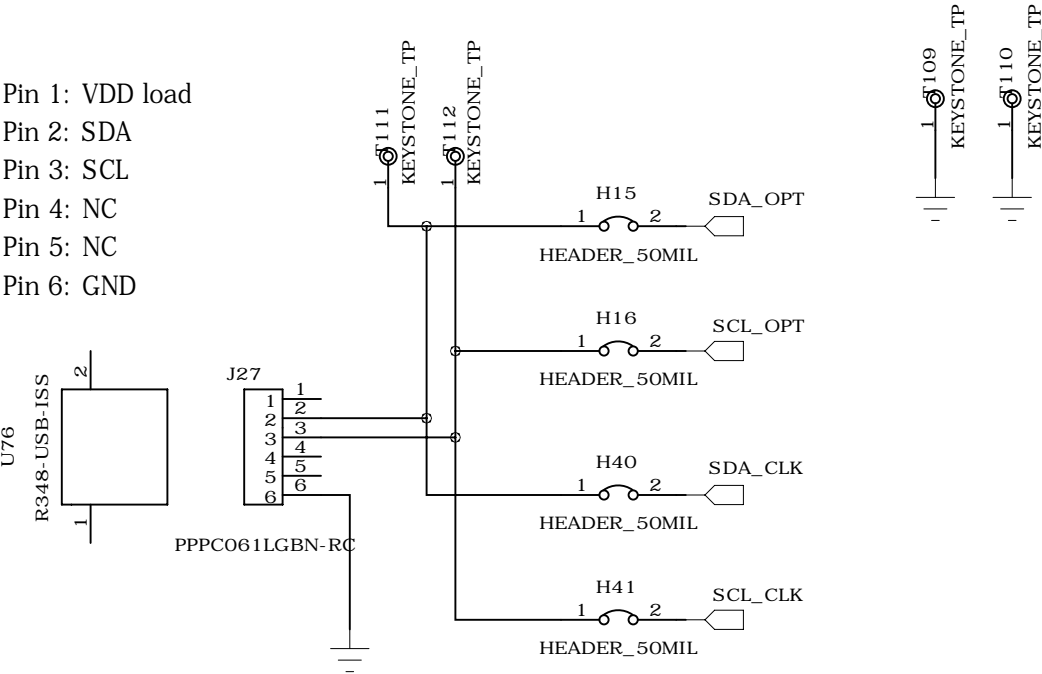
D

C

B

A

External I2C tool mfg: Devantech; model: USB-ISS; right-angle male header option
USB-ISS is mounted on top side of motherboard, upside-down
Default USB-ISS config: bootloader jumper open; power jumper closed; I2C mode only



COMPANY: Nevis Laboratories of Columbia University

TITLE: Analog Testboard

DRAWN: jb	DATED: Jan 2019	CODE:	SIZE: B	DRAWING NO: v0	REV: 0
CHECKED: < Checked By>	DATED: < Checked Date>	< Code>			0
QUALITY CONTROL: < QC By>	DATED: < QC Date>				
RELEASED: jb	DATED: < Release Date>	SCALE: < Scale>			SHEET: 27 27